Interleaved PWM with Discontinuous Space-Vector Modulation

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***Abstract*— This paper describes the effect of interleaved discontinuous space-vector modulation (SVM) in paralleled three-phase systems using three-phase pulsewidth modulation (PWM) rectifiers as an example. At the discontinuous point of the SVM, the phase shift between the switching signals of the paralleled modules generates a zero-sequence excitation to the system. Because the conventional control in a balanced three-phase system with only dq channels cannot reject this disturbance, a beat-frequency circulating current will develop on the zero axis. Based on this observation, a SVM without using zero vectors is used to eliminate the cause of pure zero-sequence current for parallel operation. Using this SVM, the circulating current is observable in dq channels. It can be suppressed dynamically by strong current loops of power-factor-correction (PFC) circuits. The concept is verified experimentally on a breadboard system.**

***Index Terms*— Circulating current, discontinuous space-vector modulation, interleaved PWM, parallel three-phase system, power electronics building blocks (PEBB's), zero-axis current.**

I. Introduction

PARALLEL three-phase power converters/inverters have many advantages, such as higher current capability, less current/voltage ripple, and higher system bandwidth. Previous research exists in applications of UPS, motor drive, and power factor improvements [1]–[6]. As insulated gate bipolar transistors (IGBT's) and other power semiconductor devices are being integrated with gate drives and control intelligence as standardized modules, such as integrated power module (IPM), it becomes quite natural to parallel directly more of these modules together, either to increase the power level and boost the current capability or to design a system with a higher redundancy.

Putting modules in parallel, however, is not risk free. One of the major concerns for the parallel operation of a three-phase system is the crosscoupling between modules because when these modules are connected to the same dc bus and a common source/load, extra current conduction paths are formed. Traditionally, in order to avoid this problem, transformers are used to isolate the direct current flow. These transformers are designed with a certain winding turns-ratio and a certain phase shift, so that the concerned harmonics can be canceled in the other side [3], [7]. However, the transformer is heavy and bulky for the inverters with low-modulation frequency, especially for a high-power application. It may occupy too much space in airplanes, ships, etc. Therefore, a direct connection between the power converter module and power system is desirable.

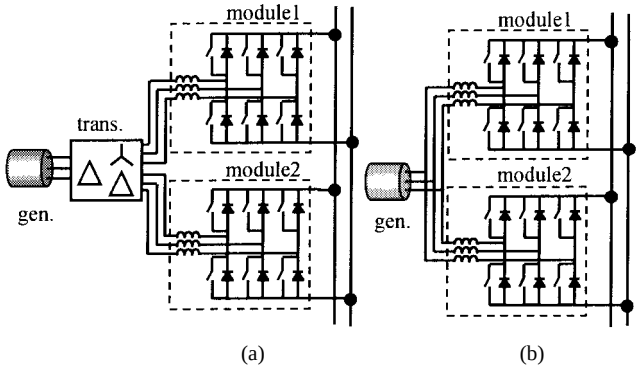

Fig. 1. Typical configurations of parallel rectifier on a single source (a) with a phase-shifted transformer and (b) with a interleaved PWM.

A three-phase pulsewidth modulation (PWM) rectifier with its unity power factor and tightly regulated dc output is one of the best candidates for the front-end dc power supply for medium to high-power applications. Much literature has documented the design, control, and operation of the rectifier [8]–[10]. In the dc-distributed power system (DPS), with a very strict requirement of redundancy, it is desirable to parallel three-phase PWM rectifiers to feed the dc bus [11]. Fig. 1(a) and (b) shows typical system configuration schemes for the DPS with rectifier modules paralleled on a single voltage source. Fig. 1(a) shows one with a phase-shifted transformer isolation connection, and Fig. 1(b) shows another with an interleaved PWM direct connection. In this paper, the discussions will concentrate on the interactions between the directed paralleled rectifiers, as shown in Fig. 1(b).

In a balanced three-phase system, the control usually is implemented in a rotating coordinate with a digital controller. In such a system, the dq components are controlled as a circle rotating at an angular speed of the modulation frequency, the zero axis is not a concern. However, as three-phase systems are paralleled directly, the circulating current can exist in all the phases. This will be translated into d, q, and zero axes. The zero-sequence current on the zero axis is perpendicular to the dq plane, on which the dq channel controllers can do nothing. The literature reported several ways to reduce the "crosscurrent" between modules: 1) insertion of current

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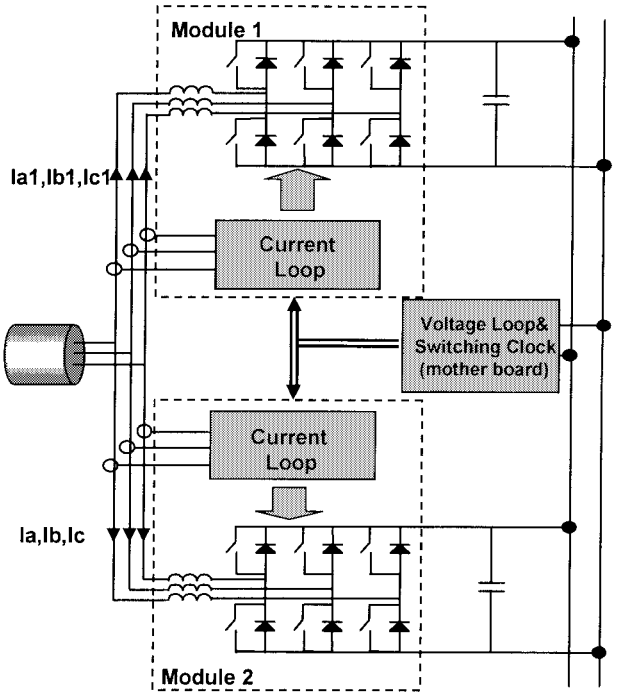

Fig. 2. System block diagram.

sharing reactors into the paralleled modules [1], [5], [6], [12], which includes two different cases, the coupled inductors are on the ac side for the VSI or the dc side for the CSI; 2) use of the "bang–bang" hysteresis control [3], which confines the current within a band by varying the switching frequency; and 3) use of a "combined-mode" current control [6], which treats the paralleled system as one system. The crosscurrent is compensated by choosing proper voltage vectors through sensing the output current and their derivatives.

This paper looks for the control schemes for standardized three-phase modules. The module itself has a certain degree of intelligence, the objective of the research is to make these modules able to "plug and play" without communicating with each other. The desired features of such parallel modules include: 1) use of constant frequency control and advanced modulations techniques such as SVM; 2) keeping each module as independent as possible; and 3) having less communication between modules. Through a comprehensive system analysis using the averaged SVM model, this paper shows the mechanism of how the zero-sequence current is produced with the interleaved discontinuous SVM. It then investigates methods to mitigate the circulating current while maintaining each module with its own SVM, as with an individual module.

II. Analysis of the Circulating Current

A. System Configuration

The system block diagram shown in Fig. 2 consists of two three-phase modules. Each is composed of three phase legs, three input boost inductors, and a current loop controller. The phase leg has an IGBT module integrated with gate drives containing isolation, protection, and diagnosis functions. The current loop controller has the following functions integrated:

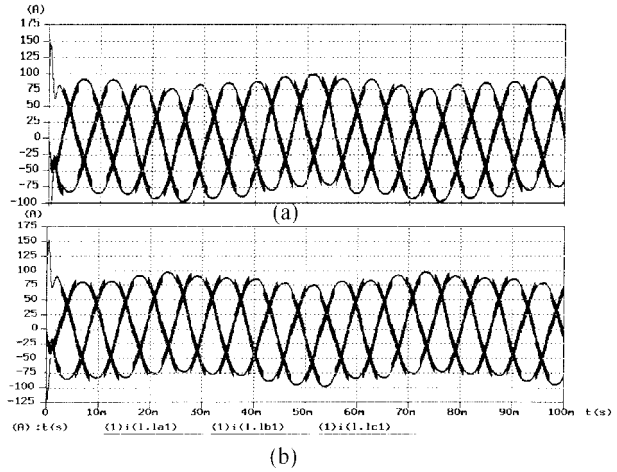

Fig. 3. Input current waveform of the paralleled modules.

- line voltage and current sensing and synchronization;
- current loop compensator;
- space-vector modulation.

The two modules are connected to a three-phase power supply at the ac side and a common dc bus at the dc side. Both accept two signals from the outside motherboard: 1) SVM interleave signal (180°) and 2) a current loop reference coming from the voltage compensator. The detailed system specifications and parameters are given in Section IV.

To reduce the total input current ripple, a 180° phase-shifted PWM is used. To ensure load current sharing, the common voltage loop provides the same current loop reference to the inner proportional–integral (PI) controller, which will track the given reference. In order to reduce the switching losses, a SVM with 60° clamping is used, which will be discussed in detail later. Although each module can be operated properly as a stand-alone unit, the interaction occurs when they are in a parallel configuration. Fig. 3 shows the simulated input current waveform of the two modules with a 20-kHz switching frequency at an input line frequency of 60 Hz.

As can be seen from the waveforms, the input current has a bias component with a 20-Hz beat frequency. This component makes the three-phase current deviate from the zero line alternatively. The bias current will trap the energy inside the converters, causing extra switching and conduction losses.

B. The Zero-Axis Current Caused by Interleaved Discontinuous SVM

There are many SVM schemes for three-phase PWM converters. The SVM with 60° clamping is most favorable for power-factor-correction (PFC) operation because the phases carrying the highest current in each 60° of line cycle are not switched. Calculations show that a 50% switching loss reduction and a very good total harmonic distortion (THD) can be achieved with this SVM [13]. To illustrate the principle of this SVM, S_a, S_b, and S_c are assumed to be the control signals for the top switches of a three-phase converter. When the reference vector is in sector 1, as shown in Fig. 4(a), where the phase A voltage and the current for PFC operation become the maximum compared to the other two phases, the top switch of

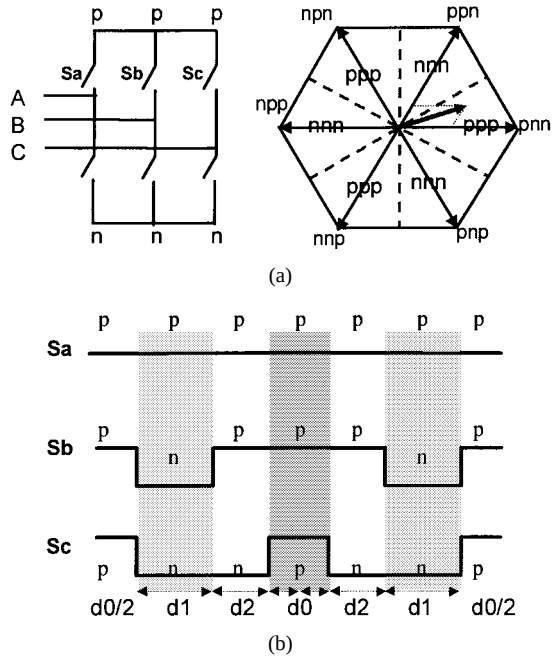

Fig. 4. The 60° clamped SVM.

phase A will keep in conduction all the time and phases B and C will do the modulation, as shown in Fig. 4(b). This means that only the ppp zero vector can be used in this 60° period of time. Extending this conclusion to a complete line cycle, a distribution of zero vectors in the hexagon can be obtained, as shown in Fig. 4(a), where the ppp and nnn vectors are used alternatively in each 60°.

Assuming that the SVM is a black box, the input to it is the modulation index from the dq (or alpha–beta) channel controllers and the switching clock. The output of this box is the control signals for active switching devices. The SVM calculation is essentially a process of mapping variables from the dq coordinate to the stationary coordinate through the space vectors. This process keeps the synthesized space vector rotating as a circle while leaving the zero axis free. As a consequence, it guarantees that the modulated line-to-line voltage always will be sinusoidal and realizes a higher line-to-line voltage with a given dc bus by actually injecting a common mode signal into the phases. Different modulation schemes inject different shapes of common mode signal. The magnitude of the common mode signal changes as a function of the modulation index.

By averaging the output of the SVM, a cycle-by-cycle average model of the SVM is obtained. In this model, instead of providing the gate signal as a pulse in each switching cycle, the SVM generates the duty ratio in terms of D_a, D_b, and D_c, as shown in Figs. 5 and 6. D_a, D_b, and D_c are discrete values comprised of small pieces of duty ratios averaged in each switching cycle.

Fig. 6(a) and (b) shows the relationships between the discrete and the averaged SVM. Fig. 6(a) shows the current reference signal and the discrete gate signal, which is at much higher frequency than the line frequency. Fig. 6(b) shows the averaged duty cycle. It can be seen that the averaged duty cycle is discontinuous at each transition of 60°.

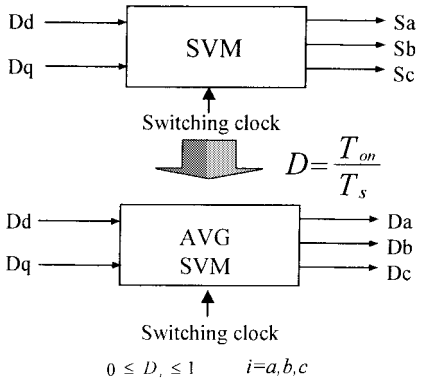

Fig. 5. An average model of SVM.

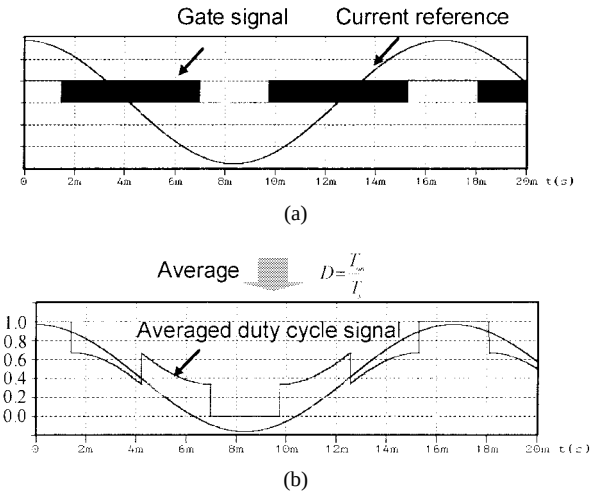

Fig. 6. The output of the SVM and averaged SVM.

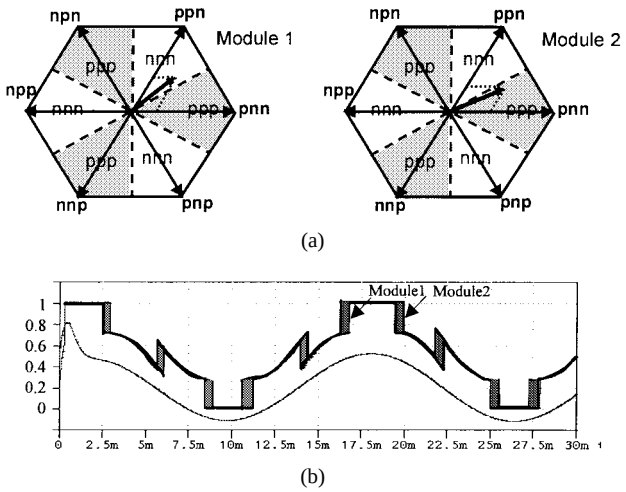

Fig. 7. (a) The position of reference vectors when passing the discontinuous point. (b) The duty-cycle difference of the interleaved discontinuous SVM.

Because of the interleaved switching clock, the reference vectors of the paralleled module do not cross over the discontinuous point at the same time. This is illustrated in Fig. 7(a) and (b). The dashed lines inside the hexagon of Fig. 7(a) correspond to the discontinuous points. The difference between the interleaved duty cycles is exaggerated in Fig. 7(b) as the shaded area. The module that passes the discontinuous point

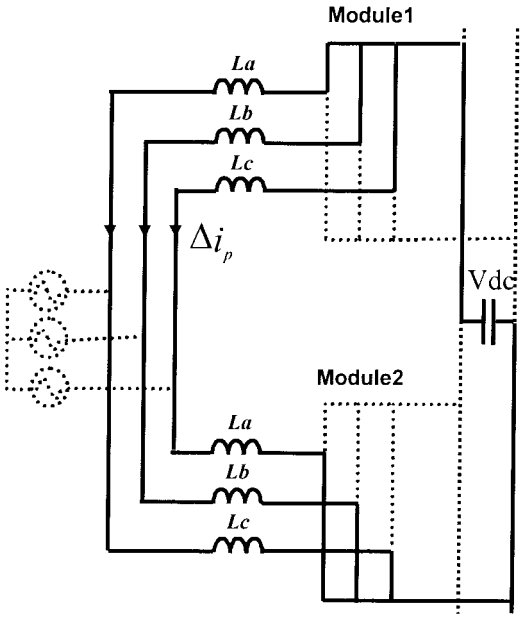

Fig. 8. The path of the pure zero-sequence current.

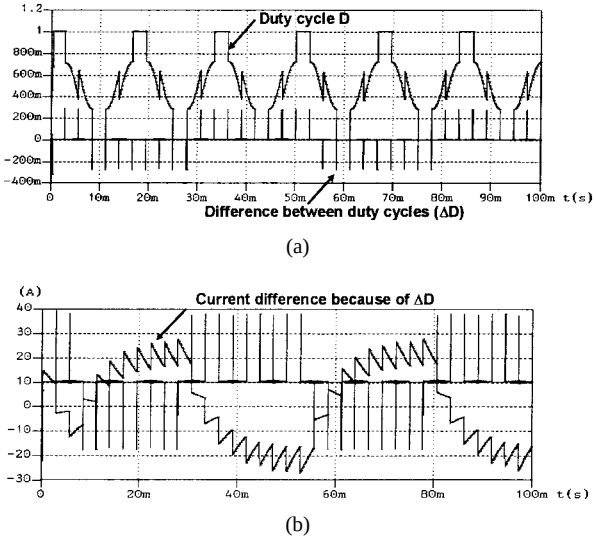

Fig. 9. Beat-frequency oscillation of the zero-sequence current.

first will use a different set of space vectors from the module behind it. This produces an effect of zero vector overlap in a very short period of time. When this is happening, the top switches of one module are connected to the positive dc rail and the bottom switches of the other module are connected to the negative dc rail. The three-phase currents will flow simultaneously from the dc bus capacitor through the top switches of one module, the boost inductors, the bottom switches of the other module, and back to the dc bus capacitor, as shown in Fig. 8. If the effective overlap time between the zero vectors is Δt, the dc bus voltage will be applied directly to the boost inductors. It produces the current

$$\Delta i_0 = \frac{V_{\rm dc}}{2L}\Delta t \tag{1}$$

where L is the inductance of the boost inductor.

This "shoottthrough" current charges and discharges the three-phase inductor simultaneously. One module picks up more current, while the other module drops off a current of the same magnitude. This current is the pure zero-sequence current, which does not show up in d and q channels with the transformation

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos(\theta-2\pi/3) & \cos(\theta+2\pi/3) \\ -\sin(\theta) & -\sin(\theta-2\pi/3) & -\sin(\theta+2\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \times \begin{bmatrix} i_a+\Delta i_0 \\ i_b+\Delta i_0 \\ i_c+\Delta i_0 \end{bmatrix}. \tag{2}$$

In the case of single-module operation, the zero vectors only serve as the freewheeling period when the three phases are tied together by conducting all the top or bottom switches. In the case of parallel module operation, however, the effect of the zero-vector overlap excites pure zero-sequence current to flow along the loops formed between the paralleled modules.

As the time elapses, at each 60° point of the line cycle, the reference vector will cross over the discontinuous points again and again in the hexagon. The reference vectors will not be synchronized to pass these points in a monotonic leading or lagging pattern. Instead, the line and switching frequencies modulate this pattern.

Assuming that the duty cycle of phase A of module 1 is D_{a1}, and the duty cycle of phase A of module 2 is D_{a2}, the difference between duty cycles will be ΔD_a in

$$\Delta D_a = D_{a1} - D_{a2}. \tag{3}$$

Fig. 9(a) shows the duty cycles and the difference between them. As can be seen, ΔD_a is modulated. Because of the duty-cycle modulation, the input current of the paralleled module is modulated also. The difference between phase A current of the paralleled modules is given by

$$\Delta i_a = i_{a1} - i_{a2}. \tag{4}$$

Fig. 9(b) shows relationships between ΔD_a and Δi_a. As indicated by this figure, at each 60° transition point, a current jump is produced. This jump results from the duty-cycle difference at the discontinuous points.

It is also interesting to note that within the continuous region of the SVM, the zero-sequence current does not stay at the previous values. This is because when the modules are in other combinations of vectors in the following switching cycle, the circulating currents still exist, but they are different in different phases. This process partly breaks up the pure zero-sequence current and translates a portion of it into dq channels. The dq current loops will try to correct this part of the current by tracking the given reference. As shown in Fig. 9(b), within the 60° range, as the zero-sequence current has not been corrected totally, the next excitation is produced again in the following transition. Therefore, there is a low-frequency component on the zero axis. Fig. 9(b) also gives the modulated pattern of ΔD, which is actually the same for all the phases. In this simulation, the line frequency is 60 Hz and the switching frequency is 20 kHz. The beat frequency is

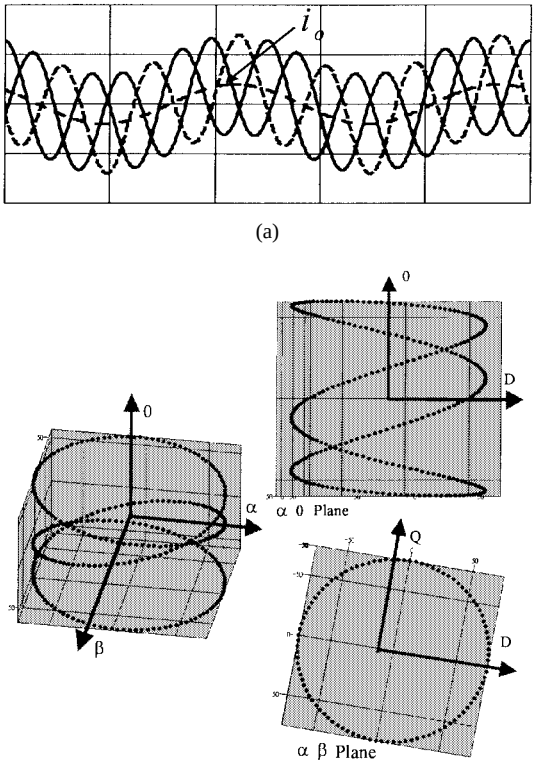

Fig. 10. (a) The effect of the pure zero-sequence current in time frame. (b) Three-dimensional (3-D) view of the three-phase current with a zero-sequence current in the rotating frame.

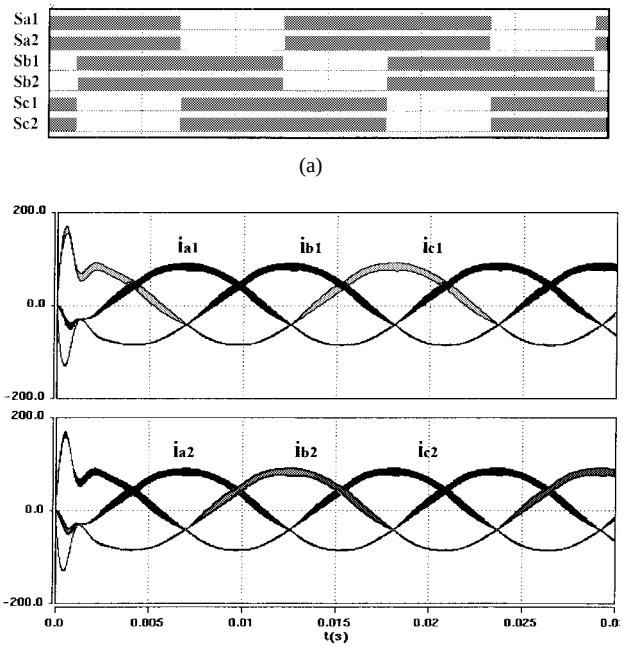

Fig. 11. (a) The gate signals of the top switches of the paralleled module with hysteresis control. (b) The three-phase input current of the paralleled module.

20 Hz. The mathematical derivation of the modulated patterns of the duty-cycle difference is provided in Appendix A.

Assuming there is a common mode current riding on a balanced three-phase current as shown in

$$\begin{aligned} i_a &= I\cos(\omega t) + \Delta i_a \\ i_b &= I\cos(\omega t - 2\pi/3) + \Delta i_b \\ i_c &= I\cos(\omega t + 2\pi/3) + \Delta i_c \end{aligned} \tag{5}$$

and

$$\Delta i_a = \Delta i_b = \Delta i_c = I_0 \cos\left(\frac{\omega}{3}t + \psi\right) = i_0. \tag{6}$$

In the time frame, the three-phase current is depicted in Fig. 10(a). By doing the transformation of

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \frac{2}{3} T \left(\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} i_0 \\ i_0 \\ i_0 \end{bmatrix} \right) \tag{7}$$

$$T = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{8}$$

where the three-phase current can be mapped into $\alpha\beta 0$ frame as shown in Fig. 10(b). The d and q components on the $\alpha\beta$ plane still rotate as a circle, but the zero-axis component oscillates up and down. In a balanced three-phase system, only two phases are independent because the sum of the voltage or current has to be zero. This is also true in the rotating coordinates. The controller can only control two of the three axes, usually d and q. Once such a pure zero-sequence current is injected into the system, the controller actually cannot see it because it is in an axis that is perpendicular to the dq plane.

III. Mitigation of the Circulating Current

To realize the zero-axis control, a third current sensor has to be inserted into the other phase of the module because the third phase current cannot be derived from the other two phases. With the sensed three-phase current, the $abc/dq0$ transformation is needed. The zero-axis hysteresis control method was tried first to solve the problem. The concept of the zero-axis hysteresis control is as follows. Before applying the zero vectors, the zero-axis current is compared with the given limits. If the current is greater than the upper limit, which means that more current is going into this module, then the *ppp* vector should be used in the following switching cycles in order to suppress the current. If the current is smaller than the lower limit, then the *nnn* vector should be used. If it is inside the window, the SVM should keep the previous zero vector.

There are two distinctive situations in which the zero-sequence current is produced. The first one is the so-called *ppp-nnn* vector overlap. The second one includes all other combinations of vectors, but not the pair of *ppp* and *nnn*. However, the hysteresis control cannot differentiate these two situations. Whenever it detects the three-phase current not adding up to zero, it will use the zero vectors to correct it. Apparently, the control cannot be accurate. Therefore, in the simulation, the *nnn* vector is used more frequently than the *ppp* vector. This means that bottom switches of the module will be used heavily.

Fig. 11 shows the simulation waveforms with Fig. 11(a) illustrating the gate signals for the top switches of the par-

alleled module and Fig. 11(b) the input current waveform of the paralleled module. As a result of the biased use of the switches, the input current is affected. The positive portion of the current has more ripples than the negative portion, as shown in Fig. 11(b). Therefore, this control strategy is not very desirable.

As we have noted earlier, the zero-sequence current produced at the discontinuous points does not hold at the same value in the following 60° period, but tends to return to the zero, which is seemingly in contradiction with the statement that the dq channel cannot reject the zero axis current. Actually, the current loops are doing their jobs. Assuming both reference vectors are in sector 1, where the pnn, ppn, and ppp vectors are used, within a switching cycle, there will be some time intervals when the two modules use different vectors. For example, one module is in the ppn vector, while the other is in either the pnn or ppp vector. Therefore, there will be a phase, either b or c, to participate in the current circulation, which breaks up the existing pure zero-sequence current and translates a portion of it into the d and q axes, where the d and q axes controllers can see them. Because of the intended PWM interleaving, the current circulation will not stop as long as the modules are not in the same vector. Therefore, it is impossible to make the sum of the three-phase current be zero at the switching frequency. The goal is to control its average value so that it does not accumulate.

Theoretically, the ppp and nnn vectors can be split apart and arranged appropriately in one switching cycle with other SVM schemes so that the effect of zero-vector overlap would be minimized or eliminated at the discontinuous point. Uncertainties, however, exist in system transients and sector transition, where transition chattering is likely to occur because of the current ripple. Once the overlap is created, the zero-sequence will exist in at least one switching cycle before it can be corrected. Because the current loop operates as a feed back loop based on the existing current to perform the following actions, it cannot be so fast as to eliminate the switching frequency current. Second, once the 60° clamping SVM is removed from the consideration, the switching losses for the rest of the SVM schemes become comparable to each other because of the similar commutation times in a switching cycle. Many different SVM's were simulated and analyzed, the SVM's that do not use zero vectors were proved the most viable solutions for interleaved PWM rectifiers. Fig. 12 shows one of the schemes with Fig. 12(a) illustrating the principle of the SVM and Fig. 12(b) the averaged duty cycles and the difference between them. As shown in this figure, the duty-cycle difference ΔD becomes smaller with this "continuous" SVM. The basic idea of this SVM is to divide the duty cycle of the zero vector into four equal periods of time and rearrange the duty cycles as the following:

$$\begin{aligned} d0' &= d0/2 \\ d1' &= d1 + d0/4 \\ d2' &= d2 + d0/4. \end{aligned} \tag{9}$$

In the $d0'$ period, the vectors that are opposite to the active ones are used to synthesize the zero vector as shown in Fig. 12(a).

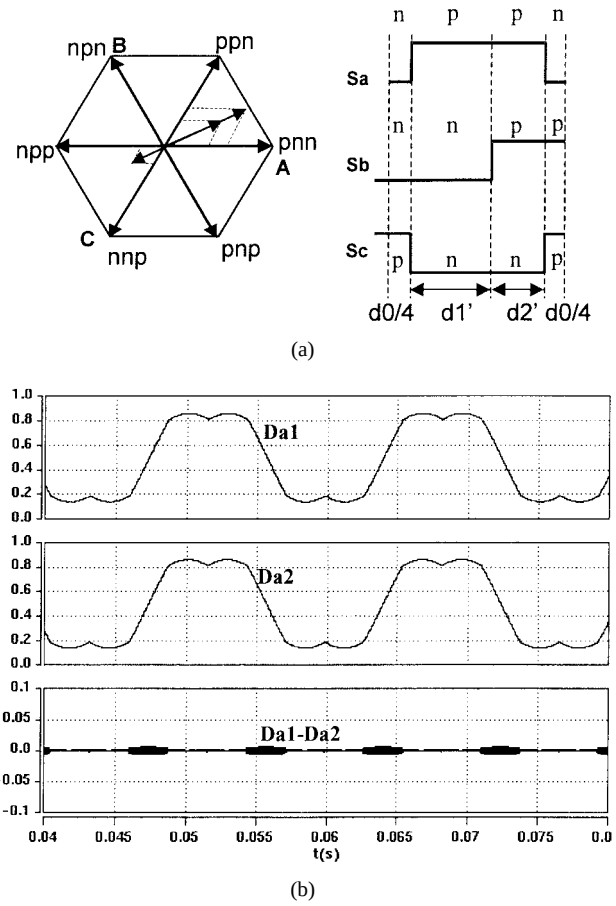

Fig. 12. (a) The proposed SVM for parallel operation without using zero vectors. (b) The averaged phase duty cycles and the difference between them.

By using this scheme, the zero-sequence current is cut off by two factors. First, there is no mechanism for producing the pure zero-sequence current by the zero-vector overlap as shown in Fig. 12(b). Even though the current circulation still exists, it takes place in a different manner. One phase may have more current, and other phases may have less current. Most importantly, this is a current that can be transformed into dq channels. Second, from each module's viewpoint, the undesired current resulting from the other modules can be treated as a disturbance to its own controller. If the circulating current is observable in the dq channel, the strong current loop will pick it up as a disturbance and reject it by modifying the output duty cycles in the following switching cycles. This is a dynamic process in which the current loops control the dq components to rotate as a circle. The high-bandwidth current loop exists naturally for PFC operations, where the controlled variables have to track the command as quickly as possible. Fig. 13 shows the simulated waveform of the input current of the two modules.

The use of this SVM involves more switching actions and a little higher current ripple. Because the change of modulation depth of SVM for PFC operation is very narrow, the ripple content is acceptable. The comparisons of the numbers of commutations and the ripple contents in the current between different SVM's mentioned in this paper are provided in Appendix B.

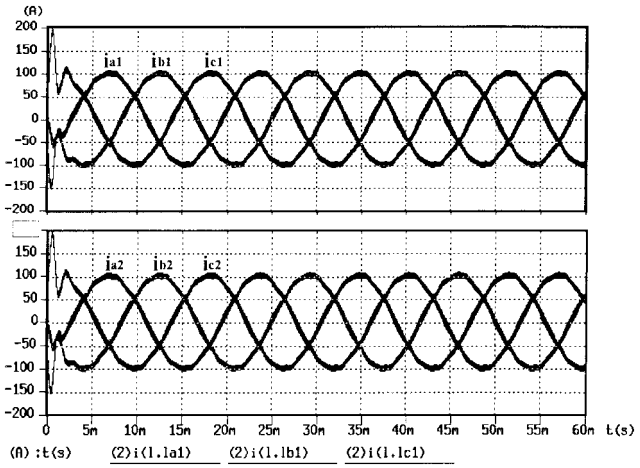

Fig. 13. Three-phase input current with the proposed SVM.

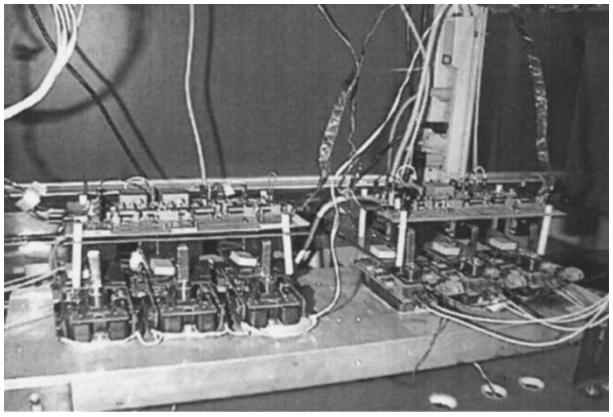

Fig. 14. Paralleled three-phase system based on the modular concept.

IV. Experiments

Currently, the Office of Naval Research (ONR) sponsors a variety of research on power electronics building blocks (PEBB's), a concept of using standardized modules to build distributed power systems [14]. One of the PEBB structures is a half-bridge power semiconductor device module integrated with gate drive and sensor. Three such PEBB's can be integrated further with other control intelligence to form three-phase modules. Although much of the research is in the packaging aspects, the conceptual PEBB structures were built to test the system control and integration issues. The objective of this research is to look for the control strategies for such a module so that once it is integrated into the module, it should allow the modules to "plug and play" with less communication. Fig. 14 shows the three-phase structure of the PEBB system. The bottom layer is the IGBT modules with the gate driver circuit. The gate drive uses optical fibers for signal transmission in order to eliminate the electromagnetic interference (EMI) coupling. The top layer is a sensor board that senses the phase current and voltage for closed loop operation. The dc terminals of the IGBT module are connected to a common laminated dc bus. The ac terminals of the paralleled IGBT modules are connected to a voltage source through current sharing reactors. Digital

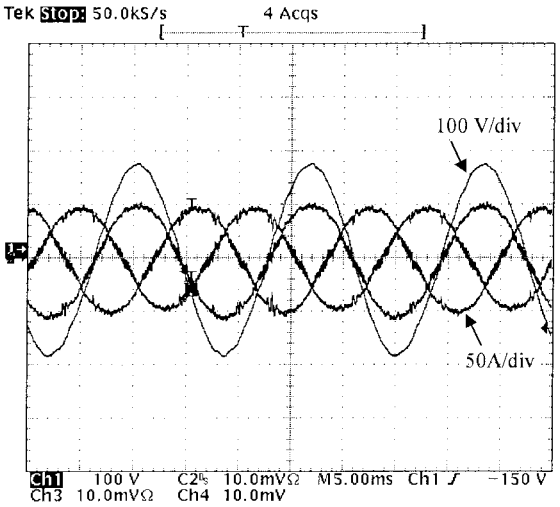

Fig. 15. Input voltage and current waveform in single-module operation.

signal processors (DSP's) are used to emulate the integrated intelligence in the module. The DSP serves as the current loop controller and SVM modulator. The common signals to each subsystem include the voltage loop output and the switching synchronization signal, both of which come from a motherboard.

The following are the system specifications and the hardware setup parameters.

Input voltage	3Φ, 208-V line-to-line.
Output voltage	400 V.
Single-module power rating	20 kVA.
Switching frequency	32 kHz.
IGBT module	Toshiba MG150J2YS50.
Input inductor	256 μH.
Output capacitor	1200 μF.
Current-sharing inductor	500 μH.
DSP	ADSP2101.

Because the inductance of the boost inductor is small, a relatively large current sharing inductor is used in the experiment in order to suppress the cross current ripple and generate a good current waveform. Fig. 15 shows the input current and voltage waveform at the 12-kW load condition for a single-module operation. The input current is in phase with the input voltage. Fig. 16 shows the input current of the paralleled modules with the proposed SVM. It can be seen that the currents on the same phase do not overlap each other exactly. They still have circulation current at switching frequency, but there is no noticeable low-frequency current oscillation. The combined input current is tested over 60 A. Figs. 17 and 18 show the effect of the interleaved switching signal on each module's input current and the total input current. The anticipated current ripple reduction is obtained. The irregularities at the ends of Fig. 18 are caused by the chattering effect of the SVM at the sector change.

V. Conclusion

In a balanced three-wire three-phase system—because the net current from the source or to the load has to be zero—there

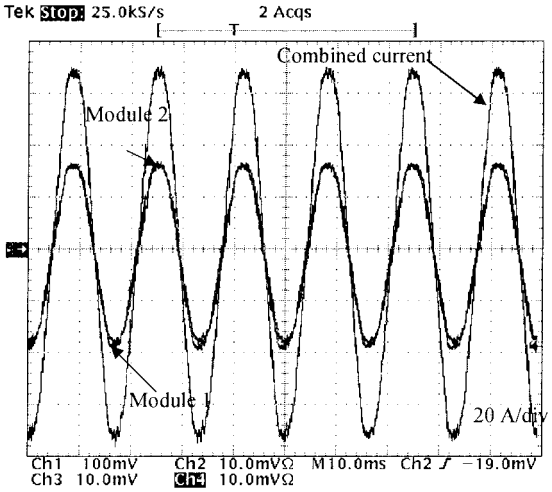

Fig. 16. Input current of the parallel modules and the total current in that phase.

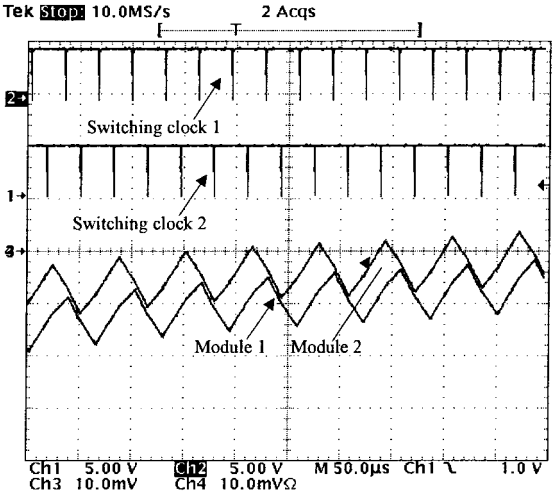

Fig. 17. Interleaved switching clock and the resulting current waveform.

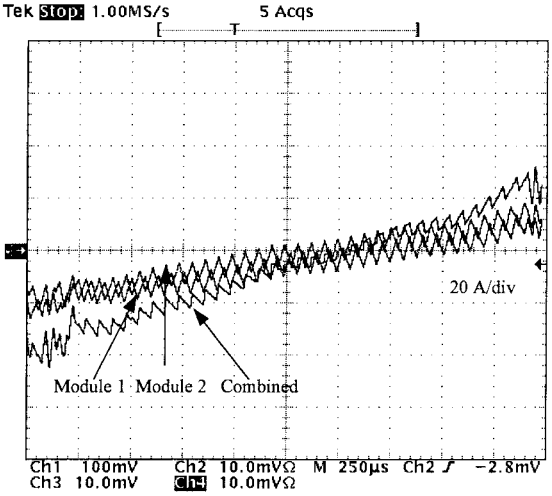

Fig. 18. Extended view of the current waveforms.

is no chance for zero-sequence current, even though there is a zero-sequence voltage induced by PWM modulations. Therefore, there is no concern about the third axis. When two or more modules are connected directly to a dc bus and a three-phase source/load without using transformer isolation, the intended PWM interleave will cause the current circulation in all the phases. Translated into rotating coordinates, the circulating current will show up on the zero axis, on which the dq current loop controller cannot help. This paper first introduces the 60° clamping SVM, which is very suitable for PFC operation for less switching loss. When it is used for parallel operation, there is an effect of zero-vector overlap at the discontinuous points caused by interleaving. This overlap will introduce the pure zero-sequence current into the system. This current has a beat frequency modulated by line and switching frequencies.

The current loop controller can have only two-dimension controls—the d and the q channels. In order to reduce the pure zero-sequence current on the zero axis using the existing current loops, several SVM's were simulated and analyzed. The SVM without using zero vectors is proven viable for parallel operation. With this SVM, there is still a circulating current at switching frequency on each phase, but this circulating current is observable to dq channels, which can be treated as the disturbance to other modules. The PFC module naturally has a high-current loop bandwidth, which tracks the given reference and rejects the high-frequency disturbance by modifying the duty cycles in the following switching cycles. This prevents the zero-sequence current from building up. The penalty of such a SVM is a little higher current ripple, which is tolerable.

The conceptual standardized power modules with integrated gate drive, signal sensing, and control intelligence are built for parallel operation. With the current loops closed, the proposed SVM shows the anticipated zero-axis current control and input current balance as well as the total current ripple cancellation.

APPENDIX

A. Calculation of the Modulated Pattern of the Zero-Sequence Duty Cycle with 180° Interleaved SVM

Parameters are given as follows.

$f = 60$ Hz	Line frequency.
$\omega = 2\pi f$	Angular line frequency.
$F_s = 20$ kHz	Switching frequency.
$T_s = 50$ μs	Switching period.
$tl = 25$ μs	Interleaving time shift.

Because the ppp and nnn vectors are used alternatively for 60°, index number i is used to count how many 60° have been passed on the time axis. $t(i)$ indicates the time instants of the 60° transition points.

Assuming that the three-phase current waveform and the switching clock of one module start at the zero point on the time axis. The switching clock of the other module shifts 25 μs. First, we have

$$t(i) = \frac{2\pi}{6\omega} = \frac{\pi}{3\omega}. \tag{A1}$$

The SVM transition from one 60° region to another is not exactly at the $t(i)$. It actually happens at the first switching

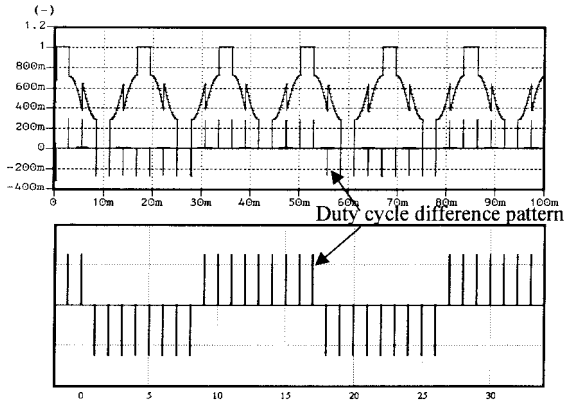

Fig. 19. The simulated and calculated the beat-frequency pattern.

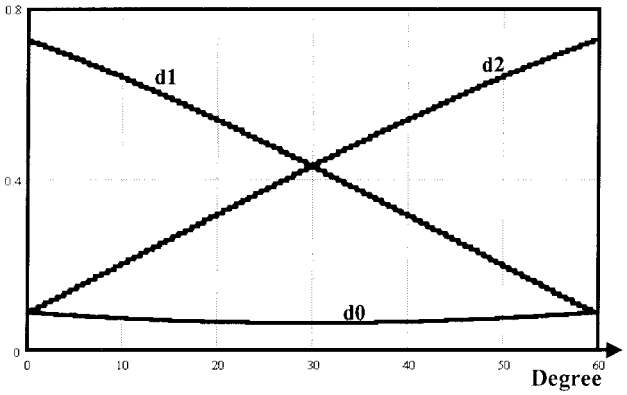

Fig. 20. Variations of duty cycles within one sector.

clock after $t(i)$. If we let TM1(i) to be the time instants for the SVM transition for the module 1 TM1(i) will be

$$\text{TM1}(i) = \text{ceil}\left(\frac{t(i)}{T_s}\right)T_s \tag{A2}$$

where $\text{ceil}(x)$ is a function to find the smallest integer greater than x. TM1(i) is the discontinuous point of the SVM for module 1. Similarly, for module 2

$$\text{TM2}(i) = \text{ceil}\left(\frac{t(i)-tl}{T_s}\right)T_s + tl. \tag{A3}$$

If TM1(i) is smaller than TM2(i), then it means that module 1 is passing the boundary of the ith discontinuous point earlier than module 2 and vice versa.

At the discontinuous point, the duty cycle jumps up and down alternatively at each transition, therefore, we define $\text{sign}(i) = (-1)^{i+1}$, which indicates the jumping direction of the SVM at the discontinuous point, where $\text{sign}(i) = 1$, jumping upwards, and $\text{sign}(i) = -1$, jumping downwards.

The zero-sequence duty-cycle pattern is then given by

$$T0(i) = \text{sign}(i)[\text{TM1}(i) - \text{TM2}(i)]. \tag{A4}$$

The comparison of the simulated and calculated beat-frequency pattern is shown in Fig. 19. The top waveform is obtained from the simulation and the bottom one from the calculation.

B. Comparison of the SVM's

The following takes sector 1 on the hexagon as an example. Other sectors can be obtained similarly because of symmetry. Sector 1 is the area between pnn and ppn vectors.

The magnitude of the space vectors is given by

$$\text{Vector} = \frac{V_{\text{dc}}}{\cos(\pi/6)}. \tag{A5}$$

The modulation index is defined as

$$dm = \frac{V_{\text{svm}}}{\text{Vector}} \tag{A6}$$

where V_{svm} is the desired line-to-line voltage, the reference vector length. Because the impedance of the inductor at line frequency is very low, a very small amount of voltage will produce a significant current capable of sustaining the dc bus voltage at certain load. Therefore, V_{svm} is almost equal to the input line-to-line voltage. At the 20-kVA power rating

$$dm = 0.637.$$

In each switching cycle, the projections of the reference vector onto pnn and ppn are given by

$$d1(\theta) = dm[\cos(\theta) - \sin(\theta)\tan(\pi/6)] \tag{A7}$$

$$d2(\theta) = dm\frac{\sin(\theta)}{\cos(\pi/6)}. \tag{A8}$$

The zero-vector duration is obtained by

$$d0(\theta) = 1 - d1 - d2 \tag{A9}$$

where θ is the angular position of the reference vector with regard to the pnn vector. Fig. 20 shows the variation of the $d1$, $d2$, and $d0$ within the sector.

Dividing one switching cycle into four segments with duty-ratio duration as $(d0/2)$, $d1$, $d2$, and $(d0/2)$ and letting k be the index number of the segments produce the equations from (A10) to (A11)

$$t_{k+1} = t_k + T_s \cdot DT_k \tag{A10}$$

$$\begin{aligned} ia_{k+1} &= ia_k + \frac{V_{\text{ph}}\sqrt{2}}{L}\int_{t_1}^{t_{k+1}} \cos(\omega t + \delta)dt \\ &\quad + \frac{V_{\text{dc}a_k}}{1.5L}(t_{k+1} - t_k) \\ ib_{k+1} &= ib_k + \frac{V_{\text{ph}}\sqrt{2}}{L}\int_{t_1}^{t_{k+1}} \cos(\omega t - 2\pi/3 + \delta)dt \\ &\quad + \frac{V_{\text{dc}b_k}}{1.5L}(t_{k+1} - t_k) \\ ic_{k+1} &= ic_k + \frac{V_{\text{ph}}\sqrt{2}}{L}\int_{t_1}^{t_{k+1}} \cos(\omega t - 2\pi/3 + \delta)dt \\ &\quad + \frac{V_{\text{dc}c_k}}{1.5L}(t_{k+1} - t_k). \end{aligned} \tag{A11}$$

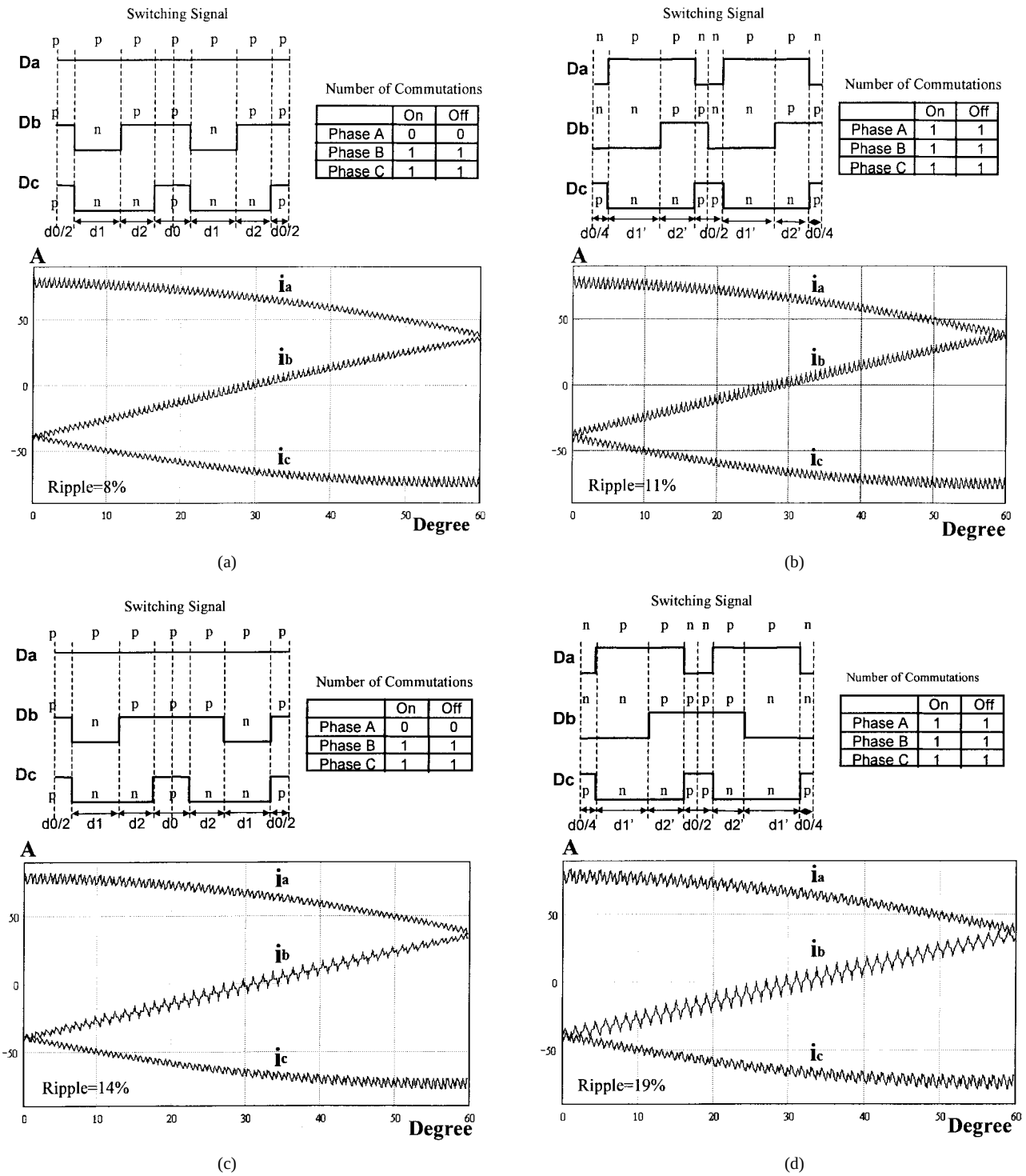

Fig. 21. The comparisons between SVM's in commutation times and current ripples. (a) and (b) Asymmetrical 60° clamping SVM and the SVM without using zero vectors. (c) and (d) Symmetrical operation.

In these expressions, we have the following.

t_k Time instant of the segments.
DT_k Duty cycle in each segment.
V_{ph} RMS value of the input phase voltage.
δ Phase delay between line voltage and the modulated voltage, which is very small.

In these equations, the phase current has three terms. The first term is the previous instant current value; the second is the inductor current contributed from the input voltage; and the third is the inductor current contributed from the dc bus voltage. In different segments within one switching cycle, the contributions from the dc bus voltage to the inductor current are different. Therefore, the nominators of the last term in (A11) have different values in each segment. Taking the 60° clamping SVM as an example, as shown in Fig. 21(a), $V_{\mathrm{dc}a}$, $V_{\mathrm{dc}b}$, and $V_{\mathrm{dc}c}$ are defined in the Table I. The physical meaning

TABLE I
THE VALUES OF $V_{\rm dc}$ IN DIFFERENT SEGMENTS OF 60° CLAMPING SVM

	d0/2	d1	d2	d0/2
Vdca	0	-Vdc	-Vdc/2	0
Vdcb	0	Vdc/2	-Vdc/2	0
Vdcc	0	Vdc/2	Vdc/2	0

TABLE II
THE VALUES OF $V_{\rm dc}$ IN DIFFERENT SEGMENTS OF THE PROPOSED SVM

	d0'/2	d1'	d2'	d0'/2
Vdca	Vdc/2	-Vdc	-Vdc/2	Vdc
Vdcb	Vdc/2	Vdc/2	-Vdc/2	-Vdc/2
Vdcc	-Vdc/2	Vdc/2	Vdc/2	-Vdc/2

of the first row of this table is the following. For phase A, in the $d0/2$ period, the zero vector is used and the dc bus voltage does not contribute to the inductor current. In the $d1$ period, the pnn vector is used. Phase A is connected the positive dc rail, and phase B and C are connected to the negative dc rail. Therefore, the phase A inductor current contributed by the dc bus voltage is

$$\Delta i_a = -\frac{V_{\rm dc}}{1.5L}(t_{k+1} - t_k) \tag{A12}$$

which is the last term in i_a for (A11). Similarly, in the $d2$ period of time, the ppn vector is used. The phase A inductor current contributed by dc bus voltage is

$$\Delta i_a = -\frac{V_{\rm dc}/2}{1.5L}(t_{k+2} - t_{k+1}) \tag{A13}$$

and in the following $d0/2$ period, the dc bus voltage does not contribute to the inductor current. The terms in Table I for phase B and C can be interpreted similarly.

For the SVM used in Section III, the duty cycles are recalculated as

$$\begin{aligned} d1'(\theta) &= d1(\theta) + \frac{d0(\theta)}{4} \\ d2'(\theta) &= d2(\theta) + \frac{d0(\theta)}{4} \\ d0'(\theta) &= \frac{d0(\theta)}{2}. \end{aligned} \tag{A14}$$

$V_{{\rm dc}a}$, $V_{{\rm dc}b}$, and $V_{\rm dcc}$ are defined as Table II in each segment. The current waveforms are calculated according the above formula. The comparisons between the 60° clamping SVM and the proposed SVM are shown in Fig. 21 from (a) to (d), where both the asymmetrical and symmetrical operations are studied.

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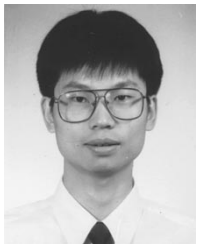
Dr. Boroyevich is a member of the IEEE Power Electronics Society AdCom, IEEE Industry Applications Society, and the Industrial Drives and Industrial Power Converter Committees. He is also a member of the Phi Kappa Phi honor society.



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