Design and experimental validation of a multiphase VRM controller

S.K. Mazumder and S.L. Kamisetty

Abstract: By combining the concepts of multiple-sliding-surface and integral-variable-structure controls, one can develop a robust controller for a multiphase 9 V VRM, which comprises four parallel DC–DC synchronous buck convertors operating at 300 kHz. The advantages of the control scheme are its simplicity in design, good dynamic response, robustness, ability to nullify the bus-voltage error and the error between the load currents of the convertor modules, and ability to reduce the impact of high-frequency dynamics due to parasitics on the closed-loop control system. Unlike a conventional variable-structure controller (VSC), which achieves superior transient performance by optimising (and hence, by varying) the switching frequency, the novel controller is able to retain the excellent dynamic performance of a conventional VSC and yet maintain a constant-frequency operation of a PWM controller under 'steady-state' condition. The latter is achieved by obtaining a duty-ratio signal; however, unlike a PWM controller, the new controller calculates the duty ratio based on Lyapunov's stability crietrion. Thus, the new controller also permits interleaved operation of the VRM modules.

1 Introduction

The power requirement for microprocessors doubles approximately every 36 months. Future power-delivery systems for microprocessors need to provide high currents at very low noise margins [1]. In addition, transient response specifications are also becoming more stringent. For instance, the design requirements specified by Intel for VRM 9.0 are shown in Table 1 [2]. Designing VRMs to meet this continually increasing power requirement at low voltages and high currents remains challenging. To achieve the specified transient-load response a single buck convertor would require a very high output-filter capacitance, which would increase the size of the VRM and make it impractical.

Paralleling a number of DC–DC synchronous-buck-convertor (SBC) modules (as shown in Fig. 1) using interleaving technique solves this problem [3, 4], thereby increasing the output ripple frequency and reducing the size of the output-filter capacitance. The multiphase VRM, comprising parallel DC–DC SBCs, operates under closed-loop feedback control to regulate the bus voltage and to achieve a uniform current distribution among the interleaved modules. The interaction among the convertor modules is a major source of nonlinearity, in addition to the switching nonlinearity. However, there are few studies on the nonlinear control of parallel DC–DC convertors where, unlike the stand-alone convertors, there is a strong interaction among the convertor modules apart from the feed-forward and feedback disturbances.

Table 1: VRM 9.0 design guidelines [2]

Electrical specifications	Intel VRM 9.0 design guidelines
Output voltage	1.408–1.5 V (our nominal reference: 1.45 *V*)
Output current	60 A
No-load operation	Outputs must not exceed 110% of the maximum value
Overshoot at turn-on or turn-off	Must be within 2% of the nominal output voltage set by VID code
Slew rate	50 A/μs
Current sharing	Should be accurate within 10% of the rated output current, except during initial power-up and transient responses

In [5], a fuzzy-logic compensator is proposed for the master–slave control of a parallel DC–DC convertor. The controller uses a proportional-integral-derivative (PID) expert to derive the fuzzy-inference rules; it shows improved robustness compared with linear controllers. However, the control design is purely heuristic and the stability of the overall system has not been proven. In [6], a VSC has been developed for a buck convertor using interleaving. However, the interleaving scheme works only for three parallel modules. Besides, that paper does not give any details regarding the existence and stability of the sliding manifolds.

In this paper, we implement a hybrid nonlinear controller for parallel SBCs and demonstrate experimentally that the steady-state and transient performances of the closed-loop parallel SBC satisfies Intel's VRM 9.0 design specifications (as shown in Table 1). The controller uses the concepts of

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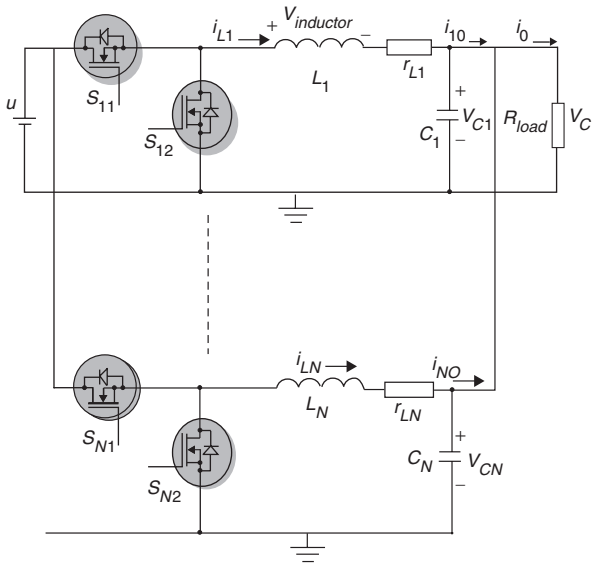


Fig. 1 *N-module multiphase VRM comprising N parallel SBCs*

integral-variable-structure- and multiple-sliding-surface-control (i.e. IVSC and MSSC) schemes [7]. The IVSC retains all of the properties of a VSC, i.e. simplicity in design, good dynamic response and robustness. In addition, the integral action of the IVSC eliminates the bus-voltage error and the error between the load currents of the convertor modules under steady-state conditions, and it reduces the impact of very high-frequency dynamics due to parasitics on the closed-loop system. Finally, when the error trajectories are inside the boundary layer we are able, by modifying the control using the concepts of MSSC [8, 9] or the block-control principle [10, 11], to reject mismatched disturbances [12, 13] and keep the steady-state switching frequency constant.

2 Nonlinear-control scheme

The control scheme for the convertor has two modes of operation: one when the error trajectories are outside the boundary layer and the other when they are inside the boundary layer. The block diagram of the overall control scheme is shown in Fig. 2 for N parallel SBC modules. The boundary layer, which is time-varying, is formed by a ramp signal with a frequency f_s $(=1/T_s)$. The limits of this boundary layer correspond to the maximum and minimum values of the ramp. At the beginning of each switching cycle, we determine whether the error trajectories (as shown in Fig. 3), which govern the regulation of the multiphase

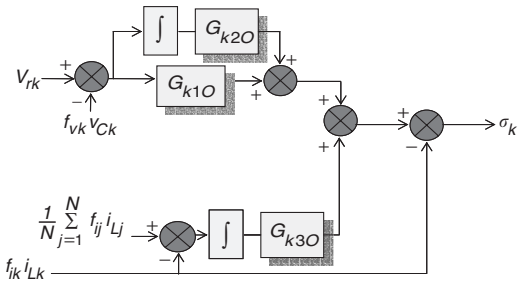


Fig. 3 *Block diagram showing the determination of* σ_k

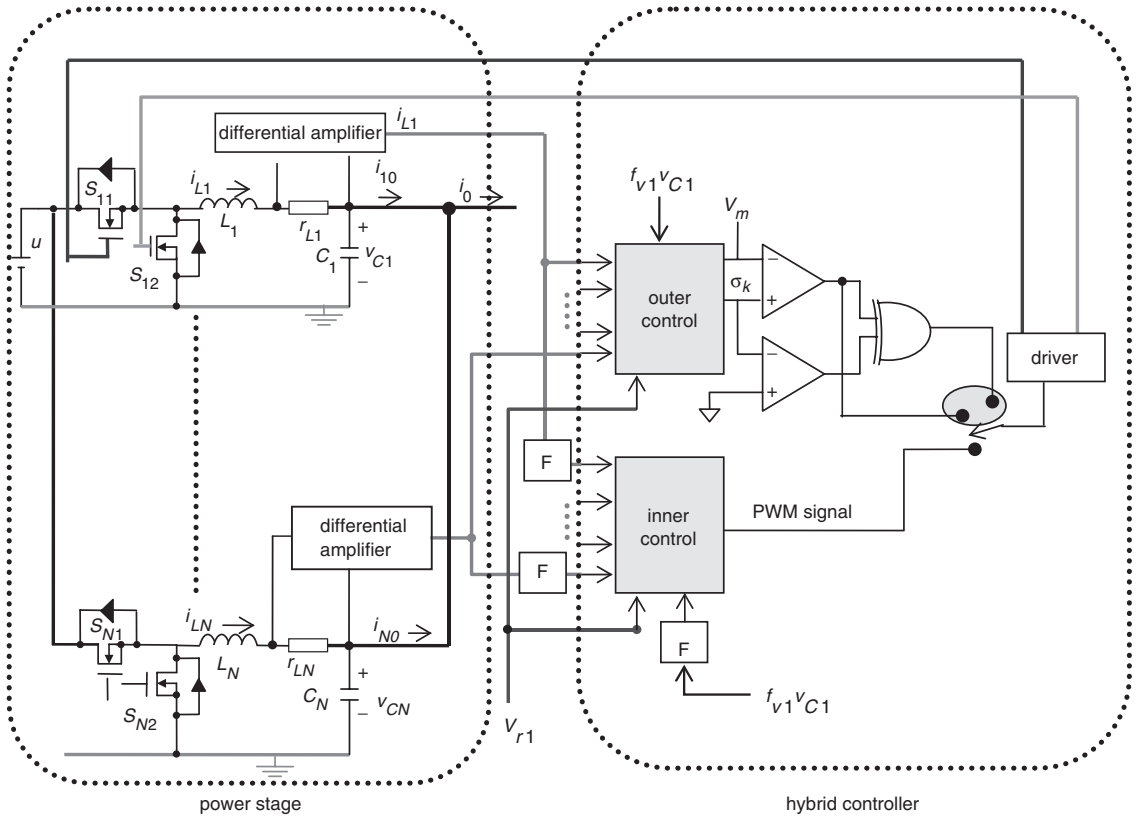


Fig. 2 *Illustration of the hybrid nonlinear control scheme for the 'first' SBC module of an N-module SBC*
The control schemes for the other $N-1$ modules are the same. The outer and inner controls are described in Section 2. The block 'F' represents a lowpass filter, which eliminates all harmonic components including and above the switching frequency. The block 'differential amplifier' represents a differential amplifier used to sense the inductor current

VRM and are given by

$$\sigma_k = G_{k1O}(V_r - f_{vk}v_{ck}) + G_{k2O}\int (V_{rk} - f_{vk}v_{ck})d\tau + G_{k3O}\int \left(\frac{1}{N}\sum_{j=1}^{N} f_{ij}i_{Lj} - f_{ik}i_{Lk}\right)d\tau - f_{ik}i_{Lk} \quad (1)$$

are within the limits of the time-varying ramp, and based on that, determine what is the mode of operation. In (1), the constants G_{k1O}, G_{k2O} and G_{k3O} are the controller gains (selection process described in [7]), f_{vk} and f_{ik} are the feedback-sensor gains for the output voltage and inductor currents, V_r is the reference of the output bus voltage, and $\frac{1}{N}\sum_{j=1}^{N} f_{ij}i_{Lj}$ represents the average of all inductor currents. The first two terms in (1) minimise voltage error while the third term ensures equal distribution of load current among the various modules. The last term improves the dynamic response of the system. The derivatives in a conventional VSC are replaced by integrals in (1). This is desirable because the integrators filter out the impacts of the high-frequency parasitic dynamics of the switching convertors. If σ_k is above the boundary, the control signal to the high-side switch of a SBC is a constant high while if it is below the boundary, the switch is turned off till the error trajectory falls within the boundary. The conditions under which control saturation outside the boundary layer guarantees that the error trajectories will reach the boundary layer are derived in [2, 7].

To derive the control law within the boundary layer, first, using Fig. 1 and a state–space-averaged model, we define the dynamics of the parallel DC–DC SBC as:

$$\frac{d\overline{i_{Lk}}}{dt} = -\frac{1}{L_k}\left(r_{Lk}\overline{i_{Lk}} + \overline{v_{Ck}} - d_k u\right)$$
$$\frac{d\overline{v_{Ck}}}{dt} = \frac{1}{C_k}\left(\overline{i_{Lk}} - \overline{i_{ko}}\right), \quad k = 1, 2 \ldots N \quad (2)$$

where, d_k is the duty ratio, $\overline{i_{Lk}}$ and $\overline{v_{Ck}}$ are the averaged values of the inductor currents and capacitor voltages, and i_{ko} are the load current of individual convertor. Next, we define the following sliding surfaces/error trajectories inside the boundary layer (computation of $\overline{\sigma_{1k}}$ and $\overline{\sigma_{2k}}$ illustrated in Fig. 4):

$$\overline{\sigma_{1k}} = G_{k1I}\overline{e_{1k}} + G_{k2I}\overline{e_{2k}} + G_{k3I}\overline{e_{3k}} \quad (3)$$

$$\overline{\sigma_{2k}} = \overline{i_{Lkd}} - \overline{i_{Lk}} \quad (4)$$

where

$$\overline{e_{1k}} = V_{rk} - f_{vk}\overline{v_{Ck}} \quad (5)$$

$$\overline{e_{2k}} = \int (V_{rk} - f_{vk}\overline{v_{Ck}})d\tau \quad (6)$$

$$\overline{e_{3k}} = \int \left(\frac{1}{N}\sum_{j=1}^{N} f_{ij}\overline{i_{Lj}} - f_{ik}\overline{i_{Lk}}\right)d\tau \quad (7)$$

G_{k1I}, G_{k2I} and G_{k3I} are the controller gains (selection process described in [7]). The sliding surfaces (3) and (4) are derived as follows. First, we define $\overline{\sigma_{1k}}$, which ensures regulation of the output voltage by incorporating the first two terms in (3), while the third term in (3) ensures equal current sharing among the parallel convertor modules. The sliding surface $\overline{\sigma_{2k}}$ ensures that the inductor current (i_{Lk}) of each module follows a desired current reference ($\overline{i_{Lkd}}$). The choice of $\overline{i_{Lkd}}$ in (11), is made such that stable convergence on the sliding surface $\overline{\sigma_{1k}}$ is guaranteed, as proven later in this Section. Stable convergence on the sliding surface $\overline{\sigma_{2k}}$ is achieved by appropriate selection of control d_k as derived in (17). Thus,

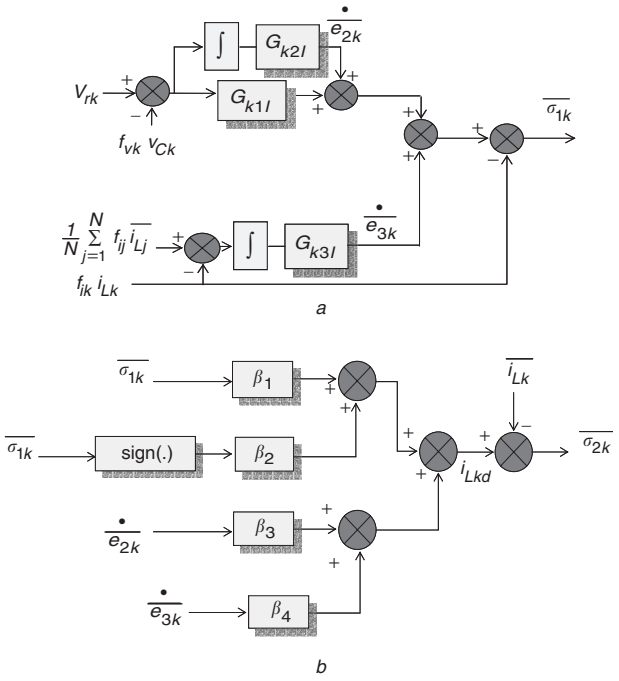


Fig. 4 *Block diagram showing the determination of σ_{1k} and σ_{2k}*
a σ_{1k}
b σ_{2k}

the overall control concept can be summarised as follows: first, guarantee rapid convergence of error trajectories on the sliding $\overline{\sigma_{2k}}$ using d_k (by suitable choice of α_{1k}), which ensures that $\overline{i_{Lkd}}$ is following i_{Lk} very closely; and then, using $\overline{i_{Lkd}}$ as a fictitious control, stabilise the error trajectories on the sliding surface $\overline{\sigma_{1k}}$.

We now derive $\overline{i_{Lkd}}$ and d_k that ensures existence and stability of the dynamics on the two sliding surfaces as well as the stability of the dynamics on the hyperplane formed by $\overline{\sigma_{1k}}$ and $\overline{\sigma_{2k}}$. First, we differentiate $\overline{\sigma_{1k}}$, to obtain

$$\dot{\overline{\sigma_{1k}}} = G_{k1I}\dot{\overline{e_{1k}}} + G_{k2I}\dot{\overline{e_{2k}}} + G_{k3I}\dot{\overline{e_{3k}}} \quad (8)$$

Substituting (2) in (8) yields

$$\dot{\overline{\sigma_{1k}}} = \frac{G_{k1I}f_{vk}}{C_k}\left(\overline{i_{Lk}} - \overline{i_{ko}}\right) + G_{k2I}\dot{\overline{e_{2k}}} + G_{k3I}\dot{\overline{e_{3k}}} \quad (9)$$

Substituting for $\overline{i_{Lk}}$ from (4) into (9) we obtain

$$\dot{\overline{\sigma_{1k}}} = \frac{G_{k1I}f_{vk}}{C_k}\left(\overline{i_{ko}} + \overline{\sigma_{2k}} - \overline{i_{Lkd}}\right) + G_{k2I}\dot{\overline{e_{2k}}} + G_{k3I}\dot{\overline{e_{3k}}} \quad (10)$$

We let

$$\overline{i_{Lkd}} = \beta_{1k}\overline{\sigma_{1k}} + \beta_{2k}\text{sign}(\overline{\sigma_{1k}}) + \beta_{3k}\dot{\overline{e_{2k}}} + \beta_{4k}\dot{\overline{e_{3k}}} \quad (11)$$

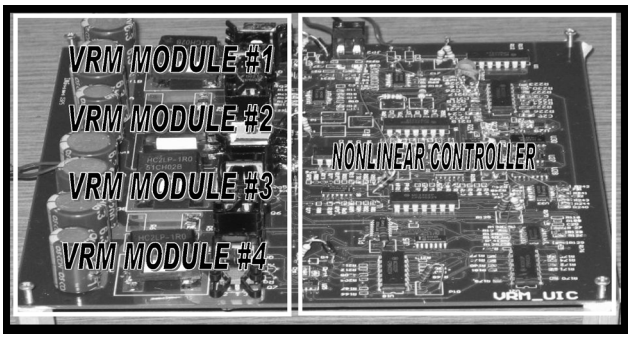


Fig. 5 *Top layer of the experimental prototype board*

where β_{1k}, β_{2k}, β_{3k} and β_{4k} are constants, in (11) and obtain

$$\dot{\overline{\sigma_{1k}}} = \frac{G_{k1I} f_{vk}}{C_k}\left(\beta_{1k}\overline{\sigma_{1k}} + \beta_{2k}\text{sign}(\overline{\sigma_{1k}}) - \overline{i_{ko}} - \overline{\sigma_{2k}}\right) - \left(\frac{G_{k1I} f_{vk}\beta_{3k}}{C_k} - G_{k2I}\right)\dot{\overline{e_{2k}}} - \left(\frac{G_{k1I} f_{vk}\beta_{4k}}{C_k} - G_{k3I}\right)\dot{\overline{e_{3k}}} \quad (12)$$

Choosing $\beta_{3k} = \frac{(C_k G_{k2I})}{(f_{vk} G_{k1I})}$ and $\beta_{4k} = \frac{(C_k G_{k2I})}{(f_{vk} G_{k1I})}$ reduces (12) to

$$\dot{\overline{\sigma_{1k}}} = \frac{G_{k1I} f_{vk}}{C_k}\left(\beta_{1k}\overline{\sigma_{1k}} + \beta_{2k}\text{sign}(\overline{\sigma_{1k}}) - \overline{i_{ko}} - \overline{\sigma_{2k}}\right) \quad (13)$$

Equation (13) shows that, when $\overline{\sigma_{2k}} = 0$, the dynamics on $\overline{\sigma_{1k}} = 0$ are convergent (for $\overline{\sigma_k} > 0$, or $\overline{\sigma_{1k}} < 0$) provided that $\beta_{2k} > \overline{i_{k\text{Omax}}}$. We assume that $\overline{\sigma_{2k}} = 0$ and design the control such that the rate of convergence of dynamics on $\overline{\sigma_{2k}} = 0$ are much faster than on $\overline{\sigma_{1k}} = 0$.

Next, we differentiate $\overline{\sigma_{2k}}$ in (4) and set it equal to $-\frac{\sigma_{1k}}{L_k}\overline{\sigma_{2k}}$ (where α_{1k} are positive constants) to guarantee convergence of the dynamics on $\overline{\sigma_{2k}} = 0$ (this is because, for stability, $\overline{\sigma_{2k}}\,\dot{\overline{\sigma_{2k}}} < 0$ and this condition is guaranteed by the choice of $\dot{\overline{\sigma_{2k}}}$ in (14)); the result is

$$\dot{\overline{\sigma_{2k}}} = \dot{\overline{i_{L_{kd}}}} - \dot{\overline{i_{Lk}}} = \dot{\overline{i_{L_{kd}}}} + \frac{r_{Lk}}{L_k}\overline{i_{Lk}} + \frac{1}{L_k}\overline{v_{Ck}} - \frac{1}{L_k}d_k u = -\frac{\alpha_{1k}}{L_k}\overline{\sigma_{2k}} \quad (14)$$

Next, using the Lyapunov function

$$V(\overline{\sigma_{1k}}, \overline{\sigma_{2k}}) = \frac{1}{2}\left(\overline{\sigma_{1k}}^2 + \overline{\sigma_{2k}}^2\right) \quad (15)$$

and (13) and (14), we can show that

$$\begin{aligned}\dot{V} &= \overline{\sigma_{1k}}\,\dot{\overline{\sigma_{1k}}} + \overline{\sigma_{2k}}\,\dot{\overline{\sigma_{2k}}} \\ &= \sigma_{1k}\left[-\frac{G_{k1I} f_{vk}}{C_k}\{\beta_{1k}\overline{\sigma_{1k}} + \beta_{2k}\text{sign}(\overline{\sigma_{1k}}) - i_{ko} - \overline{\sigma_{2k}}\}\right] \\ &+ \overline{\sigma_{2k}}\left(\frac{\alpha_{1k}}{L_k}\overline{\sigma_{2k}}\right) \le -\left(\frac{G_{k1I} f_{vk}}{C_k}\beta_{1k}\overline{\sigma_{1k}}^2 + \frac{\alpha_{1k}}{L_k}\overline{\sigma_{2k}}^2\right) \\ &+ \frac{G_{k1I} f_{vk}}{C_k}\overline{\sigma_{1k}}\,\overline{\sigma_{2k}} = -\left\{\sqrt{\left(\frac{G_{k1I} f_{vk}}{C_k}\beta_{1k}\right)}\overline{\sigma_{1k}} \right. \\ &\left. -\frac{1}{2}\sqrt{\left(\frac{G_{k1I} f_{vk}}{C_k\beta_{1k}}\right)}\overline{\sigma_{2k}}\right\}^2 - \left(\frac{\alpha_{1k}}{L_k} - \frac{1}{4}\frac{G_{k1I} f_{vk}}{C_k\beta_{1k}}\right)\overline{\sigma_{2k}}^2 \end{aligned} \quad (16)$$

is less than zero provided that

$$\frac{(\alpha_{1k} C_k \beta_{1k})}{L_k G_{kI1} f_{vk}} > \frac{1}{4}$$

From (14), by equating $\dot{\overline{i_{L_{kd}}}} + \frac{r_{Lk}}{L_k}\overline{i_{Lk}} + \frac{1}{L_k}\overline{v_{Ck}} - \frac{1}{L_k}d_k u = -\frac{\alpha_{1k}}{L_k}\overline{\sigma_{2k}}$ we obtain

$$d_k = \frac{1}{u}\left(\alpha_{1k}\overline{\sigma_{2k}} + L_k\dot{\overline{i_{L_{kd}}}} + r_{Lk}\overline{i_{Lk}} + \overline{v_{Ck}}\right) \quad (17)$$

which ensures that, for the above choice of control d_k, the stability of the sliding surface $\overline{\sigma_{2k}}$ is guaranteed. We also note that, in (17), the term $\alpha_{1k}\overline{\sigma_{2k}}$ compensates for any parametric uncertainty in r_{Lk}. (Typically, such variations due to manufacturing tolerances are within 5%.) For instance, if r_{Lk} is slightly higher than its nominal value, then a slightly higher $\overline{i_{Lk}}$ is required to regulate the output voltage at the reference value. This compensation is achieved (due to slight adjustment in d_k) owing to slight variation in $\overline{\sigma_{2k}}$ that depends on $\overline{i_{Lkd}}$, which in turn depends on $\overline{\sigma_{1k}}$; the latter accounts for error in the output voltage. Using the error signal v_{ek}, which is obtained from the duty ratio d_k using $v_{ek} = V_m d_k$, and the fixed-frequency ramp signals, we can operate N parallel DC–DC SBCs in synchroncity or in interleaving.

3 Experimental results

Figures 5 and 6 show the experimental prototype of the overall multiphase VRM and the circuitry for one power module, respectively. The experimental printed-circuit board (PCB) has four layers to reduce the impact of noise and enable operation at a high switching frequency. The parameters for the VRM are tabulated in Table 2, while the control specifications are outlined in Table 1. The VRM comprises four phases of the power stage (i.e. parallel DC–DC SBCs) and the nonlinear controller, outlined in Section 2, using analogue circuits. The complete details of the experimental VRM implementation are provided in [2].

The four modules of the VRM operate at 300 kHz and are interleaved. The interleaving technique is implemented by phase shifting the drive signals of the paralleled modules by $360^\circ/N$, where N is the number of parallel SBCs. Because we have four modules, we have phase-shifted the drive signals by a quarter of a switching cycle. This is ratified in Fig. 7, which shows the gate signals of the high- and low-side power MOSFETs (FDP6035L and FDP8030L, respectively), under steady-state conditions.

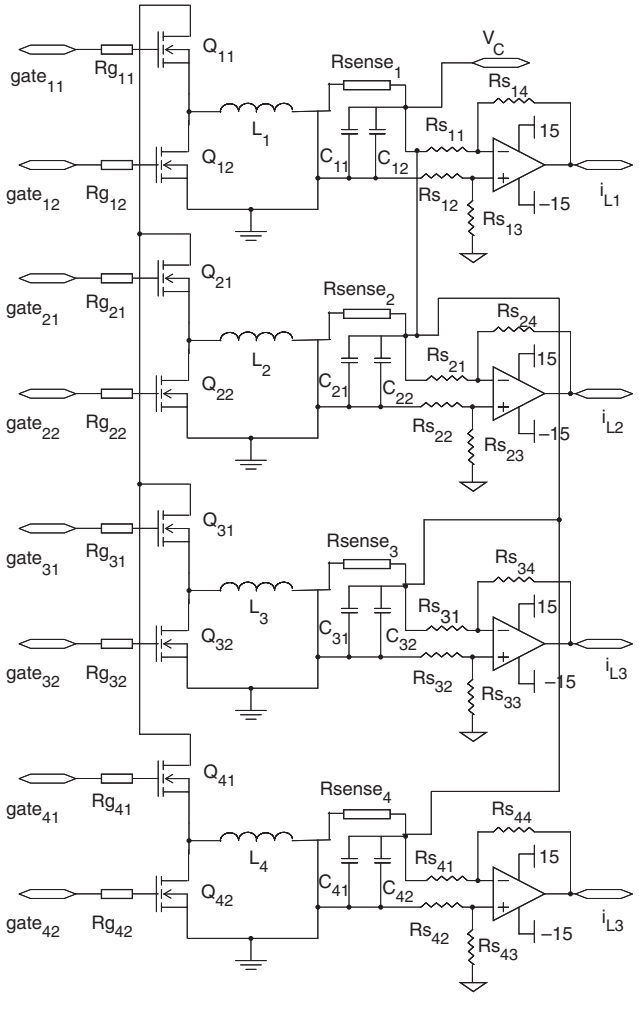
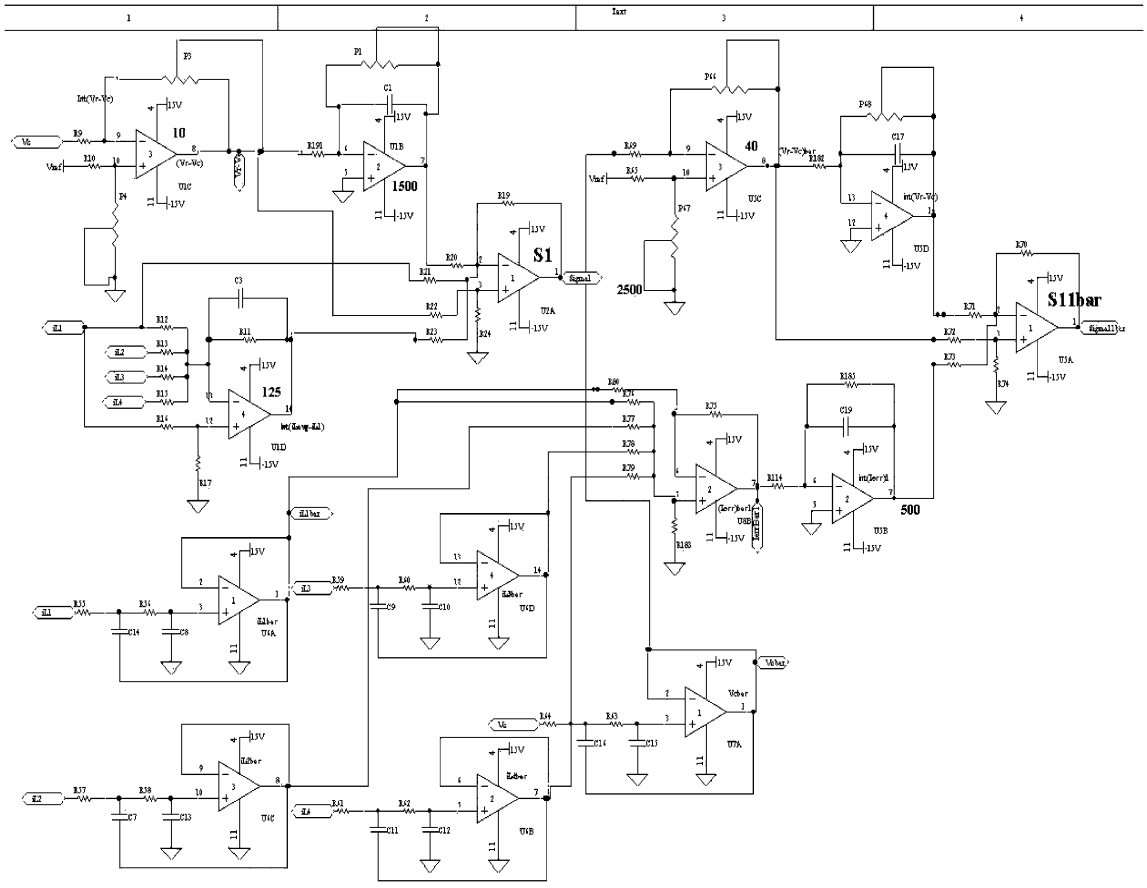
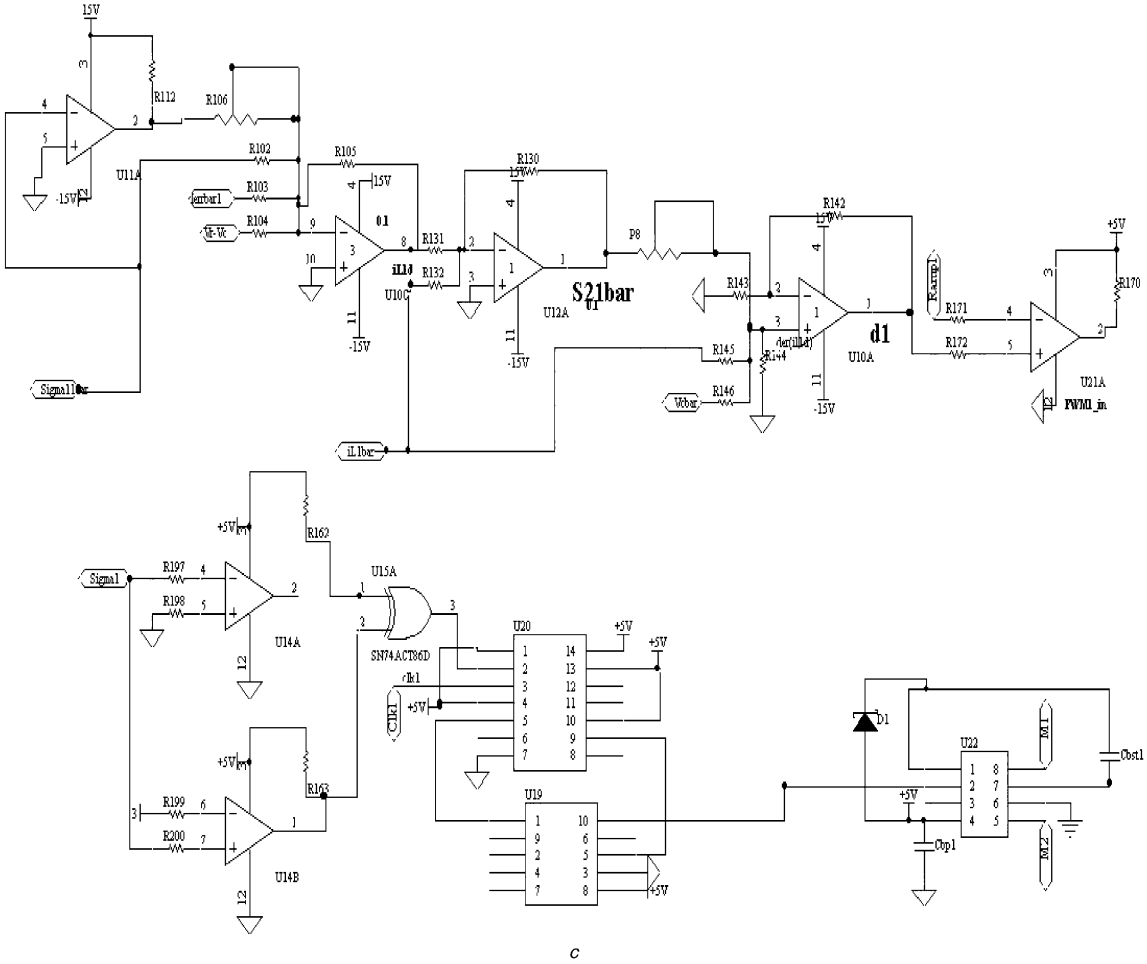


Fig. 6 *Schematics of the nonlinear controller for one phase of the four-phase VRM [2] shown in Figs. 3 and 4a. In (b), S1 represents σ_1, S11 bar and S2 bar represent $\overline{\sigma}_{11}$ and $\overline{\sigma}_{21}$, respectively*



b



c

Fig. 6 *Continued*

Table 2: Nominal parameters for the four-phase VRM

Parameter	Nominal value
r_{DS} (on) of MOSFET	0.0056 Ω
r_{Lk}	0.024 Ω
L_k	1 μH
C_k	2200 μF
V_r	1.45 V
U	12 V
f_{ik}	0.02
f_{vk}	1
Switching frequency	300 kHz
DC offset of the ramps	1.5 V
Height of the ramps	3.0 V
G_{k1O}	5
G_{k2O}	1.5×10^5
G_{k3O}	500
G_{k1I}	10
G_{k2I}	1.5×10^5
G_{k3I}	500

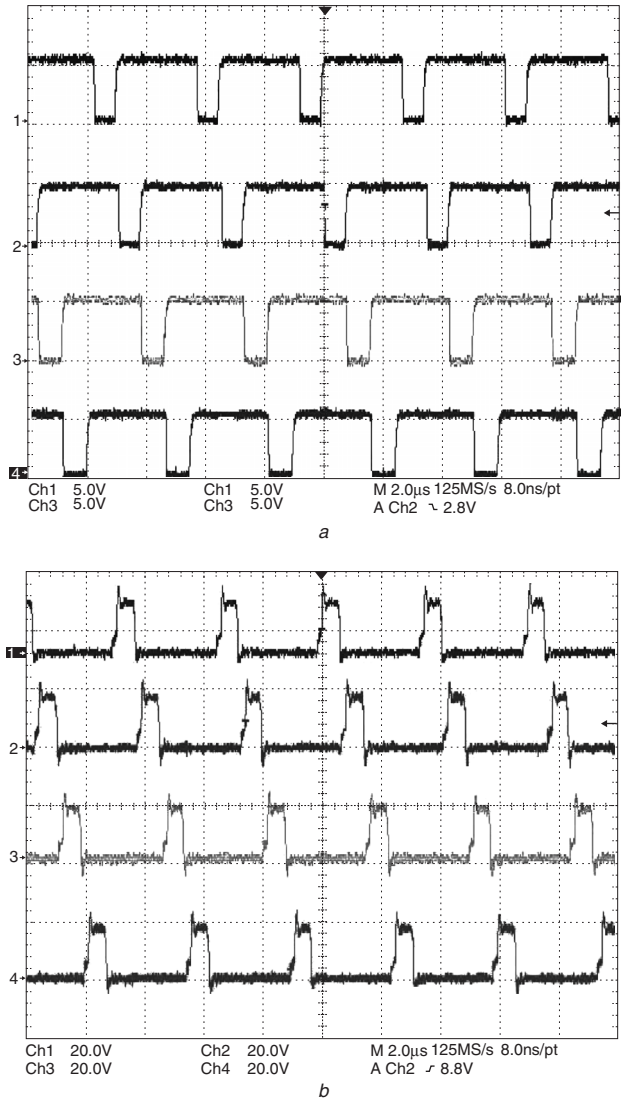


Fig. 7 *Gate signals of the four VRM modules*
a Low-side power MOSFETs
b High-side power MOSFETs

Figure 8 shows the output voltages and the inductor currents of the four modules of the VRM, under steady-state conditions. The four inductor currents are interleaved, i.e. they differ in phase by 90°. The high-side switches in the four modules of the VRM are turned on at time intervals that are a quarter of a switching-time period apart from each other. Therefore, the inductor currents do not rise and fall at the same time, but, are phase shifted by a quarter of a switching cycle.

Figure 9 shows the load current and the output voltage of the VRM during a step-down load transient of 60 A to 20 A at a slew rate of 50 A/μs. During the severe load transient, the output voltage stays within the 2% limit, as specified by Intel VRM specifications in Table 1. The inductor currents of the four phases also respond satisfactorily and maintain an even distribution of the load current among the modules during the transient conditions. The performance of the VRM remains excellent even during a step-up load transient of 20 A to 60 A (at a slew rate of 50 A/μs). This is illustrated in Fig. 10. Once again, the output voltage satisfied the Intel VRM specifications and the current sharing was maintained

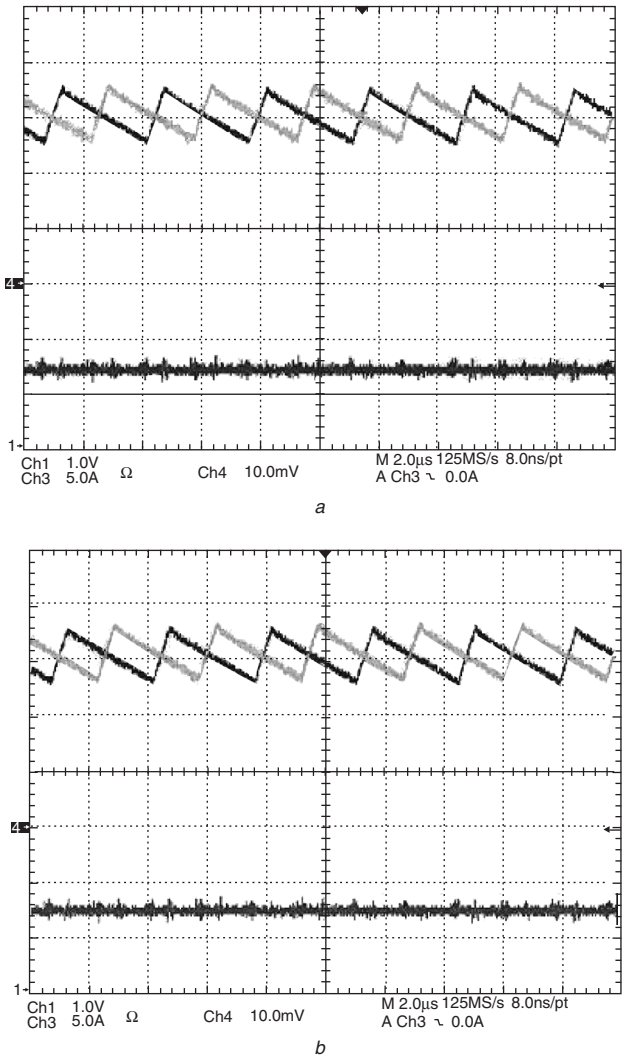


Fig. 8 *Interleaved inductor currents in the four modules of the VRM and the output voltage*
Currently the project has access to only two current amplifiers, so only two current waveforms can be recorded at once; this applies also to Figs. 9–12
a Inductor currents (5 A/division) for modules 1 and 3
b Inductor currents (5 A/division) for modules 2 and 4

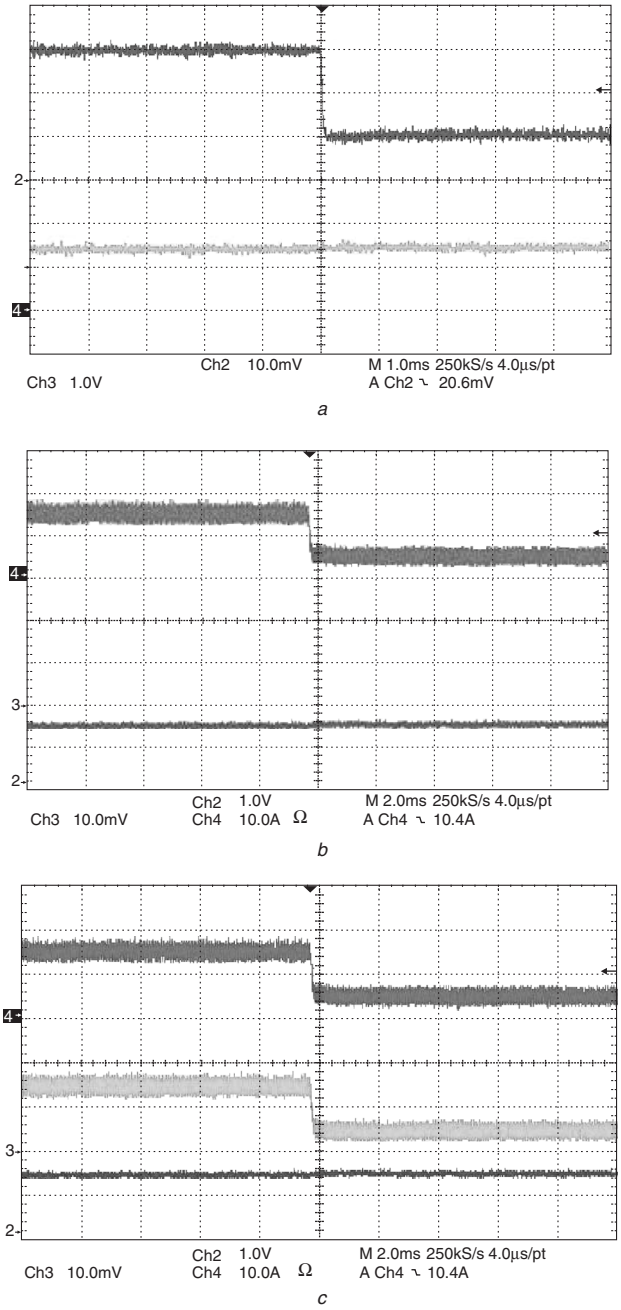


Fig. 9 *Performance of the VRM during a step-up load transient*
a Load current (20 A/division) and output voltage of the VRM
b VRM output voltage and the inductor currents (10 A/division) of modules 1 and 3
c VRM output voltage and the inductor currents (10 A/division) of modules 2 and 4

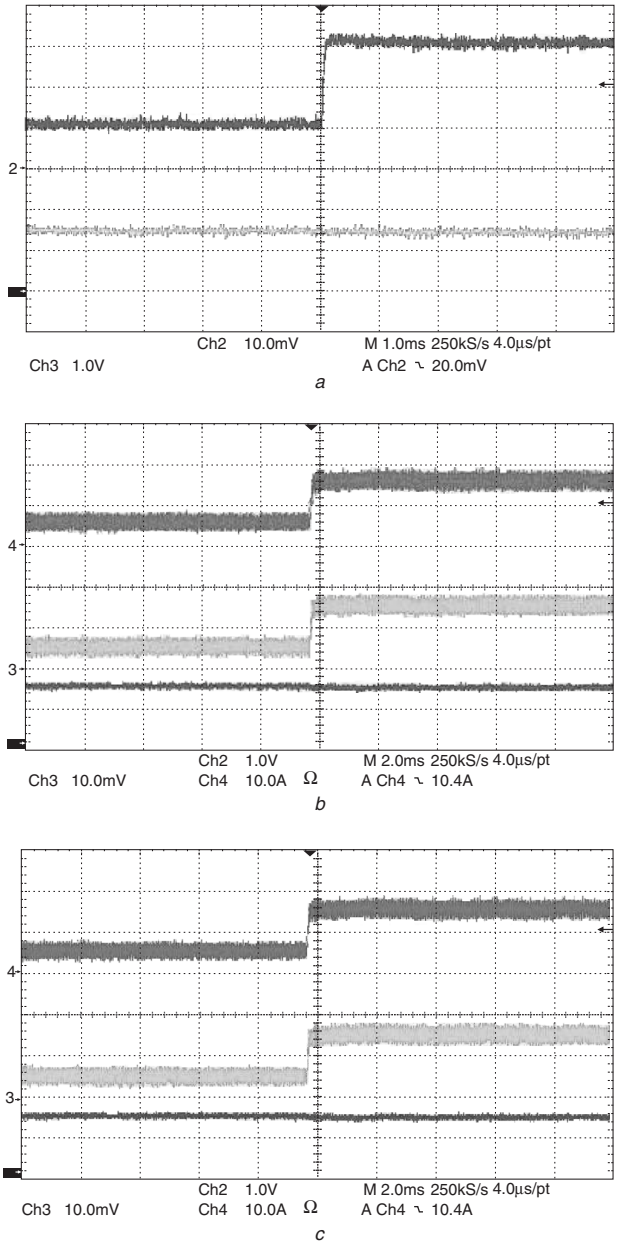


Fig. 10 *Performance of the VRM during a step-down load transient*
a Load current (20 A/division) and output voltage of the VRM
b VRM output voltage and the inductor currents (10 A/division) of modules 1 and 3
c VRM output voltage and the inductor currents (10 A/division) of modules 2 and 4

during the dynamic condition in spite of a rapid change in the load. Finally, Figs. 11 and 12 show the error-trajectory waveforms σ_{1k} and σ_{2k} during the load transients.

4 Summary and conclusions

Using the concepts of integral-variable-structure and multiple-sliding-surface controls (i.e. IVSC and MSSC), we have implemented a robust nonlinear controller for a four-phase VRM, operating at 300 kHz. The power stage of each phase comprises a synchronous buck convertor, the input to all of which is 12 V; the output voltage of the VRM is set at 1.45 V. We demonstrate the excellent performances of the multiphase VRM under steady-state and severe dynamic conditions. The controller is able to retain the 'transient' performance of a conventional sliding-mode/min–max controller (SMC/MMC) and yet maintain a constant-frequency operation of a PWM controller under 'steady-state' conditions. The latter are achieved by obtaining a duty-ratio signal; however, unlike a conventional PWM controller, the new controller calculates the duty ratio based on Lyapunov's stability criterion. The robust controller nullifies the bus-voltage and the load-current errors, exhibits good current sharing under steady-state and dynamic conditions, and, by using IVSC (which uses integrators in the control instead of the differentiators in a conventional SMC/MMC), filters out any impacts of the high-frequency parasitic dynamics in the system. An added advantage of

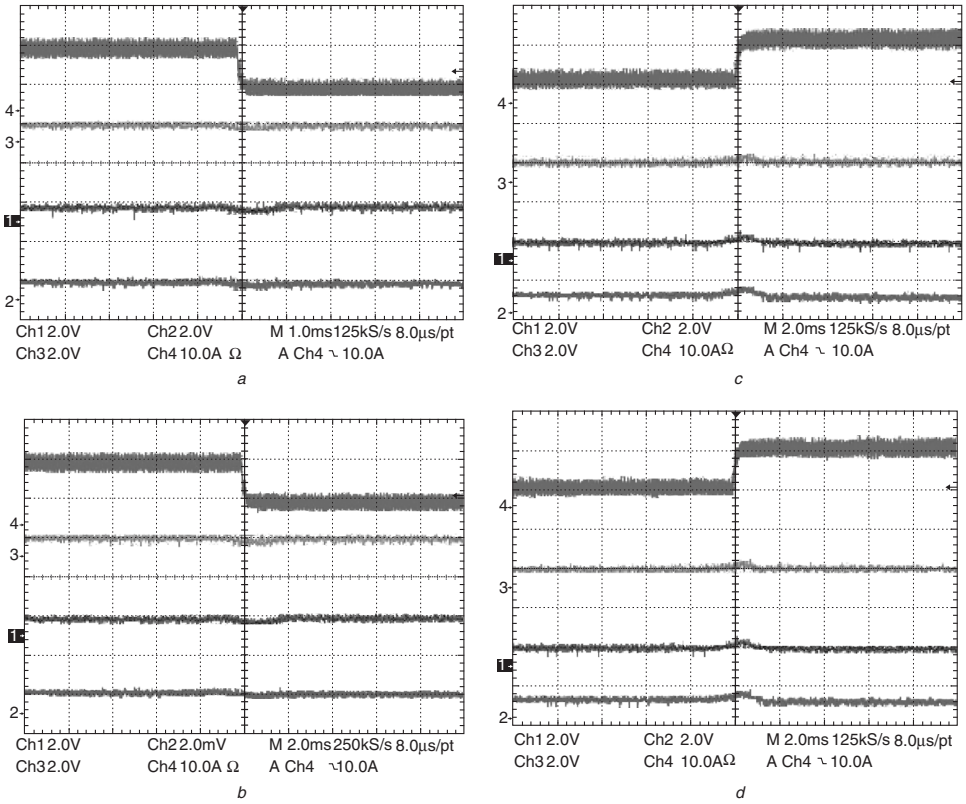


Fig. 11 *Inductor current for module 1 and error signals (σ_{1k}) for SBC modules 1–4 during step-down and step-up load transients*
Top trace: inductor current
a Step-down, experimental results for SBC modules 1 and 3
b Step-down, experimental results for SBC modules 2 and 4
c Step-up, experimental results for SBC modules 1 and 3
d Step-up, experimental results for SBC modules 2 and 4

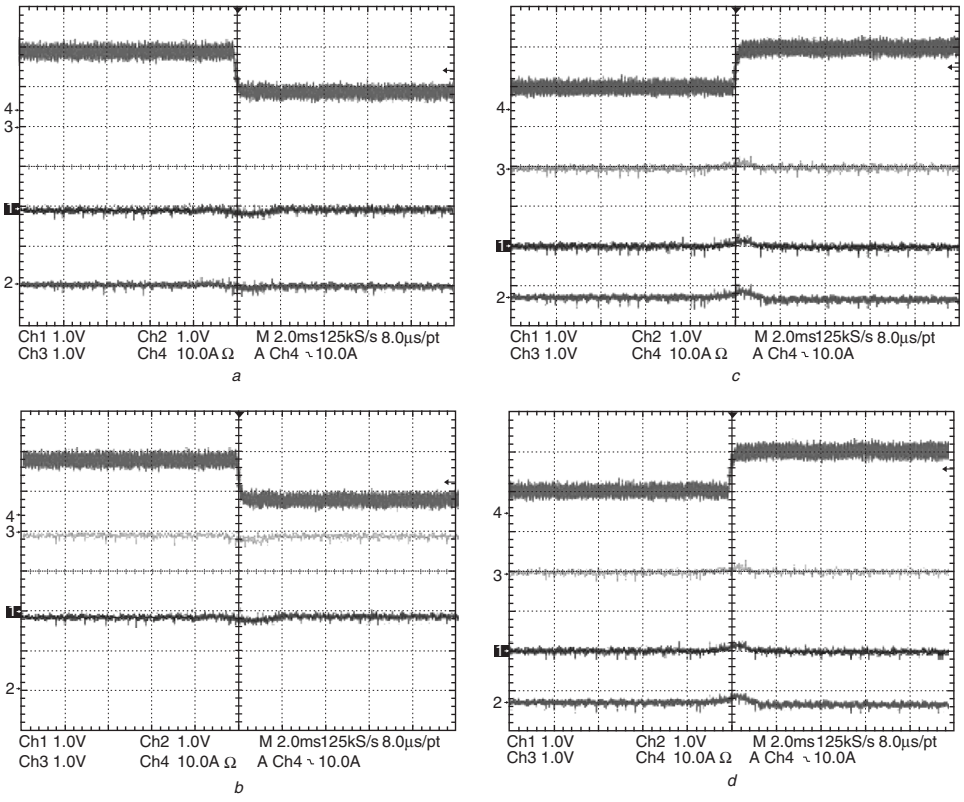


Fig. 12 *Inductor current for module 1 and error signals (σ_{2k}) for SBC modules 1–4*
Top trace: inductor current
a Step-down, experimental results for SBC modules 1 and 3
b Step-down, experimental results for SBC modules 2 and 4
c Step-up, experimental results for SBC modules 1 and 3
d Step-up, experimental results for SBC modules 2 and 4

the control is that it enables the modules to be interleaved which reduces the output-capacitor size and makes the whole system more compact.

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