Evaluation of first 10-kV optical ETO thyristor operating without any low-voltage control bias

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***Abstract*—In this paper a new single-biased all-optically triggered ETO configuration is proposed. For this purpose, an optically triggered power transistor with vertical structure is used as a power switch to help the main thyristor achieving a unity gain turn-off. In order to handle all-optical control, two different laser sources with a wavelength of 808 nm for the high power optical switch and a wavelength of 250 nm for the integrated thyristor are used to trigger them. Our simulation results show a good transition between on and off states with a rise and fall times of 26 ns and 362 ns. The total on-state voltage across the ETO is 4.4 V which is about 0.04% of the total supply voltage. The effect of parasitic inductances and the temperature on the output characteristics of the ETO is investigated separately.**

Keywords—Emitter turn-off (ETO), thyristor, optically triggered power transistor (OTPT), silicon carbide

I. INTRODUCTION

In recent years the environment in which power semiconductor devices must operate has become more and more extreme. Devices must now be able to switch faster, with higher applied bias, and with increased junction and ambient temperatures. To facilitate these extreme applications, SiC devices have been used, and have been shown to be very effective in high voltage applications. In order to achieve switching at such high voltages (> 5 kV), the thyristor device structure has been used with a reasonable on-state voltages, due to its bipolar nature. The major drawback of the thyristor is the inherent latching action of the 4-layer device, making it difficult to switch off once the device is conducting. This has been overcome in a variety of ways including forcing the anode current to zero and supplying a turn-off current to the gate of the thyristor. Auxiliary low-voltage devices to aid in the turn-off can assist in achieving the latter, and in this paper the Emitter Turn Off (ETO) configuration [1]-[3], shown in Fig. 1, is used. All integrated devices are optically excited; creating a robust power device that can be used for increased frequency and very high voltages. To operate the device, the integrated thyristor and auxiliary switch Q1 are excited at the same time, turning the device on. When Q1 is turned off, Q2 is switched on by building a voltage across Q1, turning the thyristor off in unity turn off [4]-[6] by the self-gated. The parasitic inductors shown in Fig. 1 have important effects on the transient turn-off procedure which will be discussed in the simulation results section.

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The gain of the thyristor is among the highest of all semiconductor devices, making it ideal for low power optical excitation. Optical activation has many benefits in power semiconductor devices. This allows a decrease in Electro-Magnetic Interface (EMI) disruptions in the gating signal of the power devices and allows the removal of the gate drive circuitry from the harsh environment that the power device must operate. It also reduces complexity of the drive circuitry as the bias voltage does not need to be stepped down to a suitable level for the device drivers. Optical devices can be used to drive standard power MOSFETs and IGBTs [7],[8] but required a second low voltage bias.

The outlined all-optical ETO configuration allows for a single bias, high voltage power device that can operate at elevated temperatures. In this paper, numerical analysis of the optical ETO, which requires no low-voltage control bias unlike any existing ETO (or even IGCT/MTO/GTO devices) is reported at 10 kV using the Silvaco TCAD suite. Transient results, including parasitic inductance, are given after a brief introduction to the integrated devices in the optical ETO.

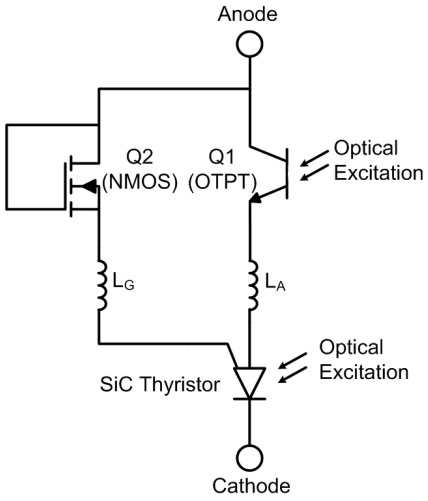

Fig. 1. Structure of the hybrid all-optical ETO.

II. INTEGRATED ALL-OPTICAL THYRISTOR

The integrated thyristor that was simulated is based on Cree's 10-kV thyristor structure outlined in [9]. The structure simulated is shown in Fig. 2(a). This device is driven by a 250

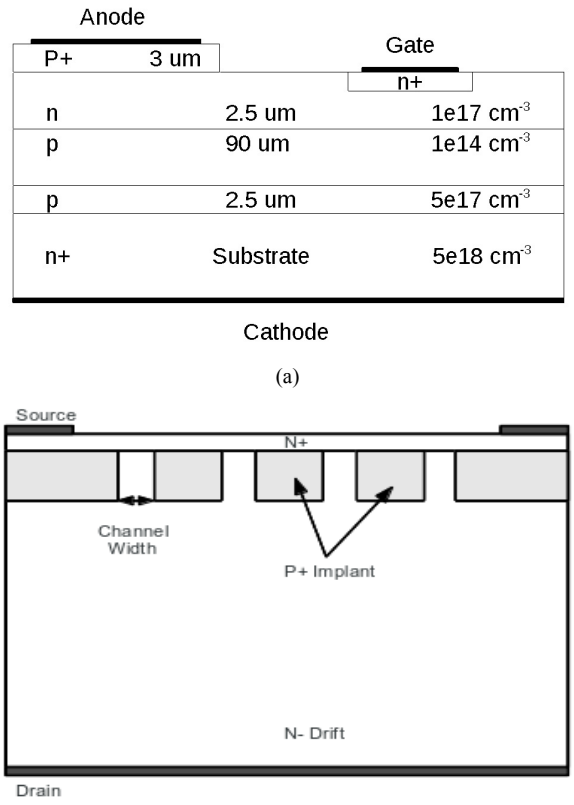

Fig. 2. (a) Optical thyristor structure, (b) Optically-triggered power transistor (OTPT) structure.

nm optical source. The thickness and doping concentration of the thick epitaxial drift layer are some of the most important factors in fabricating SiC thyristors. To achieve higher breakdown voltages, a thicker drift layer with lower doping concentration is required. Today, a thickness of more than 100 um has been achieved for the epitaxial layer by CREE Inc. They managed to decrease the drift layer doping concentration down to less than 2×10^{14} cm^{-3} [9]. With these improvements, a breakdown voltage of more than 12 kV can be achieved for SiC thyristors.

For our new all-optical ETO configuration, a new optical power device has been developed that is able to conduct a larger amount of current than previous optical power devices demonstrated [10]. To increase the gain, static induction transistor (SIT) technology was used. Fig. 2(b) shows the normally-off, bipolar-mode FET (BMFET) [11] like structure that was chosen for this device. This type of device has been demonstrated for high current and medium voltage applications, and has been tested under optical excitation [12]. This device improves on previous BMFET devices by introducing a continuous top N+ layer requiring contacts only on the edges of the device, minimizing area shadowed from the light. This increases the gain of the device while also leading to a simpler mask design.

This structure allows for the gain of the device to be indirectly related to the light intensity that is being applied. In this device, the incident light changes the electric field in the channel, essentially creating a light controlled JFET-like device. The device has shown in simulation an optical gain of >3 A/W in saturation with an excitation of 808 nm light. Due the JFET-like nature of the device, it is convenient to create an inherently paralleled multichannel device on a single die. With a large area and a cellular approach, many more channels than were simulated will be present, increasing the gain and saturation current.

This new optical device operates in series with the integrated thyristor, and therefore must be able to handle the full load current. The optical BMFET is able to operate under these conditions with a low drain to source voltage drop due to a wide channel area. A very low voltage drop must be achieved to decrease the loss experienced by the entire device, and to prevent the destruction of the switch.

III. Simulation Results

Numerical study of the optical ETO was performed with an applied bias of 10 kV, and a load current of 10 A. Physics based structure models were used for the thyristor and the series optical device and compact SPICE model was used for the MOSFET. A transient analysis was done to see the rise and fall times of the ETO under different differing conditions, such as parasitic inductances and temperatures. As a basis for comparison, a simulation at room temperature and with no parasitic inductances was performed.

Studying the transient responses of such high power devices can be computationally difficult, and very time consuming. In order to perform this work, it was necessary to find a manner in which the simulation could be done within a conventional amount of time. It was found that one way to drastically reduce the time taken in the simulation was to avoid solving for initial conditions at a extremely high bias. By applying the turn-on input signals to the devices at the beginning of the simulation, the intial solution is that at low voltages and the simuations can be run in sigificantly lower amounts of time.

These results are shown in Fig. 3. A thyristor voltage rise and fall time of 26 ns and 362 ns is recorded. The on-state voltage drop of the OTPT was 0.15 V and the voltage drop across the thyristor was 4.2 V, leading to the total voltage drop of 4.4 V. This is roughly about 0.04% of the supply voltage. In the off state, a peak voltage of 5 V was applied to the OTPT, while at steady state a voltage of 2 V was applied, which is 0.02% of the total voltage. The current waveforms are shown in Figure 4. It can be seen that the anode current is commutated to the gate, and that the turn off-delay is the combination of the fall time of the anode current and the period that the gate is conducting. The fall time of the gate corresponds to the fall time of the cathode.

A. Effect of parasitic Inductances

This device structure was also tested with different parasitic inductance (L_A and L_G in Fig. 1). The most important packaging parasitics in this type of device are small inductances in the path of the gate and the anode. These are caused by the package interconnects between the devices and should be kept to a minimum. This non-ideality is observed as a voltage build-up across the OTPT during turn-off, but during

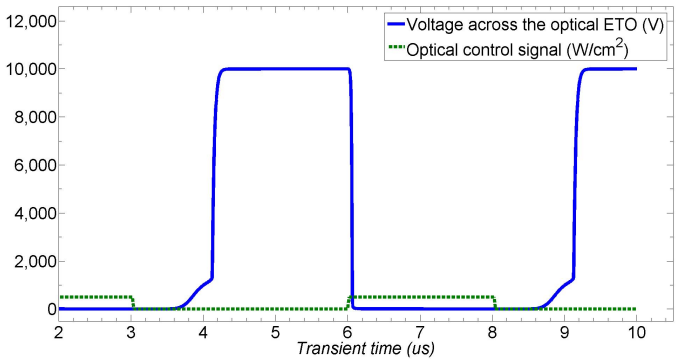

Fig. 3. Voltage across the optical ETO.

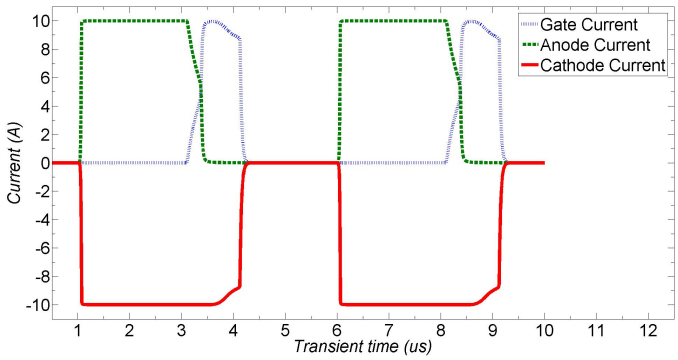

Fig. 4. Currents in the optical ETO.

turn-on no significant over-voltage on the OTPT is observed. If the value of this inductance is too large, then the OTPT will experience an unnecessarily large voltage, forcing the use of a much large device. Numerical tests for an inductance value of 100 nH placed in series with the gate, in series with the anode, and in series with both were performed. These results are shown in Fig. 5. A peak voltage across the OTPT of 54 V was observed when there are inductances in both paths, while this voltage drop is about 5 V without any parasitic inductances.

Larger parasitic inductances or an increased di/dt result in a higher peak voltage dropped across the OTPT during the turn-off procedure. This effect is shown in Fig. 6. Based on these results, the breakdown voltage of the OTPT should be chosen to be more than about 60 V in the worst case. For the OTPT simulated in this paper, a breakdown voltage of 72 V is achieved for the structure in shown Fig. 2 with a channel width of 600 nm and an epitaxial layer thickness of 25 µm.

Power losses in switch Q2 or the NMOS transistor during thyristor turn-on procedure is another issue when parasitics are introduced. This loss is originated from the leakage current in the gate path when a voltage greater than the NMOS threshold voltage is built up due to the Ldi/dt inductance voltage. This causes the gate path to conduct current for a short period of time when the thyristor is switched on. The higher the parasitic inductances are, the higher this leakage current is. In Fig. 7, the transient power loss in terms of the gate leakage current versus transient time is shown for two cases, with and without parasitic inductances. Without parasitic inductances, there is no gate leakage current during turn-on. But when the parasitics are

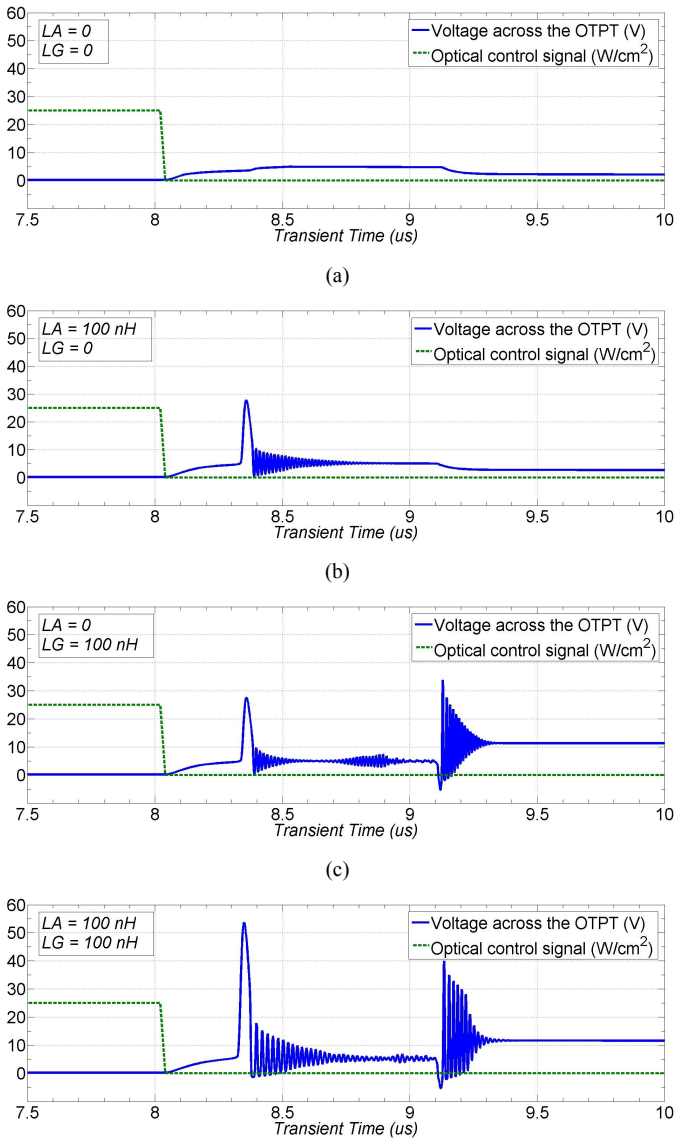

Fig. 5. Voltage across the OTPT with (a) no parasitic inductors, (b) inductor in series with anode, (c) inductor in series with gate, and (d) inductors in series with anode and gate.

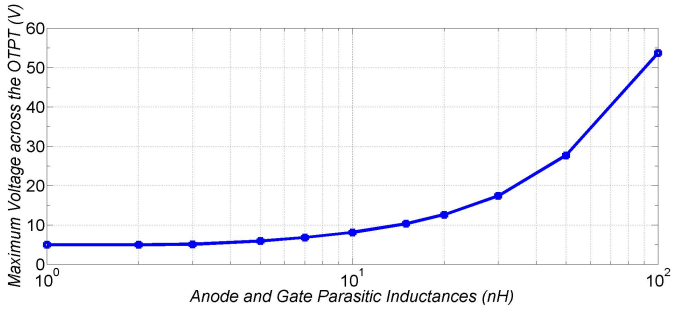

Fig. 6. Maximum voltage drop across the OTPT vs. parasitic inductances.

introduced, the gate current continues to increase as long as the anode current is increasing, providing the Ldi/dt voltage across the anode parasitic inductor. When the cathode current reaches

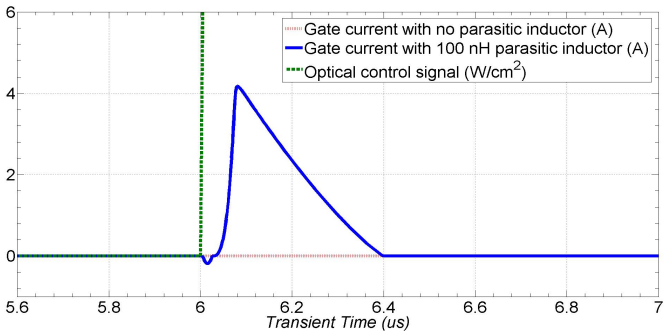

Fig. 7. Gate current during the turn-on procedure with and without parasitic inductances.

its final value, the term di/dt will vanish and cause the gate current to reduce to zero. With parasitic inductor of 100 nH, a current with a peak of about 4 A (40 % of the total load current) is passed through the gate within about 400 ns. The peak power is 27 W and the total dissipated energy is 5.4 µJ.

B. Effect of Temperature

Power devices must be able to operate under increased temperatures. This optical ETO was numerically tested under a range of temperatures from 300 K to 480 K. At temperatures greater than 480 K, the device failed to show any desirable characteristics. The voltage rise and fall times of the device structure as well as the thyristor voltage drop at the on-state were calculated. The rise and fall times slightly varied with temperature. By increasing the temperature, the rise time is increased a little while the fall time is reduced. The rise time at 300 K was found to be 26 ns and at 480 K to be 33 ns. The fall time varied more, being 362 ns at 300 K and 323 ns at 450 K. Another parameter which varied with the temperature is the fall time delay, which is defined as the time between the moment when the optical excitation is removed to the time when the load current reaches the 95% of its maximum value i.e. 9.5 A. An increase of about 150 ns for the fall time delay is observed by increasing the temperature from 300 to 480 K. In general, an increased temperature greatly increased the delay experienced by the total device structure. The other significant variation came in the thyristor on-state voltage drop being 4.2 V at 300 K and 5.6 at 480 K. These results are plotted in Figs. 8 and 9.

IV. CONCLUSIONS

Numerical analyses of a 10 kV optical ETO are presented in this paper. The results show that a single bias optically excited device structure can obtain rise and fall times that make it a good choice for high frequency and high voltage next generation power conversion. A strong resistance to inductive parasitics was found. With anode and gate parasitic inductances of 100 nH, a peak voltage of about 54 V is dropped on the axillary series low-voltage OTPT device.

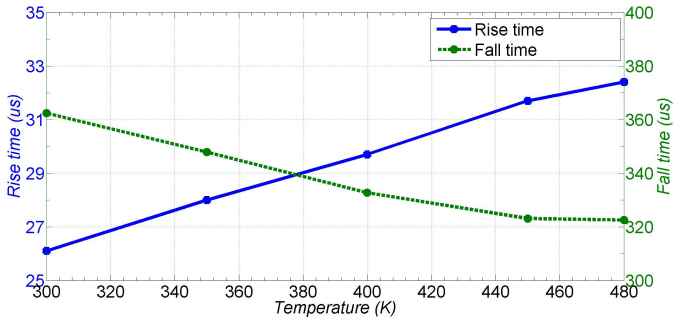

Fig. 8. Delay times of the optical ETO.

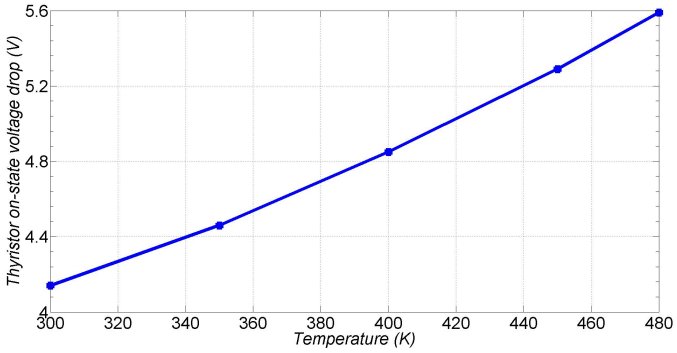

Fig. 9. Variation of the thyristor on-state voltage with temperature.

References

[1] Y. Li, A. Huang, and K. Motto, "Experimental and numerical study of the emitter turn-off thyristor (ETO)," IEEE Transactions on Power Electronics, vol. 15, no. 3, pp. 561-574, May 2000.

[2] J. Wang, G. Wang, J. Li, and A. Huang, "Silicon carbide emitter turn-off thyristor, A promising technology for high voltage and high frequency applications," Applied Power Electronics Conference and Exposition, Twenty-Fourth Annual IEEE, pp. 658-664, Feb. 2009.

[3] S.K. Mazumder, "Photonically activated single bias fast switching integrated thyristor," U.S. Patent Appl. No. 13/281,207, filed in Oct. 2011.

[4] Y. Li, A. Huang, and F.C. Lee, "Introducing the emitter turn-off thyristor (ETO)," Industry Applications Conference, vol. 2, pp. 860-864, Oct. 1998.

[5] Y. Li, A. Huang, K. Motto, and A.Z. Xu, "Introducing the emitter turn-off thyristor (ETO). Numerical and experimental demonstration of unity turn-off gain capability," Power Electronics Congress, pp. 2-9, Oct. 1998.

[6] J. Wang and A. Huang, "Design and characterization of high-voltage silicon carbide emitter turn-off thyristor," IEEE Transactions on Power Electronics, Vol. 24, Issue 5, pp. 1189-1197, May 2009.

[7] S.K. Mazumder and T. Sarkar, "Optically-activated gate control for power electronics," IEEE Transactions on Power Electronics, vol. 26, no. 10, pp. 2863-2886, 2011.

[8] A. Meye, S.K. Mazumder, and H. Riazmontazer, "Optical control of 1200-V and 20-A SiC MOSFET," Applied Power Electronics Conference and Exposition (APEC), pp. 2530-2533, Feb. 2012.

[9] Q. Zhang, A. Agarwal, C. Capell, L. Cheng, M. O'Loughlin, A. Burk, J. Palmour, V. Temple, A. Ogunniyi, H. O'Brien, and C.J. Scozzie, "SiC super GTO thyristor technology development: Present status and future perspective," Pulsed Power Conference (PPC), pp. 1530-1535, Jun. 2011.

[10] J. Nishizawa, T. Terasaki, and J. Shibata, "Field-effect transistor versus analog transistor (static induction transistor)," IEEE Transactions on Electron Devices, vol. 22, no. 4, pp. 185-197, Apr. 1975.

[11] A. Caruso, P. Spirito, G. Vitale, G. Busatto, G. Ferla, and S. Musumeci, "Performance analysis of a bipolar mode FET (BMFET) with normally off characteristics," IEEE Transactions on Power Electronics, vol. 3, no. 2, pp. 157-163, Apr. 1988.

[12] G. Breglio, R. Casavola, A. Cutolo, and P. Spirito, "The bipolar mode field effect transistor (BMFET) as an optically controlled switch: numerical and experimental results," IEEE Transactions on Power Electronics, vol. 11, no. 6, pp. 755-767, Nov. 1996.