Letters

Deadtime Elimination in a GaN-Based Grid-Connected Differential-Mode Ćuk Inverter

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***Abstract*—In this letter, the effect of deadtime in a gallium nitride (GaN) based grid-connected differential-mode Ćuk converter with high-frequency (HF) transformer isolation is analyzed. It is shown that different levels of lower order harmonics appear in the grid current depending on the power factor of an operation. Utilizing the leakage inductance of the HF transformer, the deadtime is suitably eliminated to result in an improved grid-current total harmonic distortion (THD). Experimental results support the proposed solution.**

***Index Terms*—Ćuk converter, deadtime, inverters.**

I. Introduction

A DIFFERENTIAL-MODE Ćuk inverter (DMCI) in Fig. 1 is a boost-derived topology [1], [2], which has the advantages of low device count, modularity, integrated filters, and simple gate-drive circuit [3]. The harmonic distortion issue in boost-derived converters is due to the inherent nonlinearity of these inverters [3], [4]. There can be additional harmonic distortion due to the deadtime between the devices per module. The deadtime effect in conventional buck-derived voltage-source inverters is known [5]–[7]. For boost-derived inverters, the deadtime is used as indicated in [8]. However, a detailed analysis of the effects of deadtime in boost-derived inverters, such as the DMCI, has not been reported.

In this letter, the effect of deadtime in an HF transformer-isolated DMCI is analyzed. A simple solution to alleviate the problems caused by the deadtime is proposed. In this approach, the deadtime is suitably eliminated without affecting the normal operation of the DMCI. The effect of the proposed solution in reducing the THD of the grid current for ZPF or unity power factor (UPF) is validated experimentally.

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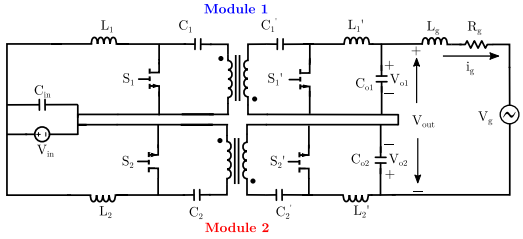

Fig. 1. Grid-connected gallium nitride (GaN) based DMCI with high-frequency (HF) transformer isolation.

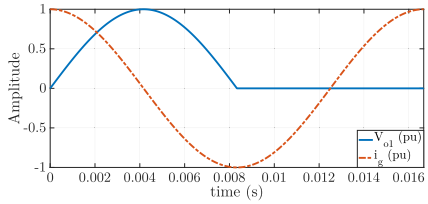

Fig. 2. Module 1 output voltage (v_{o1}) and grid current (i_g) for zero power factor (ZPF) (lead).

II. Deadtime in the DMCI With Discontinuous Modulation Scheme (DMS)

In DMS, each module of the DMCI is active for half a fundamental cycle. The modules produce half-sinusoidal voltages such that the differential output is a sine wave [3]. If V_{o1} and V_{o2} are the module output voltages in Fig. 1, the sinusoidal differential output voltage is given by $V_{\text{out}} = V_{o1} - V_{o2}$.

Ideally, complementary switching of S_1 and S_1' is desired. However, practically, a turn-ON delay or deadtime is introduced for each switch as the switches have finite turn-ON and turn-OFF time, which cause a conduction overlap and a possible shoot-through of the capacitors C_1 and C_1'. To avoid the shoot-through, a deadtime is introduced. Typical deadtime used is a few hundreds of nanoseconds for Si MOSFETs, whereas it is an order of magnitude smaller for the GaN-field effect transistors (FETs).

III. Analysis of the Effect of Deadtime in a DMCI

Fig. 2 shows per unit output of module 1 and the grid current for the ZPF lead operation. The four switching modes can be identified when $i_g > 0$ and module 1 is switching. These

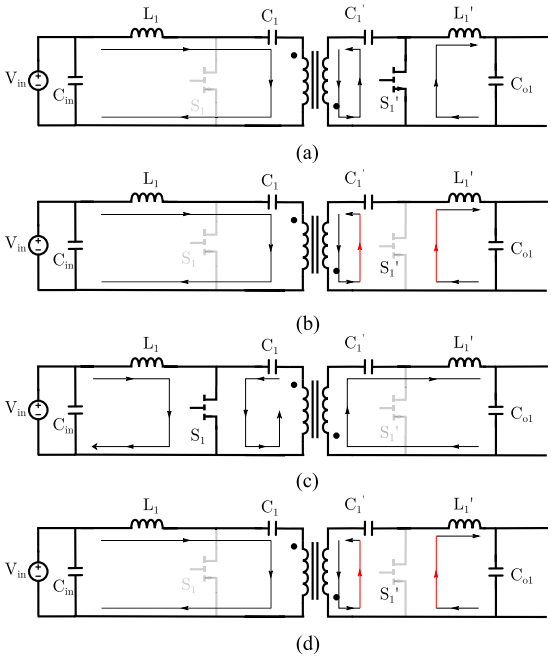

Fig. 3. Modes of operation of module 1 for ZPF case with $i_g > 0$. (a) $S_1 = 0$, $S_1' = 1$. (b) $S_1 = 0$, $S_1' = 0$ (Deadtime). (c) $S_1 = 1$, $S_1' = 0$. (d) $S_1 = 0$, $S_1' = 0$ (Deadtime).

modes correspond to $S_1 = 0$, $S_1' = 1$; $S_1 = 0$, $S_1' = 0$; $S_1 = 1$, $S_1' = 0$; and $S_1 = 0$, $S_1' = 0$. The second and the last modes correspond to the deadtime interval. These modes are shown in Fig. 3. It can be seen from Fig. 3 that while transitioning from the active states corresponding to Fig. 3(a) and (c), the deadtime period results in prolonging the state in Fig. 3(a). This is because the diode of S_1' takes over the conduction and the switch voltage continues to be zero. Thus, there is a net decrease in the output voltage compared to the ideal case. Note that in case of GaN-FETs, there is no body diode. The FET conducts in the reverse direction with a relatively higher voltage drop. The other transition from Fig. 3(c) to (a) involves another deadtime period in Fig. 3(d). However, this does not result in a deviation in the output voltage as the deadtime period is practically identical to Fig. 3(a), with the reverse conduction of the GaN-FET S_1'. Thus, the output voltage has no error during this transition. There may be a small increase in the power loss as the reverse conduction is lossy compared to the forward conduction of the GaN FET. Thus, the net effect of deadtime in this period is a decrease in the output voltage when $i_g > 0$. This is similar to the case of half-bridge inverters as discussed in [5].

The behavior of the DMCI differs from that of the half-bridge inverters in the expression of the deadtime error voltage. Consider the operation of the DMCI module 1 during the mode described in Fig. 3(a). Here, the voltage across S_1' is zero. It continues to be zero during the deadtime in the mode shown in Fig. 3(b). Ideally, the switch voltage should have changed to that of the operation in Fig. 3(c). The voltage expression for S_1' during the mode in Fig. 3(c) is derived as follows. The symbols used in the following equations are indicated in Fig. 4.

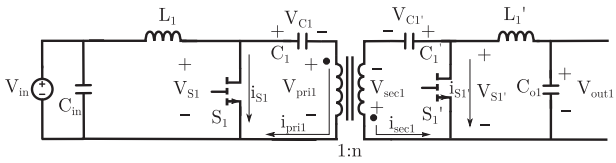

Fig. 4. Module 1 of the DMCI with various voltages and currents marked.

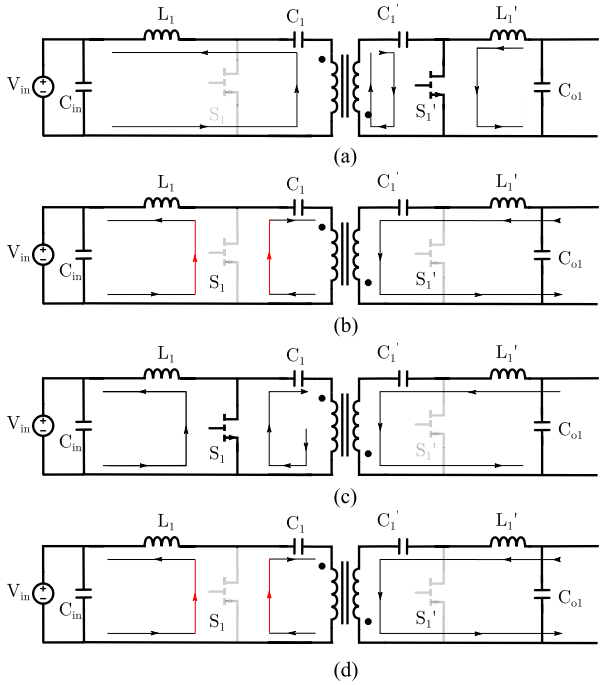

Fig. 5. Modes of operation of module 1 for ZPF case with $i_g < 0$. (a) $S_1 = 0$, $S_1' = 1$. (b) $S_1 = 0$, $S_1' = 0$ (Deadtime). (c) $S_1 = 1$, $S_1' = 0$. (d) $S_1 = 0$, $S_1' = 0$ (Deadtime).

Transformer primary voltage is given by

$$V_{\text{pri1}} = -V_{C1}. \tag{1}$$

Thus, the voltage across the switch S_1' is given by

$$V_{S_1'} = V_{C_1'} + nV_{C_1}. \tag{2}$$

The voltage in (2) is the error voltage magnitude due to the deadtime. Considering a deadtime of t_d in a switching period T_s, the average deadtime error voltage is given by

$$V_{\text{err}} = -(V_{C_1'} + nV_{C_1})t_d/T_s. \tag{3}$$

For the DMCI modules (in this case, module 1), it can be shown that $V_{C_1'} + nV_{C_1} = V_{\text{in}} + V_{\text{out1}}$. Thus, the average deadtime error voltage for $i_g > 0$ is given by

$$V_{\text{err}} = -(V_{\text{in}} + V_{\text{out1}})t_d/T_s \quad \text{for} \quad i_g > 0. \tag{4}$$

The error voltage is negative for $i_g > 0$ and the output voltage is less than the ideally expected value.

The operating modes when $i_g < 0$ are shown in Fig. 5. This case also has four switching modes. It can be seen that the transition from Fig. 5(a) to (c) through the deadtime does not

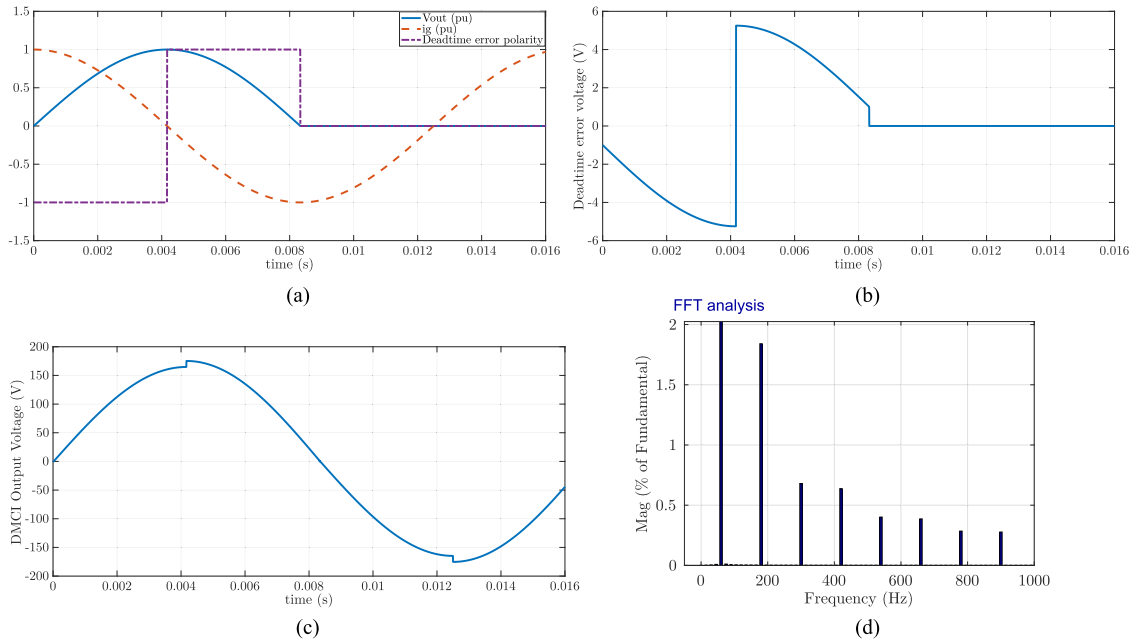

Fig. 6. (a) Module 1 output voltage, grid current, and deadtime error voltage polarity for ZPF (lead), (b) deadtime error voltage for module 1, (c) overall output voltage of the DMCI due to the deadtime, and (d) spectrum of the DMCI output voltage.

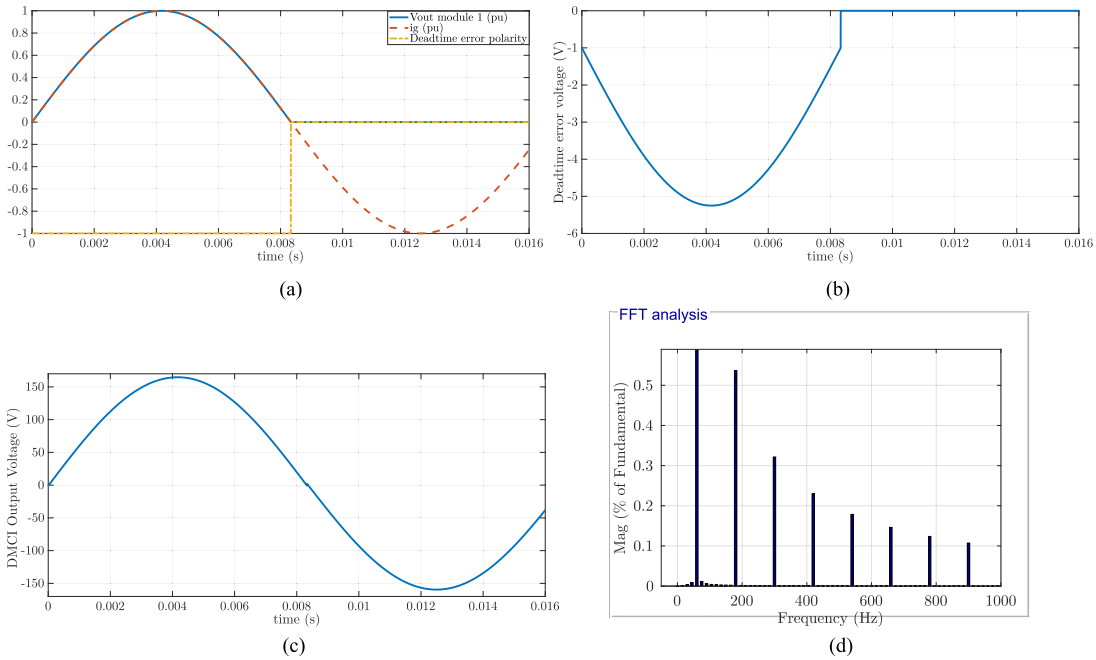

Fig. 7. (a) Module 1 output voltage, grid current, and deadtime error voltage polarity for UPF, (b) deadtime error voltage for module 1, (c) overall output voltage of the DMCI due to the deadtime, and (d) spectrum of the DMCI output voltage.

result in any voltage error as the device S_1 undergoes reverse conduction. However, the transition from Fig. 5(c) to (a) through the deadtime gives a positive voltage error as the output stays high for the period of the deadtime when the GaN-FET S_1 has reverse conduction. Thus, the average deadtime error voltage in this case is given by

$$V_{\text{err}} = (V_{\text{in}} + V_{\text{out1}})t_d/T_s \quad \text{for} \quad i_g < 0. \tag{5}$$

The effect of deadtime for the ZPF case is shown in Fig. 6. The polarity of the deadtime error voltage depends on the polarity of the grid current. This is shown in Fig. 6(a).

The actual deadtime error voltage is shown in Fig. 6(b). The deadtime is taken as $t_d = 250$ns, and the switching frequency is selected to be 100kHz. Considering 120 V single-phase output voltage and $V_{\text{in}} = 40$ V, the deadtime error voltage shown in Fig. 6(b) has an amplitude close to 5 V. For module 2, similar

error voltage is obtained, which will be phase shifted by half fundamental cycle. The combined effect of the deadtime on the DMCI output voltage is shown in Fig. 6(c). It can be observed that the waveform deviates from a perfect sinusoid. Its spectrum is shown in Fig. 6(d) and clearly shows lower order harmonic voltages. As the grid voltage ideally contains only the fundamental component, the lower order harmonics in the DMCI output voltage, as seen in Fig. 6(d), inject lower order harmonic currents to the grid, hence increasing the grid-current THD. It must be noted that a mismatch in the modules will further affect the harmonic content as discussed in [9].

In the UPF operation, the error voltage due to the deadtime does not change polarity when the module is active. The effect of deadtime for the UPF case is shown in Fig. 7, as done for the ZPF case. It can be observed from Fig. 7(c) and (d), that in UPF, the harmonic distortion is considerably lesser than that of the ZPF case.

Note that the analysis assumes that the deadtime used in both the modules is identical. Practically, however, there can be a mismatch in the deadtimes. This will affect the module voltages shown in Figs. 6(b) and 7(b). These voltages will not have different harmonic spectrum. This can result in an increase in THD including an occurrence of even harmonics and/or dc offsets. For the case when the deadtimes are identical, the even harmonics will be zero even though the module voltages clearly have an even harmonic. This is because a 180° phase shift in the module voltages results in a cancellation of the even harmonics. The mismatch effect in increasing the THD is demonstrated experimentally in Section V.

IV. Deadtime Elimination Approach for the DMCI

In order to minimize the effect of deadtime on grid-voltage harmonics, ideally the deadtime needs to be eliminated. Another approach is to use a closed-loop controller that compensates for the deadtime error voltage. The control-based approaches require a higher bandwidth, which is difficult to achieve in a DMCI. This is because it exhibits fourth-order dynamics and right-half-plane zeros.

As discussed in Section III, the deadtime error voltage appears only in one of the transitions in an active module of the DMCI. If deadtime is eliminated for this transition, then the additional harmonic distortion and dc offsets can also be reduced. Ideally, it is not possible to eliminate the deadtime as it leads to the shoot-through of the blocking capacitors ($C_1, C_1'; C_2, C_2'$). Practically, however, the HF transformer has a leakage inductance that limits the shoot-through current and eliminates the deadtime transition in the DMCI that causes the harmonic distortion. The practical DMCI with a leakage inductance is shown in Fig. 8. The current commutation when this deadtime transition is eliminated occurs in the following steps for module 1 for $i_g > 0$.

1) Consider $S_1' = 1$ and $S_1 = 0$.
2) Now, without providing a deadtime, the switching is reversed to get $S_1' = 0$ and $S_1 = 1$. There can be an overlap period of less than 10 ns for GaN FETs[10].
3) During the overlap period, the primary and secondary currents start to reduce. They do not change instantaneously due to the presence of the leakage inductance. After a finite time the primary current becomes zero. The current in the secondary switch is given by $i_{S1'} = -(i_{\text{sec1}} + i_{L1'})$.
4) After reaching zero, both primary and secondary currents change polarity till $i_{\text{sec1}} = -i_{L1'}$. Then, the secondary current gets clamped to the current in L_1', while S_1 carries the sum of the primary current and the input inductor current.

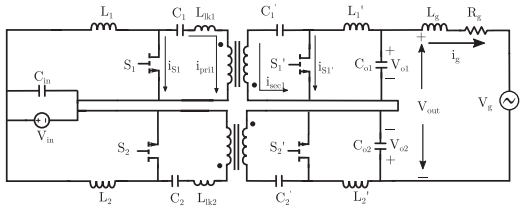

Fig. 8. Practical DMCI with the leakage inductance of the HF transformer.

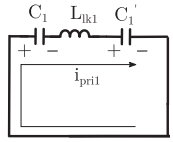

Fig. 9. HF transformer equivalent circuit during the overlap period.

Thus, the interaction between the leakage and the filter inductors during the overlap time results in avoiding the shoot-through of the blocking capacitors of the DMCI.

Consider the commutation period mentioned in step 3) previously. Both the switches of module 1 are assumed to conduct. The transformer equivalent circuit referred to the primary during this period is shown in Fig. 9. The switches are considered as short circuits during the conduction overlap period.

The voltage across the leakage inductance is given by

$$V_{lk} = -V_{c1} - \frac{V_{C_1'}}{n} = L_{lk}\frac{di_{\text{pri1}}}{dt}. \tag{6}$$

In a DMCI, the net blocking capacitor voltage is

$$V_{c1} + \frac{V_{C_1'}}{n} = \frac{V_{\text{in}}}{1 - D_1}. \tag{7}$$

The rate of change of the primary current is found to be

$$\frac{di_{\text{pri1}}}{dt} \approx \frac{\Delta i_{\text{pri1}}}{\Delta t} = -\frac{V_{\text{in}}}{L_{lk}(1 - D_1)}. \tag{8}$$

The primary current changes from an initial value of i_{L_1} to a value of $-ni_{L_1'}$ before the secondary current gets clamped to the magnitude of $i_{L_1'}$. For the experimental setup described in Section V, time taken for this to happen exceeds 20 ns, which is considerably higher than the overlap time of 5.4 ns for the GaN FET used [10]. Similar arguments apply to module 2.

Note that the other deadtime transition has not been eliminated. Consider the case when $S_1 = 1$ and $S_1' = 0$. When the deadtime is included, the module will have the state $S_1 = 0$ and $S_1' = 0$. During this period, the transformer currents fall and S_1' starts to conduct with reverse conduction (akin to body diode conduction in Si MOSFETs). Now, S_1' can be provided with a turn-ON command to have a ZVS turn-ON transition. This is

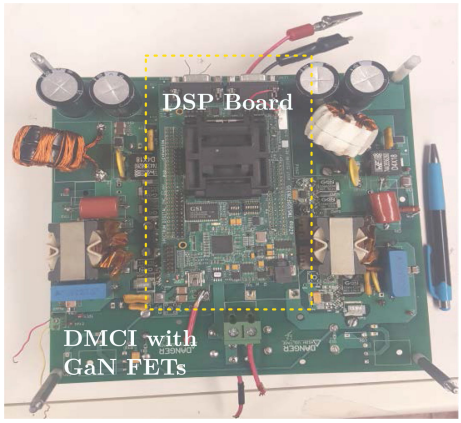

Fig. 10. Experimental setup of the DMCI.

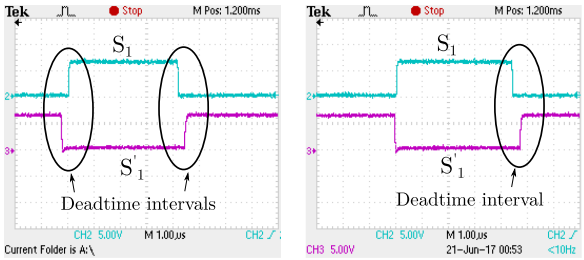

Fig. 11. Gate-drive pulses of S_1 and S_1' when (a) the conventional deadtime approach is used, and (b) with the proposed deadtime elimination. Scale: Gating pulses = 5 V/div.

preferable to directly turn ON the switch S_1' without including the deadtime, which would result in some switching loss.

V. Experimental Validation

The effect of the deadtime on the grid-current THD is observed experimentally. The prototype inverter is rated for a maximum power of 500 W. The switching frequency is 100 kHz, and the HF transformer has a leakage inductance of 400 nH from the primary side. The GaN devices used are GS66508P by GaN systems. Fig. 10 shows the picture of the experimental setup. The closed-loop control is implemented in the DSP TMS320F28335 that is stacked on top of the DMCI in Fig. 10.

The conventional pulses for the switching of module 1 are shown in Fig. 11(a). It can be seen that a deadtime is provided for both the switching transients. The proposed approach involved the elimination of deadtime based on the polarity of the current. For the case when $i_g > 0$, it is shown in Fig. 11(b). The grid currents for the ZPF case with deadtime [see Fig. 11(a)] and using the proposed deadtime elimination approach [see Fig. 11(b)] are captured in Fig. 12(a) and (b), respectively. The latter shows an improvement in the grid-current THD from 9.7% to 6.6%. The harmonic spectrum of the grid current for the case with the deadtime and with the proposed approach is provided in Fig. 13(a) and (b), respectively.

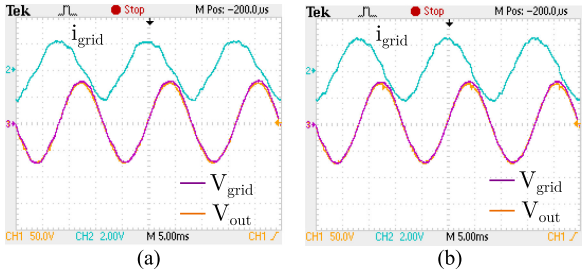

Fig. 12. Performance of the DMCI under ZPF using (a) deadtime and (b) proposed deadtime elimination approaches. Scale: V_{grid} and V_{out} = 50 V/div, i_{grid} = 2 A/div.

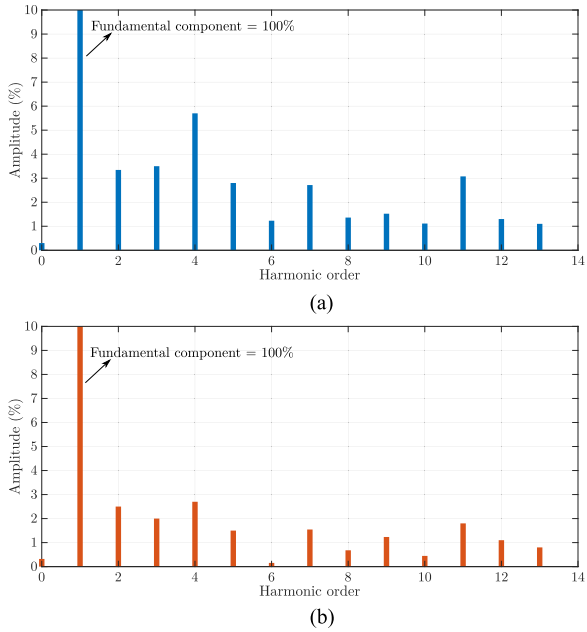

Fig. 13. Harmonic spectrum of the grid current for the ZPF operation (a) with conventional deadtime and (b) with proposed deadtime elimination approaches.

The DMCI output voltage for the ZPF case differs considerably from the UPF case as can be seen from Figs. 6(c) and 7(c). The small jumps seen near the peak of the DMCI output voltage for the ZPF case are shown in Fig. 14. The experimental result is seen to match the ideally expected result in Fig. 6(c).

Improvement in the harmonic content for the UPF case with the proposed approach is seen from Fig. 15(a) and (b).

The THD corresponding to the case with conventional deadtime is measured to be 4.32%, whereas the proposed deadtime elimination approach resulted in a THD of 3.0%. The harmonic spectra for the UPF case corresponding to Fig. 15 are shown in Fig. 16(a) and (b). It can be observed that there is an overall decrease in the harmonic content with the proposed approach.

The grid-current THD is affected by any mismatch in deadtime values used for the modules of DMCI as discussed in Section III. In Fig. 17, module 1 has a deadtime of 200 ns, while module 2 has a deadtime of 60 ns, illustrating the case of deadtime mismatch. The grid-current distortion is considerably higher than the case shown in Fig. 15(a), where equal deadtime was implemented. From the nature of the waveform, it is vi-

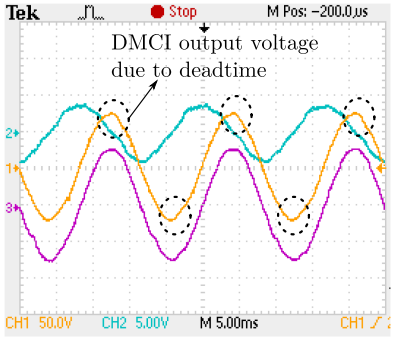

Fig. 14. DMCI output voltage in ZPF highlighted to show the jumps near the peak due to the deadtime effect. Scale: $V_{\rm grid}$ and $V_{\rm out}$ = 50 V/div, $i_{\rm grid}$ = 5 A/div.

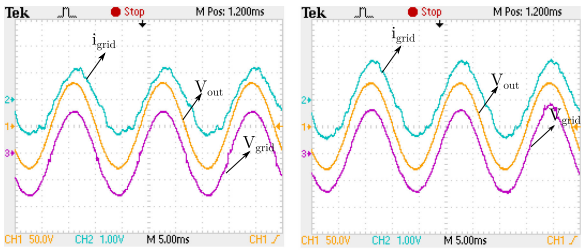

Fig. 15. Performance of the DMCI under UPF using (a) deadtime and (b) proposed deadtime elimination approaches. Scale: $V_{\rm grid}$ and $V_{\rm out}$ = 50 V/div, $i_{\rm grid}$ = 2 A/div.

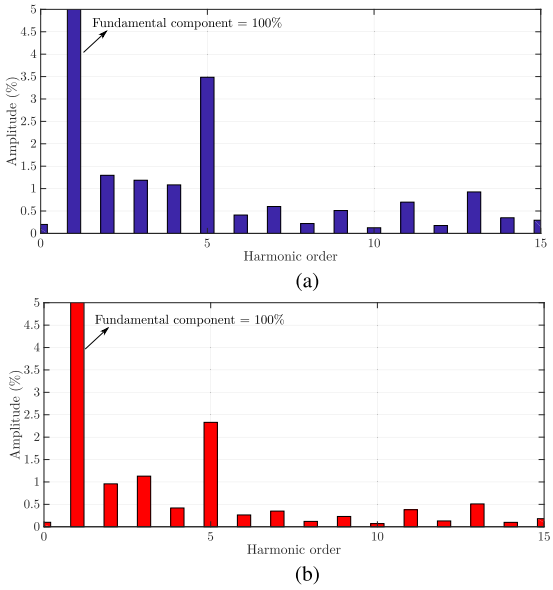

Fig. 16. Harmonic spectrum of the grid current for the UPF operation (a) with conventional deadtime and (b) with proposed deadtime elimination approaches.

sually clear that there are even harmonics (due to the lack of odd-symmetry) and a marginal increase in the dc offset.

The results shown in Figs. 12–17 are shown at lower current to highlight the harmonic distortion issue. The grid interconnection standard IEEE 1547 specifies a THD limit of 5% for the rated

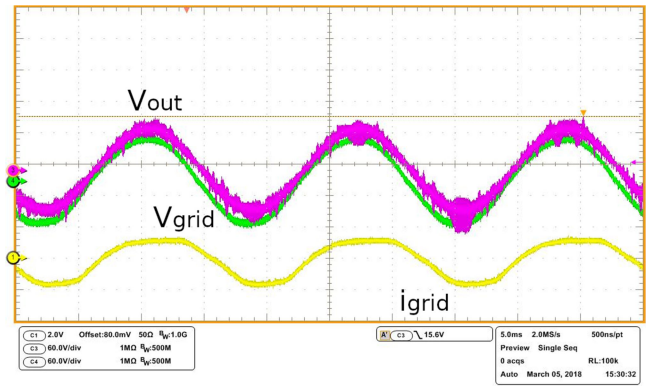

Fig. 17. Increased harmonic distortion in the grid current when there is a mismatch in the deadtime of the two modules of the DMCI. Channel 1: Grid current ($i_{\rm grid}$: 2 A/div); channel 3: DMCI output voltage ($V_{\rm out}$: 60 V/div); channel 4: grid voltage ($V_{\rm grid}$: 60 V/div).

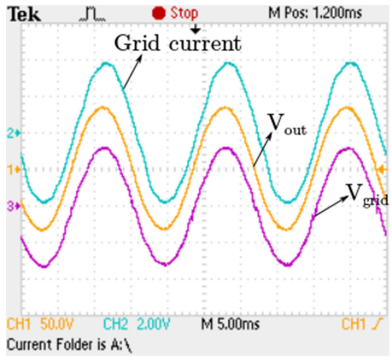

Fig. 18. Performance of the DMCI at higher grid current showing reducing harmonic distortion. Scale: $V_{\rm grid}$ = 50 V/div, $V_{\rm out}$ = 50 V/div, and $i_{\rm grid}$ = 2 A/div.

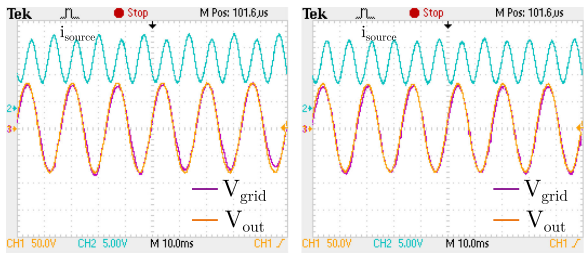

Fig. 19. Impact on the source current of the DMCI using (a) deadtime and (b) proposed deadtime elimination approaches. Scale: $V_{\rm grid}$ and $V_{\rm out}$ = 50 V/div, $i_{\rm grid}$ = 5 A/div.

operating conditions, which is met by the proposed converter. However, it is still important to reduce the THD at lower power operation in order to improve the efficiency. An increase in harmonics results in a drop in efficiency as the harmonic power does not contribute to average power transferred to the grid. The experimental result at higher grid current is shown in Fig. 18. It can be seen that the distortion is lower and the grid-current THD is measured to be 2.8%, which meets the IEEE 1547 standard.

The source current of the DMCI is shown in Fig. 19. It can be seen that for the case with conventional deadtime in Fig. 19(a), the half cycles are of unequal amplitude. For the proposed deadtime elimination case in Fig. 19(b), the half cycles are similar

with better amplitude equalization, which is a reflection of the overall THD reduction in the grid current.

VI. Conclusion

The usage of fast-switching GaN FETs and the presence of the leakage inductance in the DMCI helps in eliminating the deadtime transition that causes the harmonic distortion. During the time interval when the deadtime is eliminated, there can be a shoot-through condition. However, the GaN-FETs and the transformer leakage inductance mitigate the shoot-through current. This results in improving the grid-current THD significantly, as evident from the experimental results on a laboratory developed prototype DMCI.

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