Master–Slave Current-Sharing Control of a Parallel DC–DC Converter System Over an RF Communication Interface

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***Abstract*—Using analog wireless communication, we demonstrate a master–slave load-sharing control of a parallel dc–dc buck converter system, thereby eliminating the need for physical connection to distribute the control signal among the converter modules. The current reference for the slave modules is provided by the master module using radio-frequency (RF) transmission, thereby ensuring even sharing of the load current. The effect of delay due to RF transmission on system stability and performance is analyzed, and regions of operation for a stable as well as satisfactory performance are determined. We experimentally demonstrate a satisfactory performance of the master–slave converter at 20-kHz switching frequency under steady state as well as transient conditions in the presence of a transmission delay. The proposed control concept, which can potentially attain redundancy that is achievable using a droop method, may lead to more robust and reconfigurable control implementation of distributed converters and power systems. It may also be used as a (fault-tolerant) backup for wire-based control of parallel/distributed converters.**

***Index Terms*—Load sharing, master–slave control, parallel dc–dc converter, time delay effects, time-delayed system stability, wireless-network-based control.**

I. Introduction

LOAD-SHARING parallel dc–dc converters potentially offer several advantages over a single standalone unit in terms of modular architecture, reconfigurability, redundancy and fault tolerance, and cost. However, the reliability of such distributed systems relies heavily on their ability to share the power equally during steady state as well as transient conditions. One of the commonly used methods for stabilization of parallel dc–dc converters is the conventional droop method [1], [2], which is shown in Fig. 1(a). Load sharing among the power supplies using the droop method is dependent on the output-voltage setting of each power converter and may be compromised if a tight voltage regulation is desired. Active current-sharing mechanisms [3]–[7] provide a better alternative to conventional droop methods by monitoring the difference between the reference current (which, for instance, could be the average of the currents of all parallel modules or the current of a dedicated or democratic master) and the output (or inductor) current of each converter module and incorporate this information into the control loop. One common current-sharing approach is the dedicated master–slave control scheme, as shown in Fig. 1(b), which ensures that all of the slave modules follow the reference current of the master. However, traditional current-sharing mechanisms rely on a physical connection among the converter modules; hence, system redundancy and reconfigurability may be compromised.

A radio-frequency (RF)-based wireless-network control of power electronic converters has been proposed in [8]–[10], which can be used to achieve a level of redundancy that is close to that of the droop method, while ensuring that the load-sharing performance and voltage regulation of the system are not compromised. In [8], a pulsewidth modulated (PWM) signal-sharing mechanism (over a digital link) for a parallel dc–dc converter is demonstrated. However, the bandwidth is limited due to the lack of current-sharing loops. In this paper, we propose a dedicated master–slave control scheme based on information transfer over a wireless communication link from the master module to the slave, as shown in Fig. 1(c). The effectiveness of the wireless-network-control scheme is demonstrated for a switching frequency of 20 kHz and for a channel separation of approximately 3 ft. Furthermore, we determine the impacts of RF communication delay [11], [12] on the stability and performance of the parallel converter, with focus on the following:

1) reaching condition for orbital existence (which predicts convergence to an orbit from any arbitrary initial condition during transients/start-up [13]);
2) steady-state stability;
3) load-sharing performance.

For 1), we use a nonlinear technique based on multiple-Lyapunov functions, which is described by the authors in [14] and [15]. For 2), we use a linearized average model and frequency domain techniques, presented in [16]. For 3) we use time-domain simulations during steady state and transients. These analysis techniques are used to obtain the bounds for the time delays, which ensure that the stability and performance of the parallel converter are not compromised.

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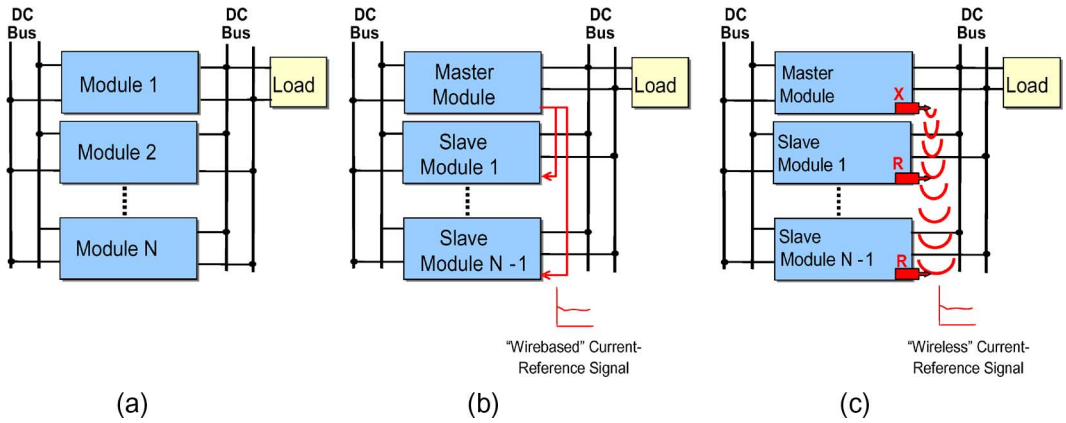


Fig. 1. Paralleling schemes for dc–dc converter. Wire-based (a) droop and (b) master–slave methods for distributing the current-reference signal of the master module among the $N-1$ slave modules. (c) Wireless master–slave current-sharing method, where the RF transmitter and receiver are represented, respectively, by the symbols X and R.

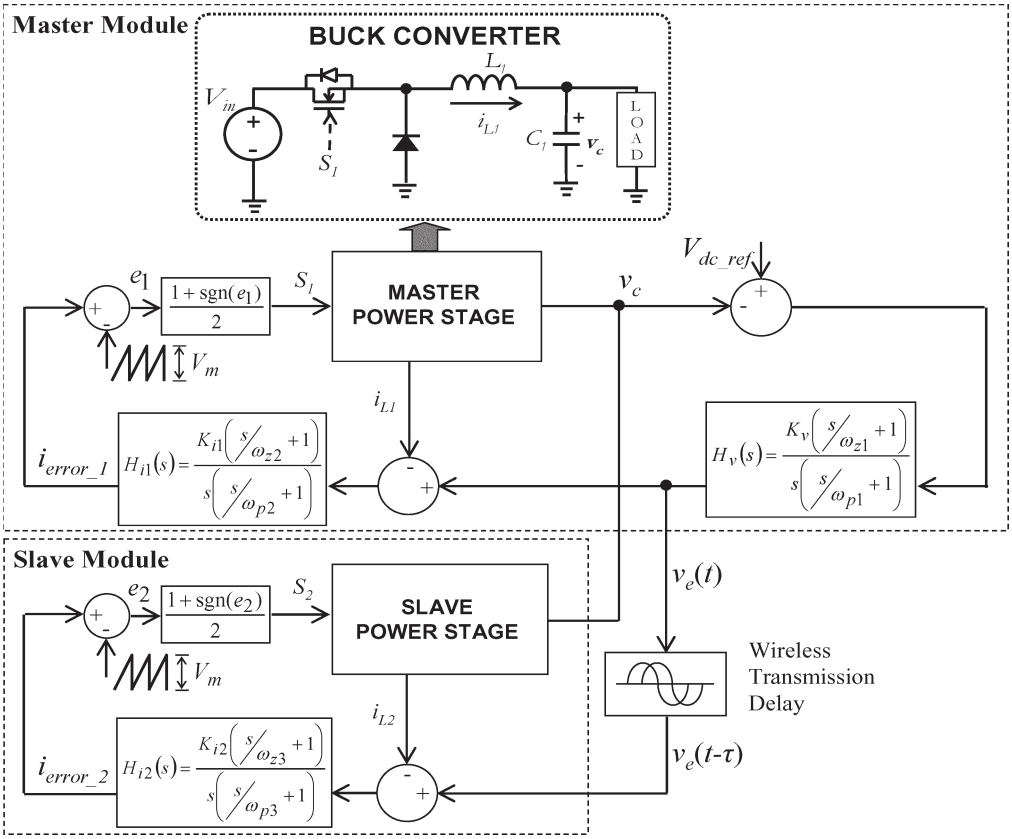


Fig. 2. Block diagram of the parallel dc–dc buck converter with wireless master–slave load-sharing control scheme. The slave module only has a current loop; the reference for its current loop is transmitted wirelessly from the master module using an analog RF transmitter block.

II. Control Scheme and Stability Analysis

The control scheme for load-sharing dc–dc buck converters with N-modules connected in parallel is shown in Fig. 2. The controller for the master module has two control loops: voltage and current loops. The output of the voltage loop acts as the reference for the current loop. All the slave modules have the same controller structure and receive the current reference from the master module. In this section, we demonstrate the control design and stability analyses for a converter with two parallel-connected modules. The analyses can be further extended to a higher number of modules by appropriately changing the system models.

The transfer functions of the voltage- and current-loop compensators of the master module are $H_v(s)$ and $H_{i1}(s)$, respectively. The gain of the voltage loop (K_v) affects voltage regulation of the system (with variations in the load, input, and power-stage parameters) and current reference of the modules. The gain of the current loop (K_{i1}) is tuned to achieve a

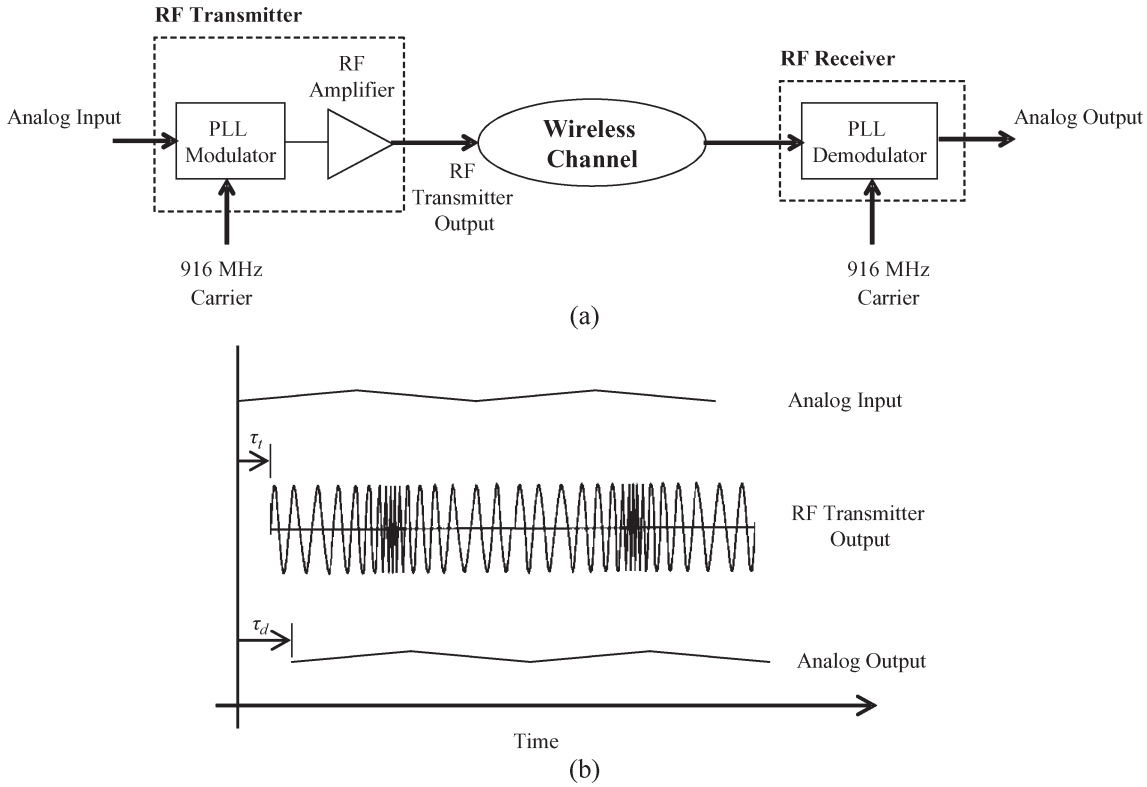


Fig. 3. Frequency-modulated RF transmission of the current-reference signal. (a) Block diagram for the transmitter, channel, and receiver. (b) Signal waveforms at the input of the transmitter (Analog Input), modulated signal at the output of the transmitter (RF Transmitter Output), where the maximum magnitude of the analog input signal corresponds to the maximum frequency but is delayed by the transmission delay τ_t, and the demodulated signal at the receiver output (Analog Output) which is delayed by a total delay of τ_d.

good transient response. The poles and zeros of the controllers are chosen so as to ensure that the closed-loop system has an adequate bandwidth and phase margin. The output of the current loop, which is an error signal, is passed through a comparator, whose other input is a ramp signal. The output of the comparator is the PWM signal, which (after passing it through a gate driver) is used to control the power MOSFET of the buck converter. The frequency of the ramp signal determines the switching frequency of the converter.

For $N = 2$, the transfer function of the current loop of the slave module is given by $H_{i2}(s)$. The reference for this controller is generated by the voltage loop of the master. This ensures that the current distribution between the two modules is even, thus alleviating problems associated with unequal load sharing among the converter modules. However, any mismatch in the current reference of the two modules (due to transmission error or delay from the master to the slave module) can lead to a load-sharing error. Because the gain of the voltage loop determines the current reference for the master and slave modules, it affects the dynamics and performance of the load-sharing converter. The current reference of the master module is transmitted to the slave module through a wireless communication channel. To achieve this, first, the current-reference signal of the master is fed to an RF transmitter on the master module. The RF transmitter broadcasts it after modulating the signal using a high-frequency carrier, as shown in Fig. 3. Subsequently, the transmitted signal is captured by the receiver antenna, which is tuned to RF transmission frequency as well. The receiver demodulates and tunes the received current-reference signal such that it closely matches the current-reference signal of the master. This current-reference signal is then fed to the current loop of the slave module. The wireless channel is modeled as a single delay (comprising transmission, propagation, and reception delays). Delay due to propagation is relatively small for channel lengths lesser than 100 ft. An increase in the switching frequency results in an increase in the phase lag between the master and slave controller outputs. By assuming that τ_d is the time delay from the master module to the slave module and that f_s is the switching frequency, then the phase lag between the two modules is given by $\Delta\phi = f_s \times \tau_d$.

To investigate the impacts of time delay on the dynamics of the parallel buck converter, we consider two modes of operation. First, we investigate the reaching conditions for orbital existence of the converter using a piecewise-linear model of the system [14], [15]. Such analyses can be used to determine if the state-trajectories of the parallel converter converge to an orbit in the presence of time-delays due to the wireless communication network. The state-space equation of this system can be expressed as

$$\dot{x}(t) = A_{0i}x(t) + A_{1i}x(t - \tau_d) + B_i \tag{1}$$

where i denotes the switching state of the system, $x = [i_{L1} \quad i_{L2} \quad v_C \quad \xi_1 \quad \xi_2 \quad \xi_3 \quad \xi_4 \quad \xi_5 \quad \xi_6]^{\mathrm{T}}$ is the state of the

converter, and τ_d is the time delay among the states. A_{0i}, A_{1i}, and B_i, which are shown at the bottom of the page, depend on the switching states. For the two-module parallel buck converter, i can take any value from 0 to $(2^2-1=3)$ depending on the output of the feedback controllers ($i_{\text{error\_1}}$ and $i_{\text{error\_2}}$).[1] The switching states of the converter can be expressed as

$$S_k(t)=\begin{cases}0, & i_{\text{error\_}k}(t)\le V_{\text{mod}}\\ 1, & i_{\text{error\_}k}(t)>V_{\text{mod}}\end{cases},\qquad k=\{1,2\}. \tag{2}$$

From this point onwards, we drop the notation of time, and an arbitrary time-delayed vector $y(t-\varphi)$ is represented as y_φ or $y(t+\varphi)$ as $y_{-\varphi}$. We transform (1) to the error coordinates using $e=x^*-x$, where x^* is the desired value of the states. The modified state-space equations in the error coordinates can be expressed as

$$\dot{e}=A_{0i}e+A_{1i}e_{\tau_d}-(A_{0i}+A_{1i})x^*-B_i. \tag{3a}$$

Equation (3a) can be rewritten as

$$\dot{e}=(A_{0i}+A_{1i})e+A_{1i}(e_{\tau_d}-e)-(A_{0i}+A_{1i})x^*-B_i. \tag{3b}$$

[1] $(i=0):(S_1=0,S_2=0)$; $(i=1):(S_1=1,S_2=10)$; $(i=2):(S_1=0, S_2=1)$; and $(i=3):(S_1=1,S_2=1)$.

Using

$$\begin{aligned}e_{\tau_d}-e&=-[e_{-\tau}]_{\tau=-\tau_d}^{\tau=0}\\&=\int_{-\tau_d}^{0}\big(-(A_{0i}+A_{1i})e_{-\tau}-A_{1i}e_{(\tau_d-\tau)}\\&\qquad+(A_{0i}+A_{1i})x^*+B_i\big)d\tau\end{aligned}$$

(3b) can be simplified to

$$\dot{e}=(A_{0i}+A_{1i})e-\int_{-\tau_d}^{0}A_{1i}A_{0i}e_{-\tau}d\tau-\int_{-2\tau_d}^{-\tau_d}A_{1i}^2e_{-\tau}d\tau+\overline{B}_i \tag{3c}$$

where $\overline{B}_i=-B_i-(A_{0i}+A_{1i})x^*+\tau_dA_{1i}(B_i+(A_{0i}+A_{1i})x^*)$.

The reaching condition of the system described by (3c) depends on the number of feasible nonrepetitive and nonredundant switching sequences [15]. For each of these switching sequences, we define a positive-definite quadratic composite Lyapunov function $V_k(e)>0$ (for the kth switching sequence), which can be expressed as [17]

$$V_k(e)=\sum_{i=1}^{h}\alpha_{ki}e^{\mathrm{T}}P_{ki}e \tag{4}$$

$$A_{0i}=\begin{bmatrix}\frac{-r_{L1}}{L_1}&0&\frac{-1}{L_1}&0&0&\frac{K_{i1}V_{\text{in}}}{V_mL_1}&\frac{K_{i1}V_{\text{in}}\omega_{z2}}{V_mL_1}&0&0\\0&\frac{-r_{L2}}{L_2}&\frac{-1}{L_2}&0&0&0&0&\frac{K_{i2}V_{\text{in}}}{V_mL_2}&\frac{K_{i2}V_{\text{in}}\omega_{z3}}{V_mL_2}\\\frac{1}{(C_1+C_2)}&\frac{1}{(C_1+C_2)}&\frac{-1}{R(C_1+C_2)}&0&0&0&0&0&0\\0&0&-1&-\omega_{p1}&0&0&0&0&0\\0&0&0&1&0&0&0&0&0\\-1&0&0&K_v&K_v\omega_{z1}&-\omega_{p2}&0&0&0\\0&0&0&0&0&1&0&0&0\\0&-1&0&0&0&0&0&-\omega_{p3}&0\\0&0&0&0&0&0&0&1&0\end{bmatrix}$$

$$A_{1i}=\begin{bmatrix}0&0&0&0&0&0&0&0&0\\0&0&0&0&0&0&0&0&0\\0&0&0&0&0&0&0&0&0\\0&0&0&0&0&0&0&0&0\\0&0&0&0&0&0&0&0&0\\0&0&0&0&0&0&0&0&0\\0&0&0&0&0&0&0&0&0\\0&0&0&K_v&K_v\omega_{z1}&0&0&0&0\\0&0&0&0&0&0&0&0&0\end{bmatrix}$$

$$B_i=\begin{bmatrix}\frac{S_1}{L_1}V_{\text{in}}\\\frac{S_2}{L_2}V_{\text{in}}\\0\\V_{\text{ref}}\\0\\0\\0\\0\\0\end{bmatrix}$$

where h is the number of switching states in a given sequence, $0 \le \alpha_{ki} \le 1$, $\sum_{i=1}^{h} \alpha_{ki} = 1$, $P_{ki} = P_{ki}^{\mathrm{T}}$ is a positive definite matrix, and $pV_k(e) \ge V_k(e_\theta)$, for any $-\tau \le \theta \le 0$ and $p > 1$. The error trajectories of the system described by (3c) converge to the orbit if there exists $P_{ki} > 0$, such that $\dot{V}_k(t) < 0$. To determine whether this condition is satisfied by (3c), we have a matrix inequality given by [14], [15]

$$\sum_{i=1}^{h} \alpha_{ki} \begin{bmatrix} M_{ki} & P_{ki}A_{1i}A_{0i} & -P_{ki}A_{1i}^2 & P_{ki}\overline{B}_i \\ -A_{0i}^{\mathrm{T}}A_{1i}^{\mathrm{T}}P_{ki} & -pP_{ki} & 0 & 0 \\ -\left(A_{1i}^2\right)^{\mathrm{T}} P_{ki} & 0 & -P_{ki} & 0 \\ \overline{B}_i^{\mathrm{T}} P_{ki} & 0 & 0 & 0 \end{bmatrix} < 0 \tag{5}$$

where $M_{ki} = (1/\tau_d)\lfloor P_{ki}(A_{0i} + A_{1i}) + (A_{0i} + A_{1i})^{\mathrm{T}} P_{ki} \rfloor + (p+1)P_{ki}$ [16]. This inequality can be solved using standard techniques for linear-matrix inequalities [18].

If there are no solutions to (5), we investigate the dual Lyapunov function to determine that the error trajectories of the converter do not converge to the orbit [19]. The dual Lyapunov function

$$\overline{V}_k = \sum_{i=1}^{h} \alpha_{ki} e^{\mathrm{T}} Q_{ki} e. \tag{6}$$

The error trajectories of the converter do not converge to the orbit, provided that

$$\sum_{i=1}^{h} \alpha_{ki} \begin{bmatrix} N_{ki} & -Q_{ki}A_{1i}A_{0i} & Q_{ki}A_{1i}^2 & -Q_{ki}\overline{B}_i \\ A_{0i}^{\mathrm{T}}A_{1i}^{\mathrm{T}}Q_{ki} & pQ_{ki} & 0 & 0 \\ \left(A_{1i}^2\right)^{\mathrm{T}} Q_{ki} & 0 & Q_{ki} & 0 \\ -\overline{B}_i^{\mathrm{T}} Q_{ki} & 0 & 0 & 0 \end{bmatrix} < 0 \tag{7}$$

where $N_{ki} = (1/\tau_d)\lfloor Q_{ki}(A_{0i} + A_{1i}) + (A_{0i} + A_{1i})^{\mathrm{T}} Q_{ki} \rfloor + (p+1)Q_{ki}$. If there are no solutions to (5) and there exist solutions to (7), we conclude that the error trajectories of the system do not converge to the orbit.

When the power devices of all the converter modules switch periodically, we use an averaged model to analyze the stability of the system. The state-space averaged model of the system is described by

$$\dot{x} = A_0 x + A_1 x(t - \tau_d) + B \qquad y = Cx \tag{8}$$

where $x = [\widetilde{i}_{L1}\ \widetilde{i}_{L2}\ \widetilde{v}_C\ \xi_1\ \xi_2\ \xi_3\ \xi_4\ \xi_5\ \xi_6]^{\mathrm{T}}$, $A_0 = A_{0i}$, $A_1 = A_{1i}$, $B = [(d_1/L_1)V_{\mathrm{in}}\ (d_2/L_2)V_{\mathrm{in}}\ 0\ V_{\mathrm{ref}}\ 0\ 0\ 0\ 0\ 0]^{\mathrm{T}}$, $C = [0\ 0\ 1\ 0\ 0\ 0\ 0\ 0\ 0\ 0]$. Here, $\widetilde{i}_{L1} = \langle i_{L1} \rangle$, $\widetilde{i}_{L2} = \langle i_{L2} \rangle$, and $\widetilde{v}_c = \langle v_c \rangle$ are the average values for the states. The duty ratios of the switches $d_1 = \langle S_1 \rangle$ and $d_2 = \langle S_2 \rangle$ determined by the feedback controllers, as shown in Fig. 2, are given by

$$\begin{aligned} d_1 &= \frac{i_{\mathrm{error\_1}}}{V_m} = \begin{bmatrix} \dfrac{K_{i1}}{V_m} & \dfrac{K_{i1}\omega_{z2}}{V_m} \end{bmatrix} \begin{bmatrix} \xi_3 \\ \xi_4 \end{bmatrix} \\ d_2 &= \frac{i_{\mathrm{error\_2}}}{V_m} = \begin{bmatrix} \dfrac{K_{i2}}{V_m} & \dfrac{K_{i2}\omega_{z3}}{V_m} \end{bmatrix} \begin{bmatrix} \xi_5 \\ \xi_6 \end{bmatrix}. \end{aligned} \tag{9}$$

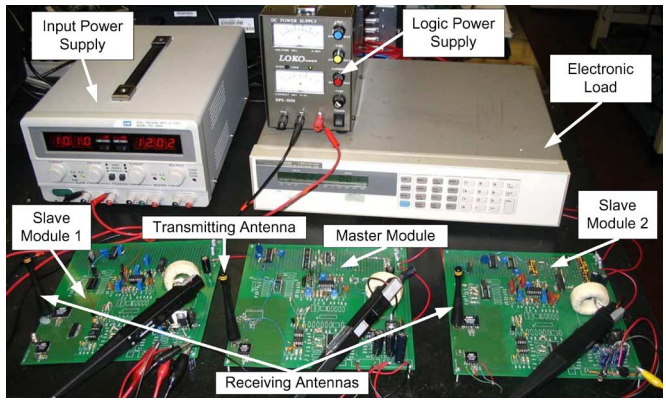


Fig. 4. Experimental setup comprising the master and two slave buck converter modules connected in parallel, logic and input power supplies, and an electronic load. The parallel power system implements dedicated master–slave current-sharing control using RF transmission.

The infinite-dimensional system in (8) with a single delay is stable if the delay τ_d is below the delay bound $\overline{\tau}$. To determine how the delay bound $\overline{\tau}$ varies with the gain of the voltage controller, we use a delay-dependent stability criterion, given in [16], which is summarized in the following.

Theorem[2]*:* For the system in (8) stable at $\tau_d = 0$, i.e., $A_0 + A_1$ is stable and $\mathrm{rank}(A_1) = q$, we define

$$\overline{\tau}_i := \begin{cases} \min\limits_{1 \le k \le n} \frac{\theta_k^i}{\omega_k^i}, & \text{if } \lambda_i\left(j\omega_k^i I - A_0, A_1\right) = e^{-j\theta_k^i} \\ & \text{for some } \omega_k^i \in (0,\infty),\ \theta_k^i \in [0, 2\pi] \\ \infty, & \text{if } \underline{\rho}(j\omega I - A_0, A_1) > 1 \quad \forall \omega \in (0,\infty) \end{cases} \tag{10}$$

then $\overline{\tau} := \min_{1 \le i \le q} \overline{\tau}_i$, and the system in (8) is stable for all $\tau_d \in [0, \overline{\tau})$ and becomes unstable at $\tau_d = \overline{\tau}$. In (10), $\underline{\rho}(A_0, A_1) := \min\{|\lambda| \mid \det(A_0 - \lambda A_1) = 0\}$, and $\lambda(A, B)$ is the generalized eigenvalue of the matrices A and B.

To use the aforementioned theorem, we devise an algorithm to compute the delay margin and also check whether the system is stable independent of delay. We first test the condition

$$\underline{\rho}(j\omega I - A_0, A_1) > 1 \qquad \forall \omega \in (0,\infty). \tag{11}$$

If the condition in (11) is satisfied for all values of ω, then the system is stable independent of delay. If there is some ω for which the condition in (11) is not satisfied, using that value, we solve $\lambda_i(j\omega I - A_0, A_1) = e^{-j\theta}$ for θ and find the corresponding delay using (10).

III. Results

Fig. 4 shows an experimental setup for the master–slave buck converter for a three-module system. The power-stage, control, and wireless-transmission parameters for the experimental parallel converter are shown in Table I. The difference in the inductance of the master and slave modules (less than 10%) is

[2]This theorem and its proof are given in [16].

TABLE I
PARAMETERS OF THE MASTER–SLAVE PARALLEL BUCK CONVERTER

Nominal Parameters	Values	Nominal Parameters	Values
Switching frequency	20 kHz	Ramp height	8 V
Bandwidth of the wireless transmitter and receiver	28 kHz	DC gain (K_v) of the master voltage loop	3000
Channel separation attempted so far	10 feet	Zero (w_{z1}) of the master voltage loop compensator	500 rad/s
Wireless transmitter to receiver delay	20 µS	Pole (w_{p1}) of the master voltage loop compensator	20,000 rad/s
Output inductance of the master	155 µH	DC gain (K_{i1}, K_{i2}) of the master/slave current loop	4000
Output inductance of the slaves	165 µH, 162 µH	Zero (w_{z2}, w_{z3}) of the master/slave current loop compensator	1000 rad/s
Output capacitance	800 µF	Pole (w_{p2}, w_{p3}) of the master/slave current loop compensator	25,000 rad/s
Reference output voltage for the master	2.5 V	Logic power supply for the master and slave boards	±15V and 5V
Input voltage	10 V	Regulated output voltage	5 V

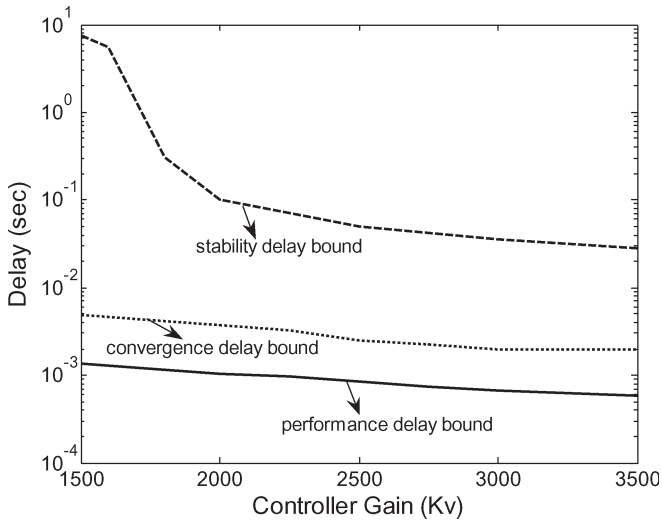


Fig. 5. Delay bound for the system to operate in stable region, to converge to the switching surface, and to meet the performance criterion (5% load-sharing error among the modules) for different values of voltage loop controller gain (K_v).

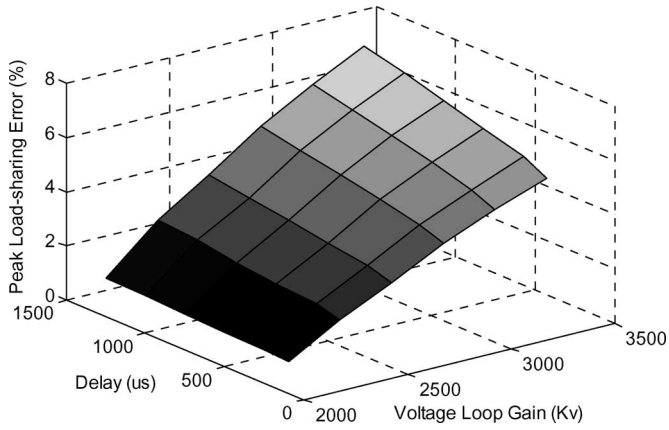


Fig. 6. Variation of peak load-sharing error with variation in the voltage loop gain and time delay between the master and slave modules.

due to small variations in the parameters of the cores and the nature of the windings. First, we examine whether the converter satisfies the reaching conditions for orbital existence. Using the conditions given in (5) and (7), we determine the bounds of the time delay for the system dynamics to converge to the orbit. Fig. 5 shows the variation of such a bound with the gain of the voltage-loop compensator. When the converter switches periodically, we use a linearized averaged model to analyze the stability of the system. For the system described by (8), $\text{rank}(A_1) = 1$, and $\overline{\tau} = \overline{\tau}_1$. To find $\overline{\tau}_1$ using the criterion in (10), we sweep the frequency from $\infty \rightarrow 0$ and find the points at which $\underline{\rho}(j\omega I - A_0, A_1) \approx 1$. Using this value of ω and the fact that there is only one nonzero generalized eigenvalue for the system considered in this paper, we have $\omega = \omega_1^1$. Next, we find the delay threshold as $\min_{1 \le k \le n} \theta_k^1/\omega_k^1$ by varying θ_k^1 in the interval of $[0, 2\pi]$. For example, the delay threshold for $K_v = 3000$ is $\overline{\tau}_1 = \theta_1^1/\omega_1^1 = 2.085/58.748 = 35.5$ ms. The time-delay bound for the system to operate in stable region at different values of the voltage controller gain is shown in Fig. 5. For the present case, this delay bound is larger than the delay bound for the system to converge to the switching surface during start-up and transient conditions.

In Fig. 6, we investigate the impact of the RF transmission delay on the performance of the load-sharing control system. We observe that the maximum difference between the output current of the converter modules under transient condition (referred to as the peak load-sharing error) increases with increasing RF transmission delay. However, for a given

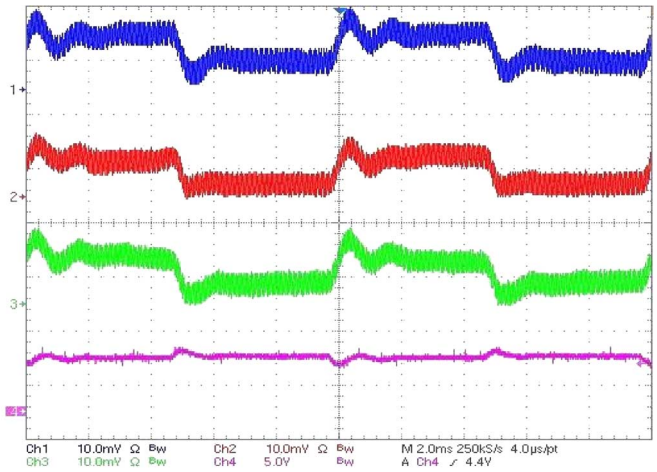


Fig. 7. Output voltage (Ch4) and master and slave inductor currents (Ch1, Ch2, and Ch3), respectively, during load-transient. The load-transient specifications are tabulated in Table II.

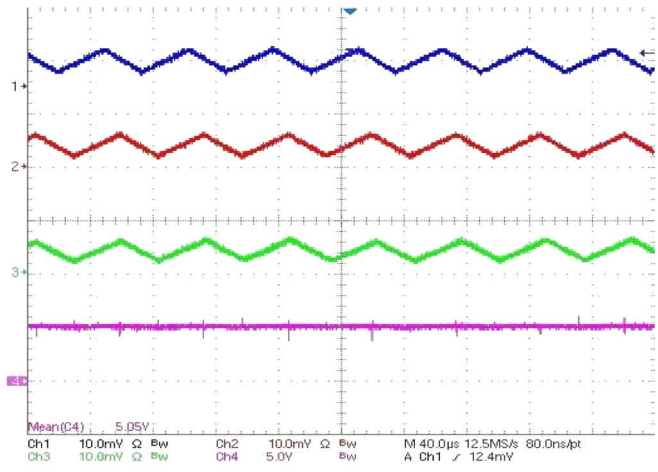
TABLE II
SPECIFICATIONS OF THE LOAD-TRANSIENT

Nominal Parameters	Values
Time period of the load-transient	10 ms
Duty ratio of the load-transient	50%
Minimum value of the load current	1 A
Maximum value of the load current	3.0 A

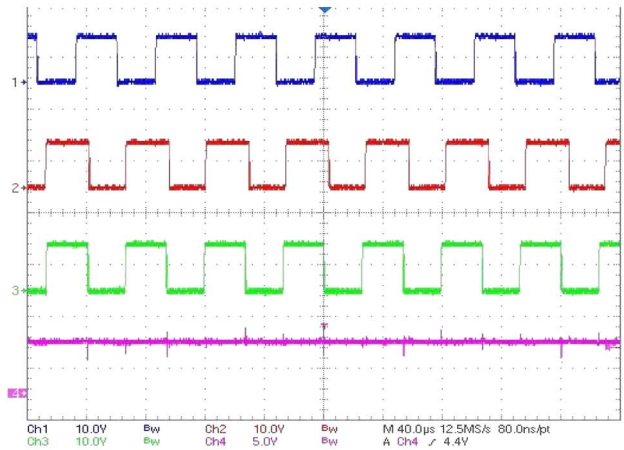
RF transmission delay, the peak load-sharing error can be reduced by reducing the master module's voltage-loop dc gain (K_v), which directly affects the current reference for the slave module. For a maximum tolerable load-sharing error of 5%, the bounds for the time-delay are shown in Fig. 5 along with the bounds for convergence and stability. This time-delay bound could vary depending on the other operating criteria of the parallel converters. Clearly, the time-delay bound for the performance criteria is the lowest and hence can be used to determine the operating delay limits of the system.

Fig. 7 shows the experimental validation of the theoretical results under a load transient condition with an RF transmission delay (τ_d) of 20 μs. We subject the master–slave converter system to a load transient; the details of which are tabulated in Table II. Fig. 7 shows the output voltage and the inductor currents of the master and two slave modules. The inductor currents of the slave modules track the corresponding signal of the master well, despite the variation in the inductance of the slave modules.

The steady-state performances of the parallel converter are shown in Fig. 8. Fig. 8(b) shows the gate-driver signals of the master and slave modules along with the output voltage. Fig. 8(a) shows that both the master and slave modules are regulated at 5 V and that the mean values of the three inductor currents are close, establishing that the master and two slave modules share the load current evenly. The ripple current of the slave modules is slightly lower (than that of the master module) because of its higher inductance.



(a)



(b)

Fig. 8. Steady-state performance of the master–slave converter system. (a) Inductor current (2 A/div) of the master (Ch1) and slave modules (Ch2 and Ch3) along with the output voltage (Ch4). We note that the input to Ch1–Ch3 (which is set at 20 mV/div) is the output of a hall-sensor current amplifier, which is set at 2 A/div. (b) Gate-driver signals (Ch1, Ch2, and Ch3) for the master and slave modules and the inverter output voltage.

IV. SUMMARY AND CONCLUSION

We demonstrate the effectiveness of an analog wireless master–slave current-sharing control of a parallel dc–dc buck converter under transient and steady-state conditions. Unlike the wireless PWM scheme described in [8], the active-current-sharing scheme, described in this paper, yields better dynamic response and mitigates the possibility of steady-state error in [8] due to RF transmitter nonlinearities. Using multiple-Lyapunov and eigenvalue approaches, this paper also analyzes the reaching conditions for orbital existence and steady-state stability, respectively, of the load-sharing converters in the presence of communication delay. Our analyses yield the time-delay bounds for stability and performance of the system. If the system operates within these prescribed bounds, the proposed control scheme can be used to achieve a high level of redundancy (of a droop method) while ensuring a satisfactory

steady-state and transient performance of wire-based active-current-sharing schemes. The proposed distributed control can be extended to multimodule parallel and networked converters as a primary or as a fault-tolerant backup control.

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