Design of an All-SiC Parallel DC/DC Weinberg Converter Unit Using RF Control

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***Abstract*—We demonstrate the feasibility of RF communication-based wireless load-sharing control of a spatially distributed two-module parallel dc/dc (Weinberg) converter unit (DDCU), each operating at a high switching frequency (0.25 MHz) and delivering an output power of 500 W. From control standpoint, we demonstrate the feasibility of wireless control scheme using a digital signal processing-field-programmable gate array (DSP-FPGA based) control–communication interface. Further, using a composite Lyapunov function methodology, we determine (in the presence of delay owing to channel disruption) the reachability of the DDCU under startup condition, and also investigate the effect of delay on orbital stability and performance. With regard to the hard-switched DDCU, we outline some practical design aspects of the high-frequency all-SiC Weinberg converter power stage and subsequently demonstrate experimentally that the DDCU achieves high efficiency in spite of operating at high frequency and high temperature, and exhibits satisfactory steady-state and transient performances despite channel separation of up to 30 ft.**

***Index Terms*—Control, dc/dc converter unit (DDCU), international space station (ISS), load sharing, network, power management and distribution unit design (PMAD), RF, reachability, SiC, stability, time delay, Weinberg converter, wireless.**

I. Introduction

ONE OF THE important building blocks of National Aeronautics and Space Administration (NASA's) power management and distribution unit design (PMAD) for powering the international space station (ISS) is the dc/dc converter unit (DDCU), as illustrated in Fig. 1 [1]. Such a DDCU needs to have parallel architecture for power scaling and system redundancy. Traditional approach to the control design of a parallel DDCU is based on decentralized droop methods [2] that offer high redundancy but at the price of often inadequate dynamic performance, or active-current-sharing methods [3] that overcome the limitations of droop methods by ensuring even distribution of currents and stresses among the modules at the price of increasing physical connections with progressively higher number of load-sharing modules.

To eliminate this problem associated with increased multiplicity of physical connections, recently, the feasibility of RF-based "*analog*" wireless control of low-frequency (20 kHz) load-sharing dc/dc buck converters was demonstrated in [4]–[7], which achieves a satisfactory compromise between conventional droop and active-current-sharing control schemes. However, for very high-frequency operation, analog implementation can suffer from drift problem that leads to pulsewidth modulation (PWM) dithering at the output of the receiver module. Further, the analog RF implementation in [7] (developed for dc/dc *non-isolated* buck converter) requires specific design for addressing the limitation of the wireless transmitter with regard to transmitting low-bandwidth control signal.

This paper outlines a DSP-FPGA-based "*fully digital*" wireless communication scheme for a two-module *isolated* Weinberg DDCU operating at one order higher switching frequency (i.e., 0.25 MHz). To analyze the effect of delay due to channel disruption at such high frequency under transient and steady-state conditions, we outline a robust analysis using composite Lyapunov-function-based methodology for reachability and orbital stability analyses. We conduct a delay analysis to ascertain the impact of reduced-rate (delayed) data transmission and channel disruption on the stability and performance of the load-sharing converter. We also demonstrate the feasibility of the parallel-converter control under such extreme conditions even at distances of 30-ft separation between the converter modules.

Further, the Weinberg DDCU module (as illustrated in Fig. 2) for ISS was developed using radiation-hardened and high-temperature SiC verticle junction FET (VJFET) and Schottky SiC diodes because harsh conditions can be detrimental to Si power devices [8]–[12]. Since there is no prior work on all-SiC Weinberg converter design, we outline the design of the SiC converter (with following parameters: input voltage = 117–173 V, output voltage = 125 V, and output power = 1 kW), and experimentally test the operation of the SiC devices at case temperatures up to 200 °C. A maximum experimental efficiency of more than 91% is obtained at the low line even at 0.25 MHz (for hard-switched operation) and for high case temperature. This is achieved by eliminating lossy snubbers [11] (because unlike Si devices, SiC devices can sustain higher breakdown voltage without compromising switch transfer efficiency [14]–[18]), reducing leakage inductances of the coupled inductor and the center-tapped transformer (that reduce the voltage spike and the associated device switching losses) by using suitably designed

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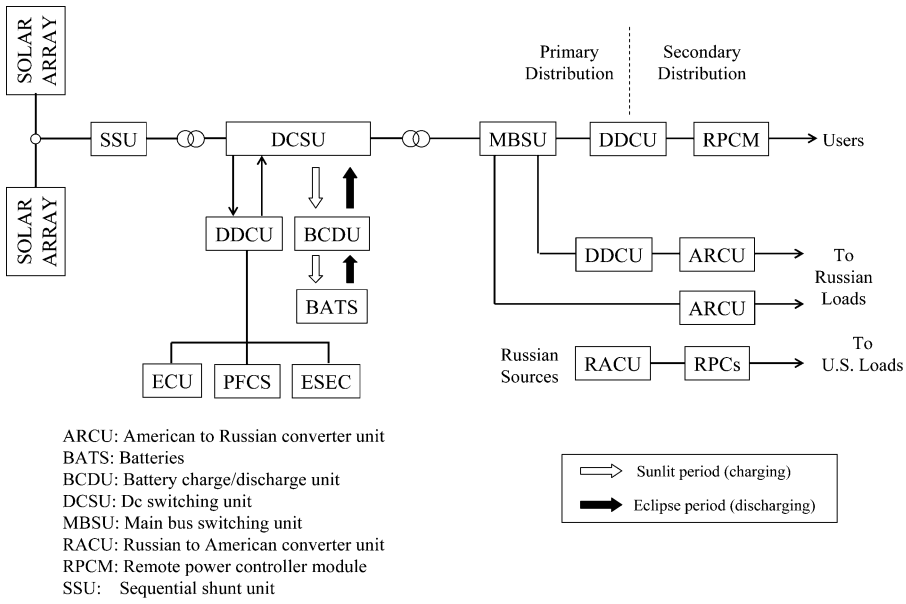


Fig. 1. Block diagram illustrating the flow of power and the placement of the DDCU.

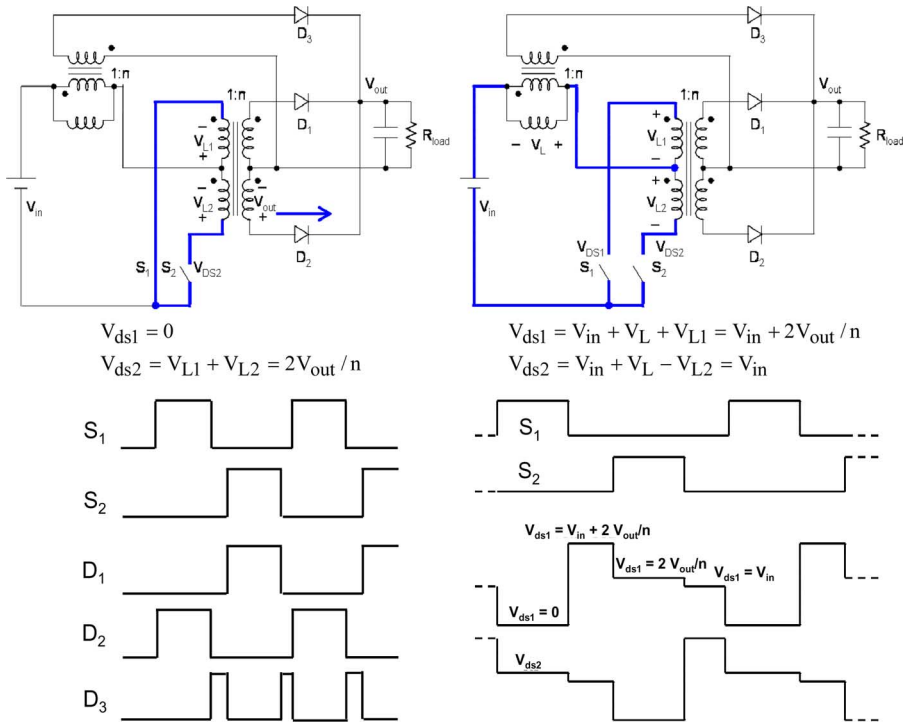


Fig. 2. Illustration of the nominal operation of the Weinberg converter and the controlled switch voltage.

planar magnetics, and due to reduced device output capacitances of SiC VJFETs and SiC Schottky diodes leading to lower switching losses.

Although the concept outlined in this paper was developed for NASA's ISS PMAD application, the potential applications of the all-SiC RF-controlled DDCU also encompass other redundant and reconfigurable power systems. The outlined concept can also be extended for high-temperature power-electronics application with low-temperature controller supported by wireless feedback and control information exchanges. This eliminates the need for developing high-temperature control electronics where Si devices are doing an excellent job. The concept outlined in this paper can be used for applications requiring isolation of low- and high-voltage elements of a power conditioning system, and distributed control and sensing.

II. All-SiC Power Stage Design and Experimental Results

Our emphasis in this section is primarily on two practical design aspects: 1) justification for SiC as opposed to competitive

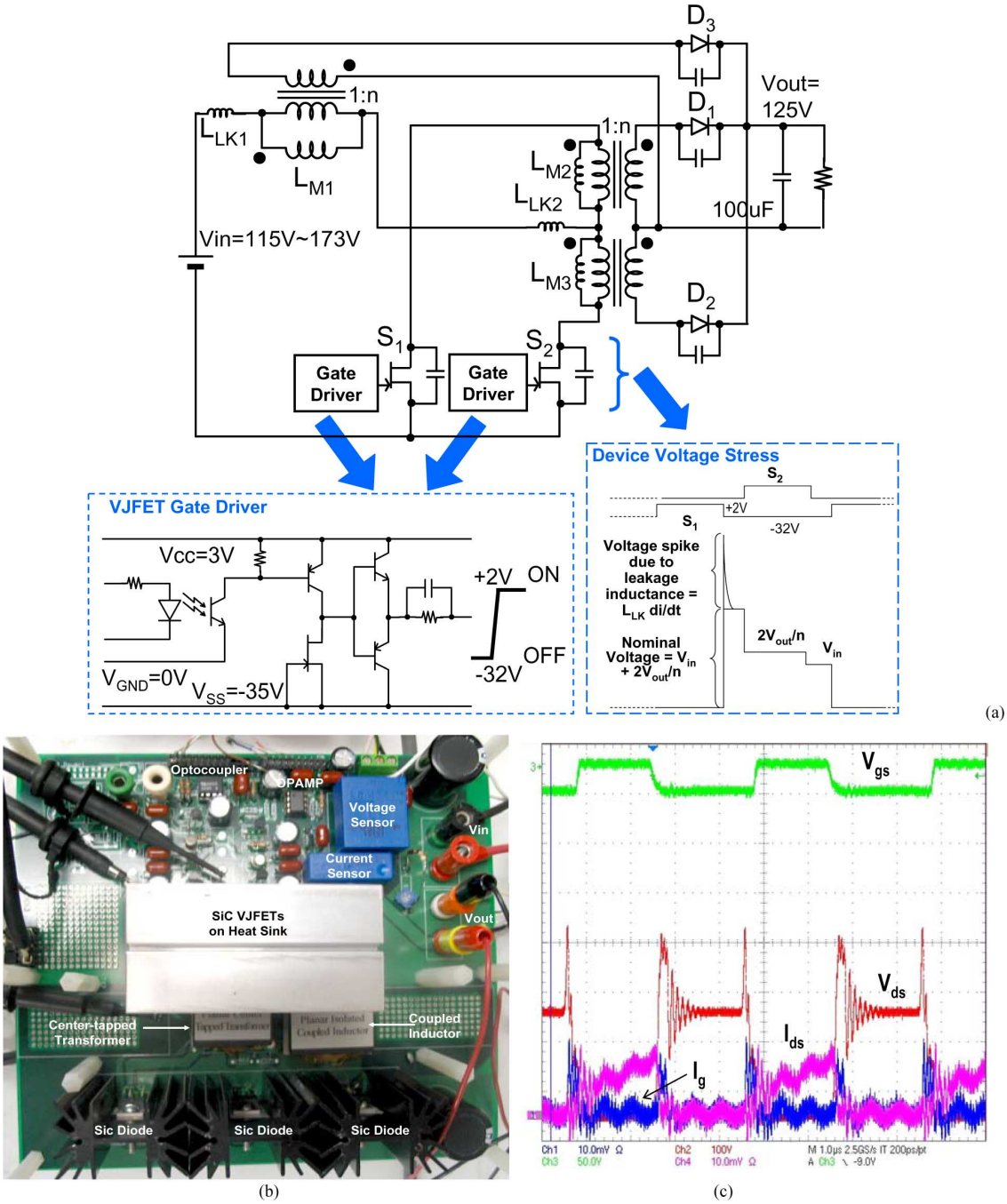


Fig. 3. (a) Topology of one practical Weinberg converter (with SiC VJFETs and Schottky diodes). The gate driver circuit has a drive capability of >1 A with $t_{\rm rise}$ and $t_{\rm fall}$ of about 25 ns and provides gate-to-source voltages of +2 and −32 V, respectively, for turn-ON and turn-OFF of the normally-ON SiC VJFET. Voltage spike across the VJFET during turn-OFF (which is the worst case condition from the standpoint of device stress in the circuit) shows difference with its nominal counterpart in Fig. 2. In addition to the nominal turn-OFF voltage, additional spike occurs as a result of leakage inductance in the transformers that interact with the VJFET output capacitance. (b) Experimental prototype of one Weinberg converter. (c) SiC gate current and voltage waveforms. (Top) Magenta—$V_{\rm gs}$ (gate-to-source voltage), Green—I_g (gate current), Cyan—$V_{\rm ds}$ (drain-to-source voltage), Yellow—$I_{\rm ds}$ (drain-to-source current). The magnitude of I_g varies from −0.78 to 1.25 A, which yields a driver loss of <5 W.

Si devices from the high-temperature and efficiency standpoint; 2) choice of the leakage inductance and its tradeoff with the breakdown voltage and mode of operation of the Weinberg converter.

We, however, begin with a brief overview of the nominal operation of the ideal Weinberg converter [19]. Fig. 2 shows the modes of operation of the converter with regard to $\rm S_1$. These two modes are repeated in an identical fashion for $\rm S_2$. Thus, while each switch operates at a frequency of f_s, the diode $\rm D_3$ operates at a frequency of $2f_s$, and so is the ripple frequency of the output. The nominal peak voltage across $\rm S_1$ or $\rm S_2$ for the maximum input voltage and the output voltage is $V_{\rm in_{max}} + 2\,(V_{\rm out}/n) = 173 + 2 \times 125/n$. However, for the practical Weinberg converter (as shown in Fig. 3), the maximum voltage across the

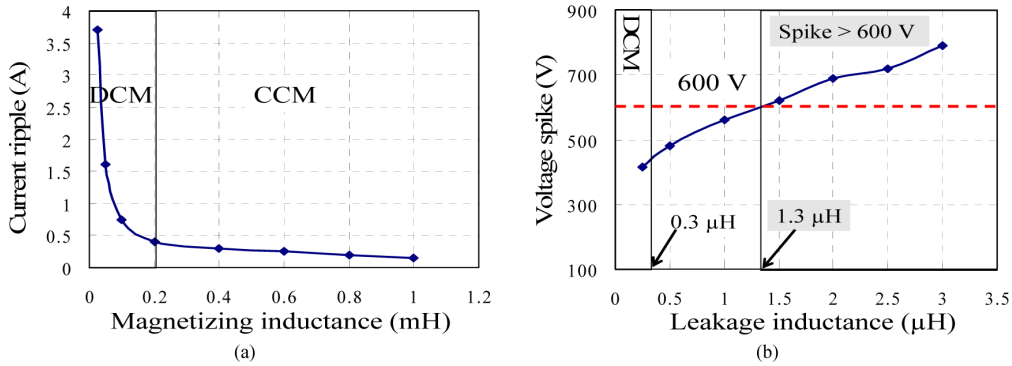


Fig. 4. (a) Simulation results illustrating the continuous- and discontinuous-modes [CCM and discrete control module (DCM)] of operation of the Weinberg converter with variation in the magnetizing inductance. For magnetizing inductance >200 μH, the converter operates in CCM. (b) Simulation results demonstrate the voltage spike across the primary-side switches with variation in the lumped leakage inductance.

TABLE I
COMPARISON OF THE ON RESISTANCES AND OUTPUT CAPACITANCES OF SiC VJFET WITH STATE-OF-THE-ART MOSFETS

Device Type	Ratings	On resistance (ohm)			Output Capacitance (pF)		
		25 °C	150 °C	200 °C	25 °C	150 °C	200 °C
SiC VJFET (SiCED)	600 V, 10 A	0.42	0.74	0.8	~ 350	~ 350	~ 350
SuperFET FCPF11N60	600 V, 11 A	0.38	0.83	N/A	~ 700	~ 700	N/A
CoolMOS SPB11N60C3	600 V, 11 A	0.38	0.95	N/A	~ 550	~ 550	N/A
CoolMOS SPW20N60S5	600 V, 20 A	0.2	0.49	N/A	~ 900	~ 900	N/A

TABLE II
BREAKUP OF PERCENTAGE POWER LOSSES OF EACH WEINBERG CONVERTER AT RATED OUTPUT POWER (500 W)

Component	V_{in} = 115 V	V_{in} = 173 V
VJFET turn on	7.1 %	2.3 %
VJFET turn off	46.2 %	63.3 %
VJFET conduction	29.5 %	15.9%
Lumped losses of diode, magnetics	17.2 %	18.5%

VJFETs (S_1 and S_2) rises beyond $V_{\mathrm{in}_{\mathrm{max}}} + 2\,(V_{\mathrm{out}}/n)$ during turn-OFF due to the lumped leakage inductance (which, in turn, depends on the coupling coefficients k and the magnetizing inductances) of the center-tapped transformer and the coupled inductor. Parametric data, obtained from simulations shown in Fig. 4(a) illustrate that the minimum magnetizing inductance required for maintaining the converter operation in continuous-conduction mode (CCM) is 200 μH. Using a coupling coefficient (k) of 0.9985, the estimated lumped-leakage inductance of the planar magnetics is 300 nH. Fig. 4(b) shows that in order to operate in CCM without exceeding the 600-V breakdown voltage of the SiC VJFET, the lumped leakage inductance should lie between 0.300 and 1.3 μH. Based on our design, we obtained a lumped leakage inductance of 510 nH (for the planar transformers), which ensures that the maximum V_{ds} is well within the breakdown voltage capability of the SiC VJFET. We note that the rated voltage of the SiC Schottky diode is 600 V, and using similar arguments as earlier, we can show that the peak voltage across the diode will be within its breakdown-voltage limit.

We now outline why the SiC VJFET best meets the efficiency requirement of the Weinberg converter, especially with regard to high-temperature operation standpoint. Table I illustrates that for similar voltage and current ratings, the SiC VJFET has a lower ON-resistance than the Si MOSFET (SuperFET FCPF11N60 [20]) at higher temperature that has clear implications for higher conduction loss. Further, the output capacitance of the Si SuperFET device is also higher, which has implications for higher switching loss. Table I also illustrates the comparison of the SiC VJFET with superjunction-structure-based Si CoolMOS (SPB11N60C3 [21]), which also has similar current and voltage ratings as that of the SiC VJFET. Once again, the ON resistance of the CoolMOS exceeds that of the SiC VJFET for higher temperatures. Further, although the output capacitance of the CoolMOS is lower than that of the Si MOSFET, it is still higher than that of the SiC VJFET. Finally, Table I also shows the comparison of a state-of-the art Si CoolMOS (SPW20N60S5 [21]), with same voltage rating but 20-A current ratings, with SiC VJFET. Since Si devices have reduced junction temperature sustenance capability, choosing a higher current rating device that yields lower ON resistance even at higher temperature is often a standard practice, particularly so since Si devices are currently cheaper than SiC VJFETs. Table I clearly shows that the ON resistance of the 20 A CoolMOS is lower than the SiC VJFET even up to 150 °C. However, the bigger device yields higher capacitance as compared to the SiC VJFET that leads to higher switching losses [18]. For the Weinberg converter under consideration, the turn-OFF switching loss (as shown in Table II) is the dominant loss for all input voltages, and hence, device capacitance is critical at 250-kHz switching frequency.

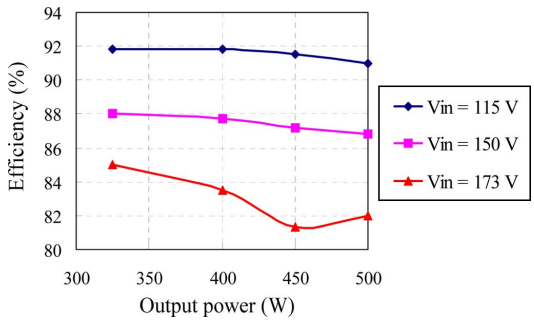


Fig. 5. Variation in the efficiency of each DDCU module with varying output power.

Using the SiC VJFET and SiC Schottky diode (SiCED 016S60 C: 600 V, 16 A), we built the experimental Weinberg converter prototype, shown in Fig. 3(b). Fig. 5 illustrates the

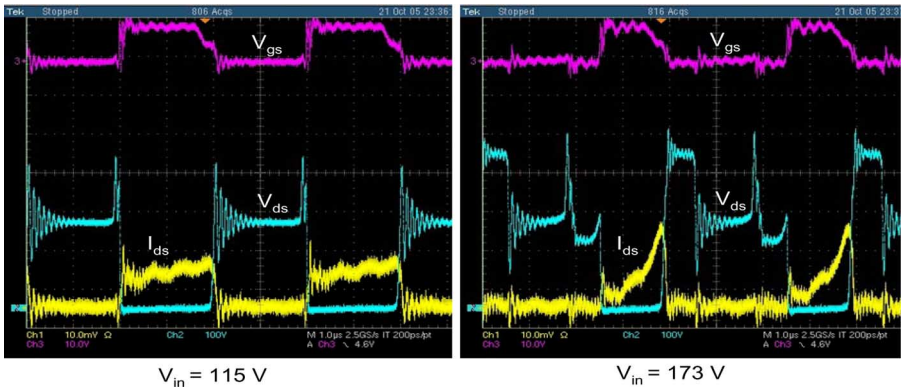


Fig. 6. Progressively higher overlap of $V_{\rm ds}$ and $I_{\rm ds}$ during turn-OFF yields higher turn-OFF loss in the Weinberg converter.

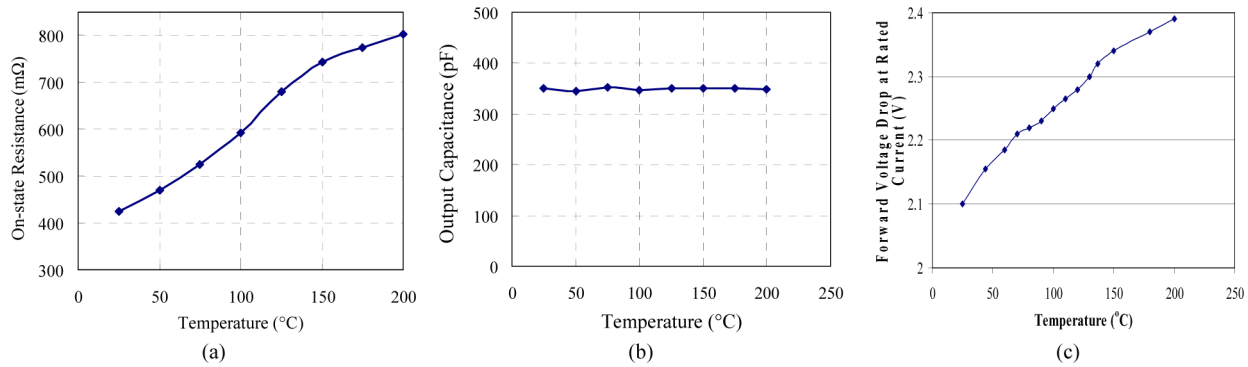


Fig. 7. Variations. (a) ON resistance. (b) Output capacitance of the SiC VJFET. (c) SiC Schottky diode forward drop with increasing case temperature. To obtain the result in (a), the SiC VJFETs are mounted on a heat sink that is placed on a hot plate to vary the case temperature. The SiC VJFETs are electrically connected to the power stage printed circuit board (PCB). ON resistance is calculated by measuring the voltage drop across the drain and source terminals of the SiC VJFET as drain-to-source current flows through it. Taking the ratio of the drain-to-source voltage drop and the drain-to-source current provides the ON resistance. To obtain the result in (b), we place the device on a hot plate (to control the case temperature) and then connect the drain and the source to the impedance analyzer 4192 A from Agilent/HP. Subsequently, we apply a negative (-25 V) voltage between the gate and the source terminals of the SiC VJFET to turn it OFF. Finally, with the device turned OFF, the impedance analyzer determines output capacitance of the SiC VJFET. To obtain the result in (c), the SiC power diodes are mounted on the heatsink, which is placed on the hot plate to vary the case temperature of the diode. Differential probes are used to measure the forward drop of the SiC diode as the case temperature is varied.

variation in the efficiency of each Weinberg converter module [Fig. 3(b)] with variation of the output power for three input voltage conditions. For $V_{\rm in} = 115$ V and $V_{\rm in} = 173$ V, the measured efficiencies are 91.4% and 81.8%, respectively, at the rated operating power. Table II shows the breakup of power losses at high- and low-input voltages. It shows that, more than half of the power loss is accrued by the switches during turn-OFF. This is because (and as illustrated in Fig. 6) during turn-OFF, $V_{\rm ds}$ transitions from 0 to $V_{\rm ds} = V_{\rm in} + 2V_{\rm out}/n$ instead of 0 to $V_{\rm in}$. Higher $V_{\rm ds}$ along with higher $I_{\rm ds}$ just before turn-OFF leads to higher turn-OFF losses. The value of $I_{\rm ds}$ just before turn-OFF is higher when $V_{\rm in} = 173$ V because the duty ratio reduces and the inductor current slope ($V_{\rm in}/L_M$) increases. Therefore, the overlap of $I_{\rm ds}$ and $V_{\rm ds}$ becomes even greater. Fig. 6 illustrates the progressively higher overlap of $V_{\rm ds}$ and $I_{\rm ds}$ with increasing input voltage leading to higher turn-OFF loss. Finally, Fig. 7 shows the impacts of increasing case temperature on the ON resistance and output capacitance of the SiC VJFET and the forward drop of the SiC diode. It clearly demonstrates that with increasing case temperatures, the switching losses of the VJFET and the conduction loss of the diode vary negligibly. The ON resistance of the VJFET does increase by a factor of 2. Overall, the converter efficiency is expected to decrease by no more than 2% for the worst case condition since the dominant loss is the turn-OFF loss.

III. Load Sharing Controller Design Using RF Wireless Network

A. Controller Description

The load-sharing controller is implemented on a digital platform, as illustrated in Fig. 8 using a DSP (TI TMS320C6713), an FPGA (Altera Flex10 K), and a wireless transceiver (Microlinear ML2722). Such an implementation has several advantages, including 1) ease of implementation of complex control schemes, 2) flexibility to realize different controller structures for different operating conditions, and 3) ability to mitigate effects of transceiver saturation, which is common in

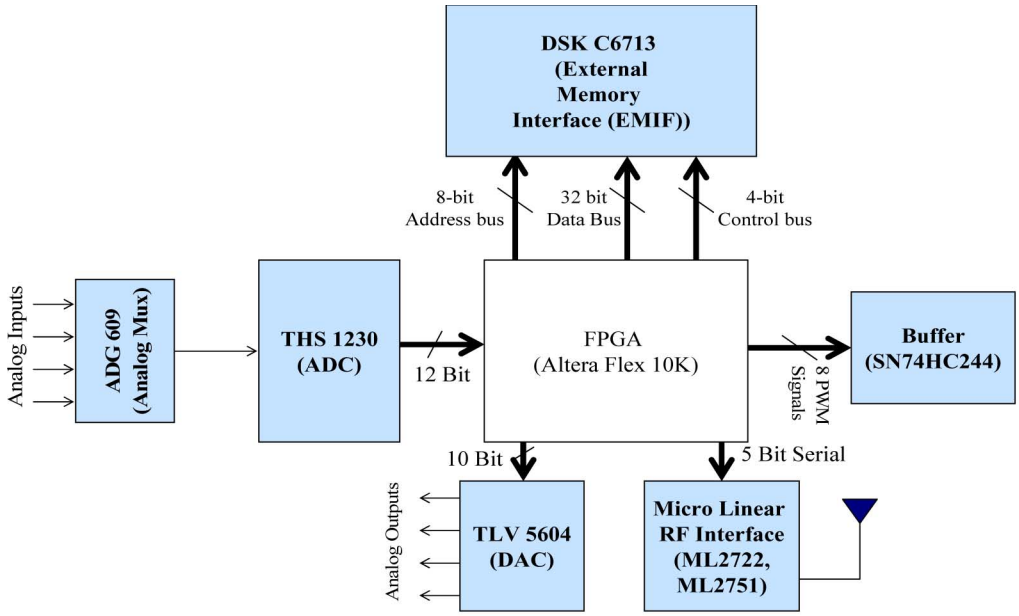


Fig. 8. (a) Architecture of the digital controller. (b) Experimental hardware for implementing the digital controller.

analog transceivers and could distort the information exchanged among the modules. We note here that at this stage, the digital controller interface is designed to be flexible enough to allow implementation of different control schemes and controller algorithms. However, eventually such a control–communication interface can and should be realized in a dedicated application-specific integrated circuit (ASIC) to reduce cost, board space, and debugging hurdles.

The overall digital controller architecture is illustrated in Fig. 8(a). The load-sharing control scheme is implemented on the DSPs of the two modules, while the PWM signal generation for the converter switches and the voltage- and current-sensor interfaces for each module are implemented on the FPGA. For wireless communication, the protocol for medium access control (MAC) layer [22] is implemented in the DSP while the transmitter power control [22] is realized in the FPGA. The size of the transmitted packet is 24 bits (for 12-bit control variable that is exchanged among the modules). Finally, Fig. 8(b) illustrates the hardware implementation, where all the key digital controller blocks have been identified.

One of the problems with wireless control is packet drop that results in discontinuous communication between the master and slave, as illustrated in Fig. 9(a). The slave is out of synchronization and the master needs to support the additional current for the time when the data is lost. It was observed that the data is disrupted when the transmitter IC does a phase lock loop update every 100 ms. The disruption lasts for about 150 μs. Such a data can have an adverse impact on the load sharing performance of the parallel converters, as shown in Fig. 9(b). To overcome this problem, a threshold level on the data received by the slave module is set. If the incoming data exceeds this threshold level, the data packet is discarded and the load-sharing data from the

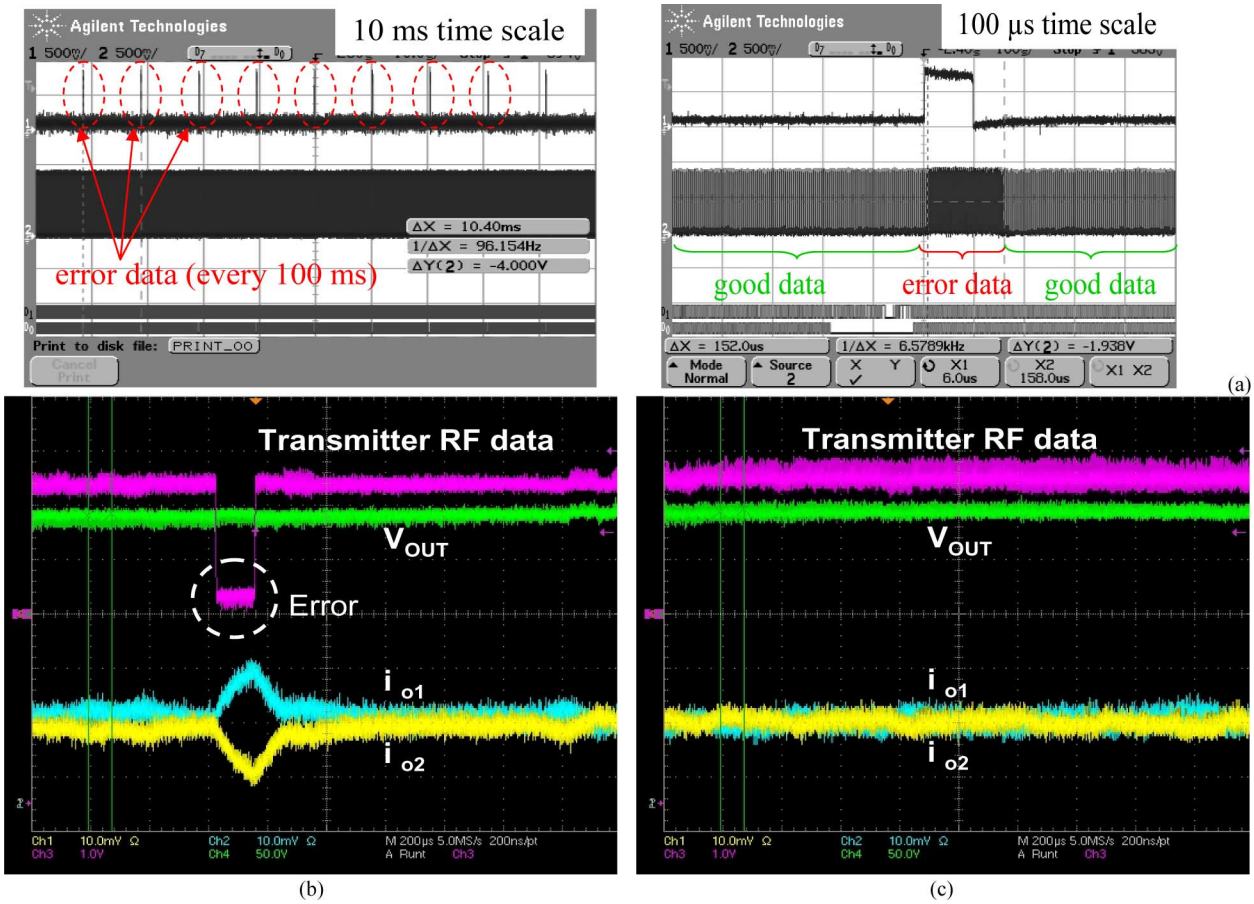


Fig. 9. (a) Discontinuous communication between the master and slave due to lack of synchronization. (b) Case when the received data is used by the slave controller without any changes leading to load-sharing error. (c) Case where data limiting ensures that the received data (before channel disruption) is used by the slave controller in case the current received data exceeds a threshold level. This yields satisfactory current sharing.

previous sample is used instead. Fig. 9(c) shows a much improved load sharing between the master and slave. However, this data-limiting scheme introduces an additional time delay in the load-sharing information at the receiver apart from the delay due to the transmission channel and due to processing of the data to be communicated at the transceiver and the receiver nodes. Therefore, in the next section, we study the impacts of time delay on the stability and performance of the overall system.

B. Impacts of Time Delay on System Stability and Performance

In this section, we investigate the impacts of time delay on the global stability and performance of the system. Global stability analyses involve determining the reaching conditions for orbital existence (which determines whether the error trajectories of the system converge to an orbit from an arbitrary initial condition) [23], [24] and the stability of the nominal (corresponding to the switching period) steady state orbit [24], [25].

Fig. 10 illustrates the control block diagram of the Weinberg converter. The state-space piecewise linear (PWL) model of the closed-loop parallel Weinberg converter is described by

$$\dot{X} = A_{0i}X + A_{1i}X\left(t - \tau_D\right) + B_i \qquad (1)$$

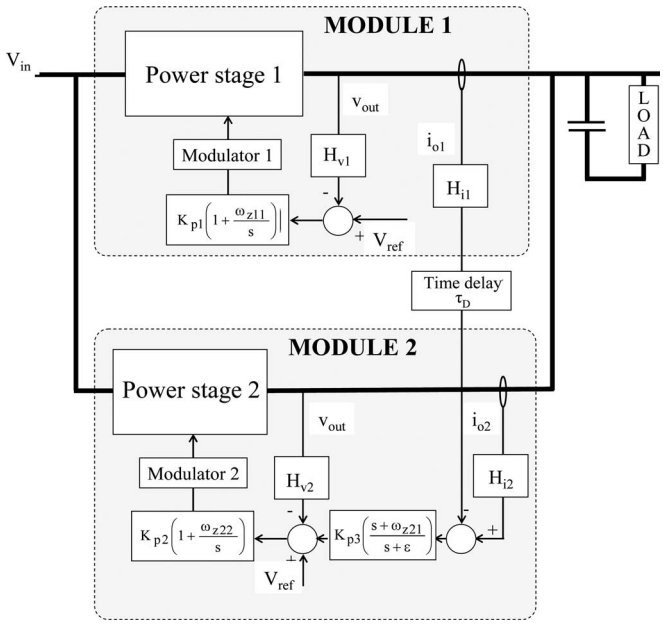
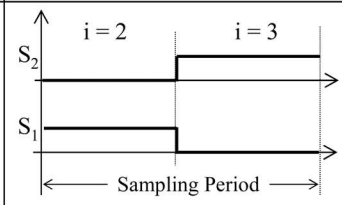
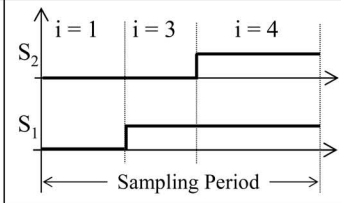
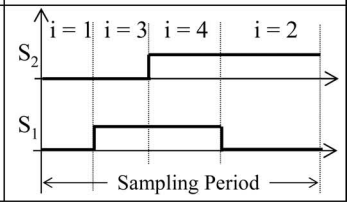


Fig. 10. Schematic illustrating the control block diagram of the load-sharing Weinberg converter [each module shown in Fig. 3(a)]. Symbol τ_D represents the time delay due to RF communication between the two nodes.

TABLE III
POSSIBLE SWITCHING SEQUENCES OF THE LOAD-SHARING WEINBERG CONVERTERS

Number of States in a Sequence	Switching Sequences				Total Number of Feasible Sequences	Illustration
	First Switching State	Second Switching State	Third Switching State	Fourth Switching State		
2	(i = 1)	(i = 4)			2	
	(i = 2)	(i = 3)				
3	(i = 1)	(i = 2)	(i = 3)		4	
	(i = 1)	(i = 2)	(i = 4)			
	(i = 1)	(i = 3)	(i = 4)			
	(i = 2)	(i = 3)	(i = 4)			
4	(i = 1)	(i = 3)	(i = 4)	(i = 2)	1	

where i represents the switching state of the system and τ_D represents the end-to-end delay due to wireless communication. In (1), $X = [\, i_{L1} \quad i_{L2} \quad v_C \quad \xi_1 \quad \xi_2 \quad \xi_3 \quad \xi_4 \quad \xi_5 \quad \xi_6 \quad \xi_7 \,]^T$, A_{0i}, A_{1i} are matrices, and B_i is a column vector. The definitions of all the matrices and the values of system parameters are given in Appendix. Here, i_{L1}, i_{L2}, and v_c are the coupled-inductor magnetizing currents of each module and the output capacitor voltage, and ξ_1, ξ_2, ξ_3, ξ_4, ξ_5, ξ_6, ξ_7 represent the controller states.

The reaching conditions for orbital existence of the system (1), which is described in [23] and [24], depends on the number of nonrepetitive and nonredundant switching sequences. For the load-sharing Weinberg converter, the possible switching states are: ($i = 1$, $\mathrm{S}_1 = 0$, and $\mathrm{S}_2 = 0$); ($i = 2$, $\mathrm{S}_1 = 1$, and $\mathrm{S}_2 = 0$); ($i = 3$, $\mathrm{S}_1 = 0$, and $\mathrm{S}_2 = 1$); and ($i = 4$, $\mathrm{S}_1 = 1$, and $\mathrm{S}_2 = 1$). Here, S_1 and S_2 are the switching functions of the two Weinberg converter modules. The total number of possible nonrepetitive and nonredundant switching sequences generated due to these switching states [when the converters are operating in channel control module (CCM)] can be evaluated using Table III. Here, we neglect the case where only one switching state occurs within a switching cycle because such a condition would result in transformer saturation due to volt–second imbalance. From Table III, we observe that the number of feasible nonrepetitive and nonredundant sequences for the case where two switching states occur within a switching cycle is two, and for three switching states and four switching states in one switching cycle, it is four and one, respectively. Therefore, the total number of feasible nonrepetitive and nonredundant switching sequences for the case of the load-sharing Weinberg converter is $M = 7$.

To determine the reaching condition of (1), we define a positive-definite composite Lyapunov function [23], [24]

$$V_k\,(e) = \sum_{i=1}^{h} \alpha_{ki} e^T P_{ki} e, \qquad k = 1, 2, \ldots, M \tag{2}$$

where $0 \le \alpha_{ki} \le 1$ and $\sum_{i=1}^{h} \alpha_{ki} = 1$. In (2), k represents a particular switching sequence and h represents the number of switching states in a given switching sequence. The system described by (1) is globally stable provided that $d/dt\,(V_k\,(e)) < 0$, which is ensured provided the following matrix inequality is satisfied [23] for any $\gamma > 0$, $p > 1$:

$$\sum_{i=1}^{h} \alpha_{ki} \begin{bmatrix} G_{ki} & P_{ki}A_{1i}A_{0i} & -P_{ki}A_{1i}^2 & P_{ki}\bar{B}_i \\ -A_{0i}^T A_{1i}^T P_{ki} & -\gamma p P_{ki} & 0 & 0 \\ -\left(A_{1i}^2\right)^T P_{ki} & 0 & -\gamma P_{ki} & 0 \\ \bar{B}_i^T P_{ki} & 0 & 0 & 0 \end{bmatrix} < 0 \tag{3}$$

where $G_{ki} = 1/\tau_D[(A_{0i} + A_{1i})^T P_{ki} + P_{ki}(A_{0i} + A_{1i})] + (\gamma p + \gamma) P_{ki}$ and $\bar{B}_i = -\,(A_{0i} + A_{1i})\,X^* + B_i$ (X^* is the desired values of the states). By varying τ_D in (3), we can determine the reaching conditions for orbital existence for different network operating conditions. Stability of the nominal orbit can be evaluated by investigating the change of (2) over the nominal time period (for this case, it is the switching time period). The nominal orbit is stable provided that $d/dt\,(V_k\,(e)) = 0$. By

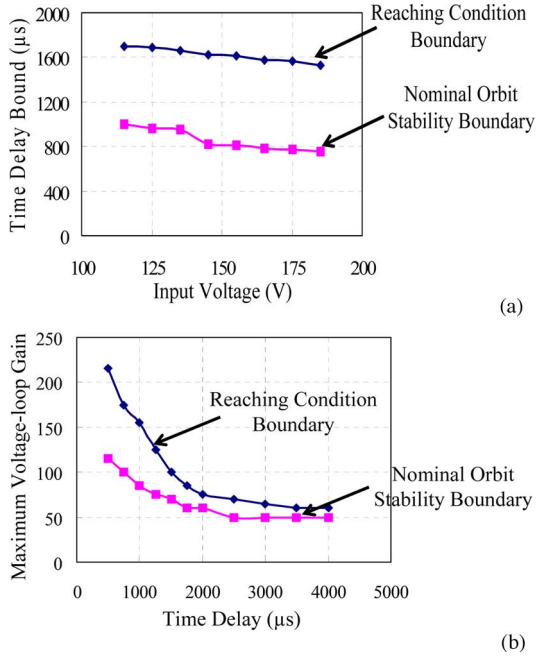


Fig. 11. (a) Variation of the maximum values of time delay that can be sustained by the system (1) while ensuring that the reaching condition for orbital existence is satisfied and the nominal steady state orbit is stable. (b) Variation of the maximum value of voltage loop gain that can be allowed for a given time delay.

equating the left-hand side of (3) to zero, the condition for stability of the nominal orbit can be expressed as

$$\sum_{i=1}^{h} \alpha_{ki} \begin{bmatrix} G_{ki} & P_{ki}A_{1i}A_{0i} & -P_{ki}A_{1i}^2 & P_{ki}\bar{B}_i \\ -A_{0i}^T A_{1i}^T P_{ki} & -\gamma p P_{ki} & 0 & 0 \\ -\left(A_{1i}^2\right)^T P_{ki} & 0 & -\gamma P_{ki} & 0 \\ \bar{B}_i^T P_{ki} & 0 & 0 & 0 \end{bmatrix} = 0 \tag{4}$$

where P_{ki} are positive-definite matrices and α_{ki} is obtained using the numerical search algorithm. If there are no positive-definite matrices P_{ki} that satisfy (4), we conclude that the nominal orbit is unstable. We note that unlike the conventional map-based approach [25], which ascertains stability of (1) using a map that is derived by sequential patching of solutions corresponding to the ith state, and hence, requires the knowledge of the modulation scheme, the composite Lyapunov-function-based approach depends only on the switching states of the nominal sequence. Even if the nominal sequence changes (e.g., due to a change in the modulation scheme), (4) is true as long as the switching states in the sequence are the same.

Fig. 11(a) illustrates the maximum values of time delay that can be sustained by the system (while satisfying (3) and (4), respectively) for input voltage variation from 115 to 173 V. Clearly, higher time delays can be sustained by the system as the input voltage reduces. The variation of the maximum allowable voltage-loop gain (K_{p1} and K_{p2}) with time delay is illustrated in Fig. 11(b). For Fig. 11(b), the input voltage is 173 V. Fig. 11(a) and (b) can be used to design the controller parameters depending on the operating requirements of the system. Fig. 12 shows the effects of time delay on two performance parameters of the system, namely the ringing voltage amplitude and settling time. Clearly, time delay has an adverse effect on the system performance.

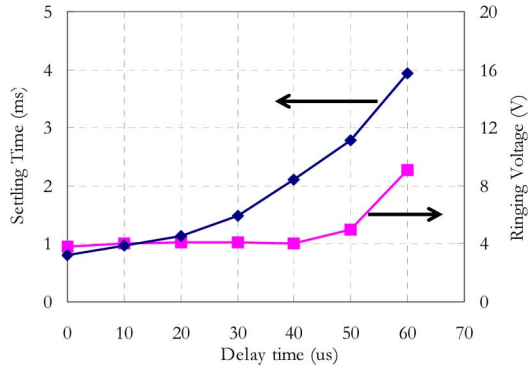


Fig. 12. Variation of the settling time and magnitude of output voltage ringing with variation of the time delay.

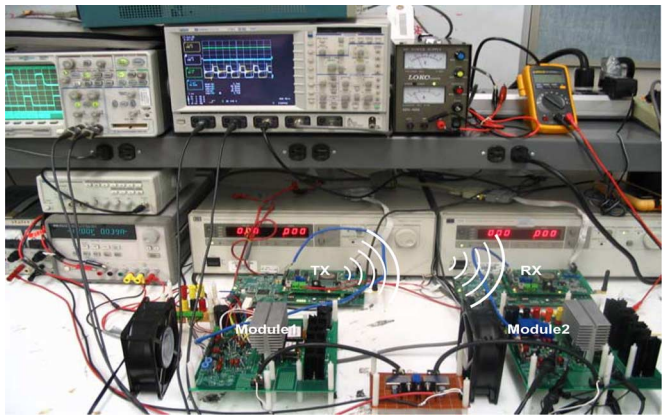


Fig. 13. Experimental setup of the load-sharing converter, where control information is exchanged between the master (left) and slave (right) modules using RF-based communication.

C. Experimental Results

Fig. 13 shows the experimental setup of a two-module parallel Weinberg converter, where the control system is designed using the procedure outlined earlier and the power stage design has been described in Section II. Fig. 14 shows that the startup response (0–1000 W), steady state response (1000 W), and a transient response (625–1000 W) of the RF-controlled load-sharing converter (all at $V_{\rm out} = 125$ V and $V_{\rm in} = 117$ V with a channel distance of three feet) are satisfactory. In Fig. 15, we demonstrate that the dynamic and steady state performances of the system are satisfactory even with a channel distance as high as 30 ft. It clearly shows equal current sharing during and after the load transient. Further, in Fig. 15(b), we show that the channel distance does not have any adverse effect on the overall efficiency of the parallel Weinberg converter.

Fig. 14. Start-up, steady state, and transient responses of the load-sharing converters for a channel separation of 3 ft.

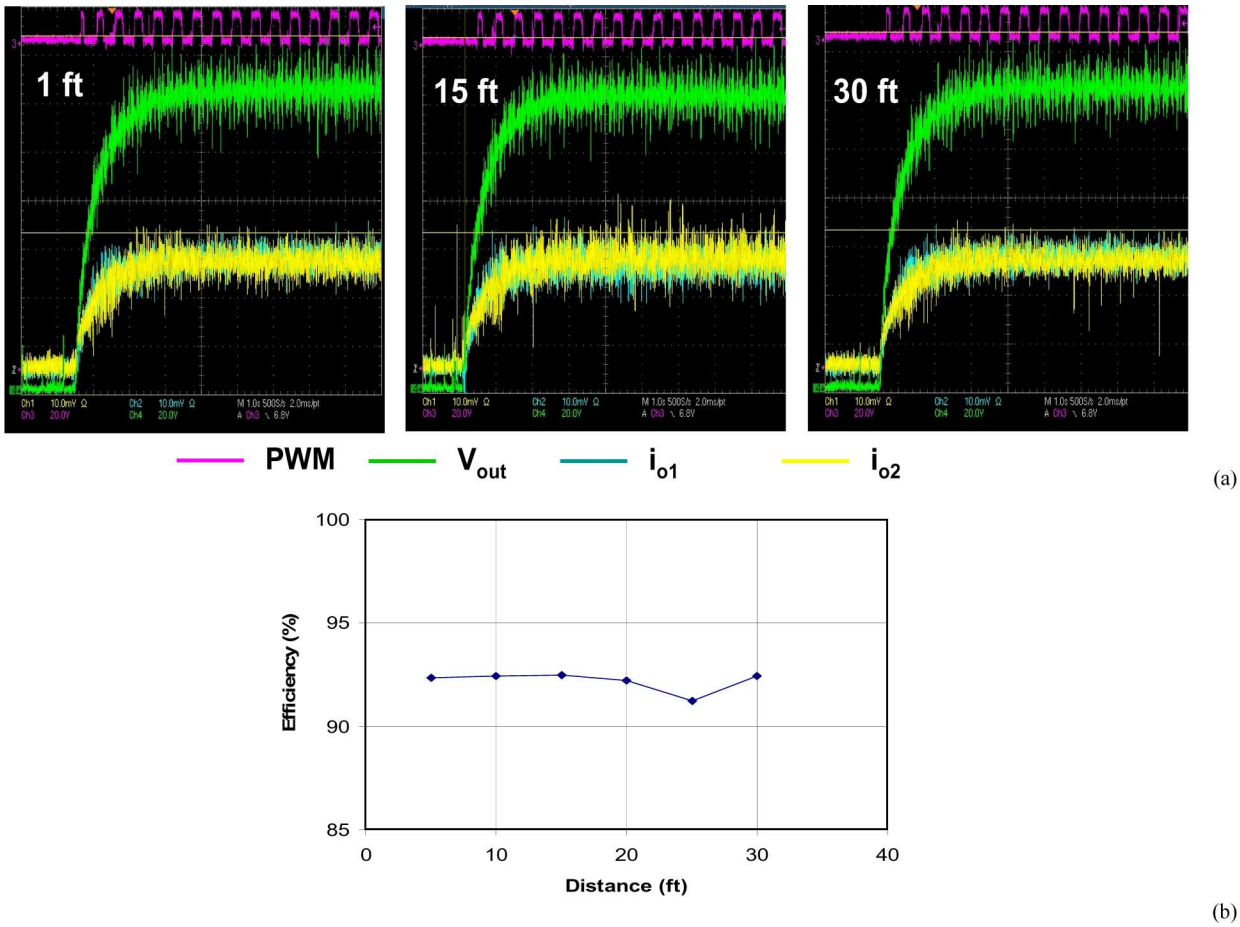


Fig. 15. (a) Dynamic performance of the system even for channel separations (distance between the antenna of the master and the slave module) of 1, 15, and 30 ft. (b) Variation of the efficiency of the parallel Weinberg converter (at rated power) with channel distance.

IV. Summary and Conclusion

To address DDCU application of NASA's international space station (ISS), the Weinberg converter is developed using 600 V SiC VJFET and Schottky diodes. This eliminated the need for snubbers without compromising switching losses for the same breakdown voltage. Further, SiC VJFET yields a smaller device capacitance and ON resistance than its Si counterpart of similar ratings, which yields lower switching loss (that happens to be the dominant loss component for the application under consideration) and conduction losses. Consequently, and due to the tightly controlled leakage inductance of the high-frequency planar magnetics, the hard-switched converter achieves a maximum efficiency of 91.4% with a total output power of 1 kW. Further, since the experimentally measured device capacitance of the SiC VJFET and the forward drop of the SiC Schottky

diode vary negligibly even at high case temperature (200 °C), the efficiency of the converter is expected to drop by no more than 2% even at such high temperature since the only additional drop will be due to the conduction loss of the VJFET since its ON resistance approximately doubles at 200 °C. Moreover, the maximum operating temperature (200 °C) of the current commercial SiC-based devices is due to packaging limitations. As such, the core SiC VJFET device can be operated at much higher temperature. So, as the packaging improves, it can be anticipated that the maximum operating device temperature will improve as well. Of course, with Si devices, operation at such high case temperature is infeasible. A way around that problem, which is usually adopted, is to choose an Si device of larger current rating that yields lower ON resistance. However, such a device will have a large device output capacitance (as illustrated in Table I), which, in turn, will increase the switching loss. Since the device output capacitance varies negligibly with temperature while the ON resistance increases for the same variation in temperature, the overall efficiency will reduce far more than the SiC counterpart since for the present application, switching loss is the dominant component.

We have designed and evaluated the performance of a parallel DDCU, comprising two-high frequency (0.25 MHz) Weinberg converter modules that are controlled in a distributed manner by exchanging control information over a wireless communication link. The RF controlled distributed control scheme is able to regulate the output voltage at 125 V under steady state and dynamic conditions for input voltage varying between 117 and 173 V. A stability analysis of this delay-dependent control system based on the nonlinear switching model of the Weinberg converter was carried out to select suitable controller gains and time-delay limits. It was observed that, as the input voltage increases, the reachable and stability regions marginally reduce for the same time delay incurred due to wireless transmission. Overall, the experimental performance of the load-sharing converter under startup, steady state, and load- transient conditions was found satisfactory even for channel distance even up to 30 ft. It was also observed that the channel distance does not have any adverse effect on the overall efficiency of the parallel Weinberg converter. Moving forward, addressing the issue related to mitigation of intentional channel disruption is a priority with regard to security. Another option that will be considered is the feasibility of a rotating master–slave control scheme (using single-/multiple-antenna architecture) instead of a dedicated master–slave control to address robustness versus speed tradeoff.

TABLE IV
PARAMETERS OF EACH MODULE OF THE DDCU

Power Stage		Controller	
Parameter	Nominal value	Parameter	Nominal value
Inductance, L	500 μH	Voltage sensor gain, H_{v1} and H_{v2}	0.024
Capacitance, C	100 μF	Current sensor gain, H_{i1} and H_{i2}	0.75
Transformer turns ratio, n	1.2	Voltage loop gain, K_{p1}, and K_{p2}	100
Rated Power	1 kW	Current loop gain, K_{p3}	10
		Voltage loop zeros, ω_{z11}, and ω_{z22}	100
		Current loop zero, ω_{z21}	1000

APPENDIX

DEFINITION OF THE MATRICES IN (1)

The definitions of the matrices of the state-space equation of the Weinberg converter, described in (1), are given by, A_{0i}, as shown at the bottom of this page

$$A_{1i} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -H_{i1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad \forall i$$

$$B_1 = [0 \quad 0 \quad 0 \quad V_{\text{ref}} \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0]^T$$

$$B_2 = \left[{}^1\!/_L \quad 0 \quad 0 \quad V_{\text{ref}} \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \right]^T$$

$$B_3 = \left[0 \quad {}^1\!/_L \quad 0 \quad V_{\text{ref}} \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \right]^T$$

and

$$B_4 = \left[{}^1\!/_L \quad {}^1\!/_L \quad 0 \quad V_{\text{ref}} \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \right]^T.$$

The various parameters of the DDCU are given in Table IV.

$$A_{0i} = \begin{bmatrix} 0 & 0 & -{}^1\!/_{nL} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -{}^1\!/_{nL} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ {}^1\!/_C & {}^1\!/_C & -{}^1\!/_{RC} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -H_{i2} & 0 & -K_{p1} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -H_v & 0 & K_{p2}\omega_{z11} & \varepsilon & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & \varepsilon & 0 & 0 & 0 \\ 0 & 0 & -H_v & 0 & 0 & 0 & 0 & -(\omega_{z22}+\omega_{z21}) & K_{p3}\omega_{z22}\omega_{z21} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & \varepsilon \end{bmatrix} \quad \forall i$$

REFERENCES

[1] E. B. Gietl, E. W. Gholdston, B. A. Manners, and R. A. Delventhal. (2000). "The electric power system of the international space station—A platform for power technology development," NASA Tech. Rep. TM-2000—210209 [Online]. Available: http://gltrs.grc.nasa.gov/cgi-bin/GLTRS/browse.pl?2000/TM-2000–210209.html

[2] C. Jamerson and C. Mullett, "Parallel supplies via various droop methods," in *Proc. High Freq. Power Convers. Conf.*, 1994, pp. 68–76.

[3] V. J. Thottuvelil and G. C. Verghese, "Stability analysis of parallel dc/dc converters with active current sharing," in *Proc. IEEE Power Electron. Spec. Conf.*, 1996, pp. 1080–1086.

[4] S. K. Mazumder, K. Acharya, and M. Tahir, "Wireless control of spatially distributed power electronics," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2005, pp. 75–81.

[5] S. K. Mazumder, M. Tahir, and S. L. Kamisetty, "Wireless PWM control of a parallel dc/dc buck converter," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1280–1286, Nov. 2005.

[6] K. Acharya, S. K. Mazumder, and M. Tahir, "Fault-tolerant wireless network control of load-sharing multiphase interactive power network," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2006, pp. 1167–1174.

[7] S. K. Mazumder, M. Tahir, and K. Acharya, "Master–slave current-sharing control of a parallel dc/dc converter system over an RF communication interface," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 59–66, Jan. 2008.

[8] K. Shenai, K. F. Galloway, and R. D. Schrimpf, "The effects of space radiation exposure on power MOSFETs: A review," *World Sci. Publishing*, vol. 14, no. 2, pp. 445–463, 2004.

[9] Y. Sugawara, "Recent progress in SiC power device developments and application studies," in *Proc. Power Semicond. Devices ICs Conf.*, 2003, pp. 10–18.

[10] A. Elasser and T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proc. IEEE*, vol. 90, no. 6, pp. 969–986, Jun. 2002.

[11] V. R. Garuda, M. K. Kazimierczuk, M. L. Ramalingam, L. Tolkkinen, and M. D. Roth, "High temperature testing of a buck converter using silicon and silicon carbide diodes," in *Proc. Energy Convers. Eng. Conf.*, 1997, pp. 1561–1567.

[12] B. J. Baliga, "Trends in power semiconductor devices," *IEEE Trans. Electron Devices*, vol. 43, no. 10, pp. 1717–1731, Oct. 1996.

[13] J. E. Bruemmer, F. R. Williams, and G. V. Schmitz, "Efficient design in a dc to dc converter unit," in *Proc. IEEE Intersoc. Energy Convers. Eng. Conf.*, 2002, pp. 56–60.

[14] P. Bhatnagar, N. G. Wright, A. B. Horsfall, C. M. Johnson, M. J. Uren, K. P. Hilton, A. G. Munday, and A. J. Hydes, "High temperature applications of 4 H-SiC vertical junction field-effect transistors and Schottky diodes," *Trans. Tech. Publ., Mat. Sci. Forum*, vol. 556–557, pp. 987–990, 2007.

[15] M. Chinthavali, B. Ozpineci, and L. M. Tolbert, "High temperature and high frequency performance evaluation of of 4 H-SiC VJFET and Schottky diodes," in *Proc. IEEE Appl. Power Electron. Conf.*, 2005, pp. 322–328.

[16] T. Funaki, J. C. Balda, J. Junghans, A. S. Kashyap, H. A. Mantooth, F. Barlow, T. Kimoto, and T. Hikihara, "Power conversion with SiC devices at extremely high ambient temperatures," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1321–1329, Jul. 2007.

[17] W. Wondrak, R. Held, E. Niemann, and U. Schmid, "SiC devices for advanced power and high-temperature applications," *IEEE Trans. Ind. Electron.*, vol. 48, no. 2, pp. 307–308, Apr. 2001.

[18] D. Stephani and P. Friedrichs, "Silicon carbide junction field effect transistors," *Int. J. High Speed Electron. Syst.*, vol. 16, no. 3, pp. 825–854, 2006.

[19] A. Weinberg and J. Schreuders, "A high power high voltage dc/dc converter for space applications," in *Proc. IEEE Power Electron. Spec. Conf.*, 1985, pp. 317–329.

[20] [Online]. Available: http://www.fairchildsemi.com/ds/FC/FCPF11N60.pdf

[21] [Online]. Available: http://www.infineon.com/cms/en/product/channel.html?channel=ff80808112ab681d0112ab6a628704d8

[22] M. Tahir and S. K. Mazumder, "Markov chain model for performance analysis of transmitter power control in wireless MAC protocol: Towards delay minimization in power-network control," in *Proc. IEEE 21st Int. Conf. Adv. Inf. Netw. Appl. (AINA 2007)*, Niagara Falls, ON, Canada, May 21–23, pp. 909–916.

[23] S. K. Mazumder and K. Acharya, "Multiple Lyapunov function based reaching condition analyses of switching power converters," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2006, pp. 2232–2239.

[24] S. K. Mazumder and K. Acharya, "Global stability analyses of switching power converters," (Tutorial), in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2007, pp. 1981–1987.

[25] S. K. Mazumder, A. H. Nayfeh, and D. Boroyevich, "Theoretical and experimental investigation of the fast- and slow-scale instabilities of a dc/dc converter," *IEEE Trans. Power Electron.*, vol. 16, no. 2, pp. 201–216, Mar. 2001.

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