A Soft-Switching Scheme for an Isolated DC/DC Converter With Pulsating DC Output for a Three-Phase High-Frequency-Link PWM Converter

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***Abstract*—This paper outlines a soft-switching mechanism based on zero-voltage-zero-current-switching (ZVZCS) principle for the front-end isolated dc/dc converter of an isolated three-phase rectifier-type high-frequency-link bidirectional power converter. In conjunction with a back-end dc/ac converter operating with a novel patent-filed hybrid modulation scheme outlined in [1], [2], and [21] that reduces the number of hard-switched commutation per switching cycle, the proposed ZVZCS scheme can lead to less overall switching losses than other conventional switching schemes. The proposed ZVZCS scheme is effective for various load conditions, operates seamlessly with a simple active-clamp circuit, and is suitable for applications where low-voltage dc to high-voltage three-phase ac power conversion is required.**

***Index Terms*—High-frequency link, isolated three-phase converter, soft switching, zero-voltage-zero-current-switching (ZVZCS).**

I. Introduction

HIGH-EFFICIENCY, low cost, and high power density are important attributes of a low-input-voltage three-phase converter (fed with a low-voltage dc source) such as battery-based three-phase uninterruptible power supply, naval bidirectional power conversion modules, fuel-cell-powered electric motor drive, or distributed generation systems with renewable energy sources. Galvanic isolation is typically mandatory for safety concerns and voltage and current scalability, and in that regard, a high-frequency-transformer-based approach can be a preferable choice from the standpoint of weight, footprint, and cost reduction. Among all possible topologies, a high-frequency-link (HFL) pulsewidth-modulated (PWM) converter can eliminate the intermediate *LC* filter that is needed for a conventional high-frequency (HF) fixed-dc-link converter approach [27]. Further, as compared to a resonant-link inverter, it yields lower switch stress, better total harmonic distortion THD, and simpler all-device structure (i.e., no passive components in power stages). Thus, the PWM HFL converter approach is better suited from the viewpoint of cost, efficiency, and portability.

Two typical HFL converter topologies have been proposed in the literature. One is the cycloconverter-type HFL converter, which reduces the conversion complexity by directly placing a three-phase PWM cycloconverter to the secondary side of an HF transformer [3]–[10], [28], [29]. The other is the rectifier-type HFL (RHFL) converter, which possesses a structure similar to that of a conventional fixed-dc-link converter except for the absence of the dc-link filter [2], [11]–[15]. Although the RHFL converter comprises an extra rectifier stage, overall, it requires less number of switches since it does not need to handle bidirectional voltage. A typical three-phase RHFL converter is plotted in Fig. 1. It comprises two full bridges (Bridges I and II) as the front-end followed by an HF transformer and a dc/ac full bridge (Bridge III) as the final stage. The voltage-source-inverter (VSI)-like structure provides inherent freewheeling paths in Bridge III, which simplifies its switching scheme precluding the possibility of disruption of the load current due to open circuit. Furthermore, the auxiliary circuit, which is commonly used in an HFL converter to recover the transformer leakage energy and/or to limit the secondary side overvoltage, can be simplified. Nevertheless, RHFL converters may suffer from additional switching losses because of three-stage HF operation.

To address this problem, several switching schemes have been proposed for achieving soft switching without using any additional component. The conventional method is to implement a square-wave modulation on Bridges I and II, and apply one of the many well-established continuous sine-wave modulation schemes to Bridge III. All associated switches on Bridges I and II are turned on and off during the zero-vector intervals of Bridge III to achieve zero-current switching (ZCS). The normally used schemes for Bridge III are continuous sinusoidal PWM (SPWM) and space-vector modulation (SVM) [6], [12], [14]. However, Bridge III still experiences significant switching losses owing to the usage of slow-speed high-voltage semiconductor devices that operate under hard-switching conditions. Some discontinuous-modulation schemes, which were originally proposed for fixed-dc-input VSI, can be utilized for Bridge III to partially reduce its switching losses by allowing no switching on one of its three legs [25], [26]. The ZCS of front-end bridges is still applicable. A novel hybrid modulation, if applied to Bridge III, can further reduce its switching losses by allowing no switching on two of its three legs [21]. Unfortunately, this

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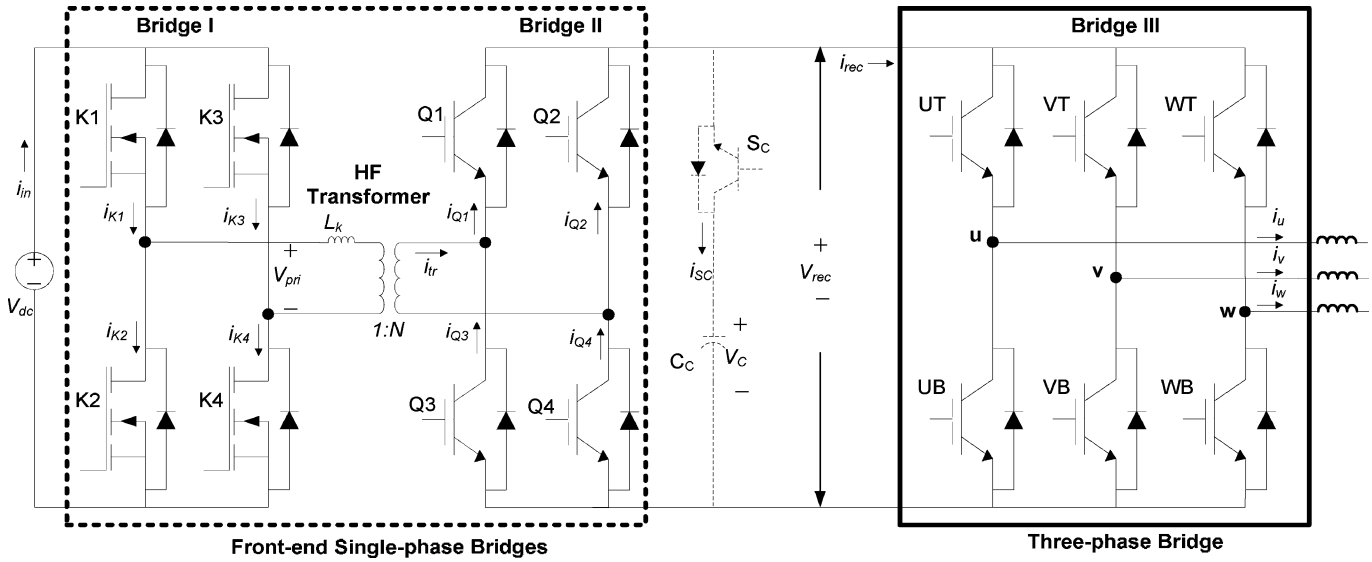


Fig. 1. Schematic of a typical RHFL converter suitable for low-voltage dc to high-voltage ac conversion.

method violates the ZCS condition for the front-end switches and may cause high switching losses on Bridges I and II.

This paper proposes a soft-switching scheme that can reduce the switching losses for the front-end isolated dc/dc converter of the RHFL converter (as shown in Fig. 1). It enables ZVZCS for all switches on two front-end bridges and ZVS for switches on Bridge III without using any additional component or polarity sensing. In conjunction with the hybrid modulation for Bridge III, the proposed ZVZCS scheme can lead to less overall switching losses than other conventional switching schemes and is valid for various load conditions and bipolar load current.

This paper includes five sections. The conventional and the proposed switching schemes and their respective mechanisms to achieve soft switching are first outlined in Section II followed by a detailed explanation of the proposed method in Section III. The analytical calculation of overall switching losses is given in Section IV. Finally, key simulated and experimental waveforms of a scaled 1 kVA prototype inverter (using the proposed soft-switching scheme) are presented to validate the ZVZCS scheme for the front-end isolated dc/dc converter. The comparison of the overall switching losses for the inverter prototype using the proposed ZVZCS and state-of-the-art schemes are presented as well.

II. Overview of the Proposed Switching Scheme

A. Conventional Switching Schemes With ZCS

The conventional switching scheme applies a square-wave modulation on the front-end bridges such that Bridge III can be treated as a fixed-dc-input VSI, although its input is not strictly a dc. Various types of SPWM or SVM schemes can be utilized to modulate Bridge III and the ZCS of both front-end bridges can be achieved by switching the associated switches during the zero-vector intervals of Bridge III.

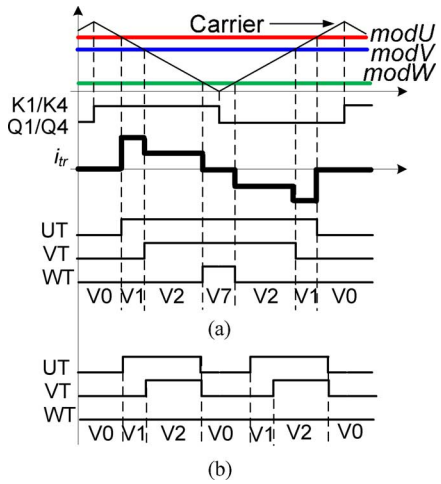


Fig. 2. Gate signals and the transformer current in one switching cycle for an RHFL converter with square-wave modulation on front-end bridges and two different schemes on Bridge III. (a) SPWM with one-sixth third harmonic injection. (b) Discontinuous switching scheme "DIS-V0."

Fig. 2(a) illustrates this mechanism by plotting gate signals of switches of Bridges I and II, gate signals of three upper switches of Bridge III, and $i_{\rm tr}$ (transformer current) of the RHFL converter. Bridge III is modulated using a carrier-based SPWM with third-harmonic injection that is one-sixth of the fundamental waveform in magnitude [20]. This scheme is referred to as "SPWM-3rd." All switches on Bridges I and II are turned on and off during zero-vector intervals of Bridge III [see zero vectors V0 and V7 in Fig. 2(a)]. During that time interval, all of the upper switches (UT, VT, WT) or all of the lower switches (UB, VB, WB) of Bridge III are ON, as represented by V7 or V0. Further, during these zero-vector intervals, load currents circulate inside Bridge III, causing a zero $i_{\rm tr}$. Therefore, switches K1 through K4 and Q1 through Q4 operate under

ZCS. As will be explained in Section III, the switching losses of a MOSFET caused by the discharging of its body capacitor ($C_{\rm oss}$) are not considered here. Also notice that switches of Bridge III commutate six times per switching cycle under hard-switching conditions.

Some discontinuous-SVM schemes, initially proposed for fixed-dc-link VSI, can also be adopted for Bridge III to reduce its switching loss without affecting the ZCS of Bridges I and II. These schemes differ on how to place V0 and V7. Fig. 2(b) shows gate signals for switches UT, VT, and WT when Bridge III is modulated using a discontinuous-SVM scheme, which uses only V0 [25]. For this scheme, at any instant of time, only one of the legs of Bridge III does not switch. In this paper, this scheme will be referred to as "DIS-V0."

Another popular SVM scheme, also known as "minimum-switching-loss-PWM", alternatively uses V0 and V7 at each of the six adjacent sectors in one line cycle [26]. This method has two variations: one, which is suitable for inductive loads, and the other, which is suitable for capacitive loads. For both these schemes, at any instant of time, only one of the legs of Bridge III does not switch. In this paper, these schemes will be referred to as "DIS-V7V0" and "DIS-V0V7," respectively.

B. Proposed ZVZCS Phase-Shifting Scheme for Front-End Bridges

The switching scheme proposed for the HFL converter illustrated in Fig. 1 applies a six-pulse-modulated phase-shifting control with the ZVZCS scheme (outlined in Section III) for Bridges I and II and the hybrid modulation for Bridge III that is outlined in [1], [2], and [21]. We only focus on the ZVZCS phase-shifting scheme for Bridges I and II in this paper.

Notice that the topology of the front-end dc/dc converter is widely used in many applications. However, most existing soft-switching schemes are not applicable due to the lack of capability to handle the pulsating output current $i_{\rm rec}$. For a three-phase RHFL converter, current $i_{\rm rec}$ normally experiences abrupt changes in magnitude and polarity during a switching period. It is unlike the case in a high-frequency-switched dc/dc (unidirectional or bidirectional) or a single-phase dc/ac converter, where the output current of the rectifier stage can be regarded as constant within a switching cycle [16]–[18], [30], [31]. The proposed switching scheme enables a seamless transition between Bridge I ZCS and Bridge II ZVS according to the polarity of output current of Bridge II ($i_{\rm rec}$) without sensing any current or voltage, and therefore, it is effective for various load conditions.

Fig. 3(a) plots gate signals, carrier signal, and two reference signals [ref6(t) and mod$W(t)$] of the proposed scheme. Signals are captured for one switching cycle (f_s Hz) and when only leg W operates at high frequency. As shown in Fig. 3, K1 and K2, and Q1 and Q2 are synchronized with the sawtooth carrier ($2f_s$ Hz), while K3 and Q3, and K4 and Q4 are phase-shifted with respect to K1 and K2. The phase shift is adjusted by a six-pulse reference, ref6(t) (spread across six regions P1–P6) and is obtained by rectifying a three-phase ac signal as defined

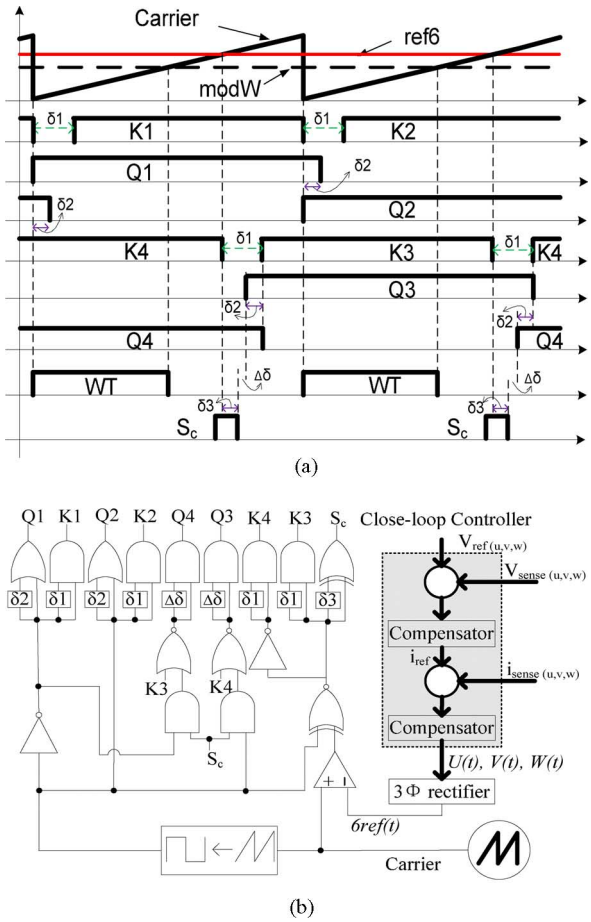


Fig. 3. (a) Carrier, references, and some gate signals in one switching cycle for the RHFL converter in Fig. 1 operating with the proposed ZVZCS scheme. (b) Control diagram for the front-end two bridges.

in (1) and (2)

$$\text{ref6}\,(t)=\begin{cases} w\,(t)-v\,(t) & \text{P1}: \quad -\pi/6\le\omega t<\pi/6 \\ u\,(t)-v\,(t) & \text{P2}: \quad \pi/6\le\omega t<\pi/2 \\ u\,(t)-w\,(t) & \text{P3}: \quad \pi/2\le\omega t<5\pi/6 \\ v\,(t)-w\,(t) & \text{P4}: \quad 5\pi/6\le\omega t<7\pi/6 \\ v\,(t)-u\,(t) & \text{P5}: \quad 7\pi/6\le\omega t<3\pi/2 \\ w\,(t)-u\,(t) & \text{P6}: \quad 3\pi/2\le\omega t<11\pi/6 \end{cases} \tag{1}$$

$$\begin{cases} u(t)=m\sin(\omega t) \\ v(t)=m\sin\left(\omega t-\dfrac{2\pi}{3}\right) \\ w(t)=m\sin\left(\omega t+\dfrac{2\pi}{3}\right) \end{cases} \tag{2}$$

where $u(t)$, $v(t)$, and $w(t)$ in (1) and (2) are the three-phase voltage references with amplitude m. For a unity-amplitude carrier, m is less than 0.577 for the converter to operate below the overmodulation region. Modulation index (MI) is defined as the ratio of m and 0.577. Reference mod$W(t)$ is used to modulate leg W of Bridge III.

In practice, a small dead time $\delta 1$ is added to the complementary switches of Bridge I to prevent the short-circuiting of the input voltage source, and a small overlap time $\delta 2$ is added to the

complementary switches of Bridge II to avoid the open circuit of the load current. As observed from Fig. 3, $\delta 1$ must be larger than $\delta 2$ to preclude short-circuiting of Bridge I caused by Bridge II. The switch of active-clamp circuit S_c (shown in Fig. 1 with a dotted line) turns on before the falling edge of K3 or K4, and remains on for a small time of $\delta 3$. It turns off before switch Q3 or Q4 turns on to avoid short-circuiting of the clamp capacitor C_c (i.e., $\Delta\delta = \delta 1 - \delta 2 - \delta 3 > 0$). The control diagram is plotted in Fig. 3(b) to illustrate how to generate the corresponding gate signals for Bridges I and II. Many voltage and/or current closed-loop controllers [shown in the dotted rectangle block in Fig. 3(b)] proposed for three-phase systems can be adopted.

C. Mechanisms of the Proposed ZVZCS Scheme

By properly selecting the width of $\delta 1$ through $\delta 3$, the proposed ZVZCS scheme can achieve soft-switching for the front-end switches regardless of the polarities of $i_{\rm rec}$. For positive $i_{\rm rec}$ (the definition of variables and their positive directions are given in Fig. 1), diodes on Bridge II conduct and switches on Bridge II have ZCS. For negative $i_{\rm rec}$, diodes on Bridge I conduct and switches on Bridge I have ZVS. Furthermore, as will be explained in detail in Section III, if $i_{\rm rec}$ is positive right after WT turns off, a zero-current region of the transformer current $i_{\rm tr}$ will be created before Q3 (or Q4) turns on. Depending on the polarity of $i_{\rm rec}$ right after WT turns on, this ZC region will end either after K2 (or K1) turns on (if $i_{\rm rec} > 0$) or after Q1 (or Q2) turns off (if $i_{\rm rec} < 0$). On the other hand, if $i_{\rm rec}$ is negative right after WT turns off, a zero-voltage region of Bridge II output voltage $V_{\rm rec}$ will be generated before Q3 (or Q4) turns on, and similarly, this ZV region will end either after K2 (or K1) turns on or after Q1 (or Q2) turns off according to the polarity of $i_{\rm rec}$. The switches of Bridge I will have ZCS if they are operating within the ZC regions and the switches of Bridge II will have ZVS if they are operating within the ZV regions. In either case, the current of a diode will decay to zero before it sustains reverse-biased voltages. Therefore, diodes of both bridges have lossless turn-off, which eliminates reverse-recovery problems.

The active-clamp circuit used in this scheme has multiple functions. It recovers the stored leakage energy and limits the overvoltage spikes caused by the resonance between the leakage inductance and the parasitic capacitance. Importantly, it helps obtain the aforementioned ZV or ZC regions. The detailed explanation on operating principles of ZVZCS switching mechanism for Bridges I and II is provided in Section III.

III. Detailed ZVZCS Operation Under Various Load Conditions

A. Assumptions and Notes

1) Although MOSFETs are applicable, insulated-gate bipolar bipolar transistors (IGBTs) are chosen for Bridges II and III along with antiparallel diodes. The current is considered separately for each IGBT and diode. Switch current of Bridge I will not be separated. Switches on all bridges are assumed to be ideal except when switching losses need to be considered.
2) Dead time needed for two complementary switches on the switching leg of Bridge III is not considered here.
3) Load currents are assumed to be three balanced sinusoidal waveforms with amplitude I

$$\begin{cases} i_{\rm u}(t) = I\sin(\omega t - \varphi) \\ i_{\rm v}(t) = I\sin\left(\omega t - \varphi - \dfrac{2\pi}{3}\right) \\ i_{\rm w}(t) = I\sin\left(\omega t - \varphi + \dfrac{2\pi}{3}\right) \end{cases} \tag{3}$$

where φ in (3) is the phase displacement between a phase current and the corresponding phase voltage.
4) The analysis given shortly is based on the conditions with inductive loads ($\varphi > 0$) but also applicable for capacitive loads.
5) Due to the three-phase symmetry, only two segments P2 and P3 are described. Operations in P4 and P6 are similar to P2, while operations in P1 and P5 are similar to P3.

Waveforms of the gate signals, current of the clamp capacitor, $i_{\rm sc}$ and its voltage V_c, and transformer current $i_{\rm tr}$ are sketched on a switching cycle basis for the case of $\varphi \in [0, \pi/6]$ (Fig. 4, small inductive load conditions) and $\varphi \in [\pi/6, \pi/2]$ (Fig. 5, large inductive load conditions). For each figure, waveforms on the left part show a half-cycle operation in P2 ($\omega t \in [\pi/6, \pi/2]$), while waveforms on the right show a half-cycle operation at P3 ($\omega t' \in [\pi/2, 5\pi/6]$). The starting points in P2 and P3 are marked as t_1 and t_1'. The phase distance between t_1 and the beginning of P2 ($\pi/6$) equals the distance between t_1' and the beginning of P3 ($\pi/2$), as shown in (4)

$$t_1 - \frac{\pi}{6} = t_1' - \frac{\pi}{2}. \tag{4}$$

V_c, the voltage of capacitor C_c, is assumed fixed. Three-phase filter inductor currents $i_{\rm u}, i_{\rm v}$, and $i_{\rm w}$ as defined in (3) are assumed constant within one switching cycle and can be written as

$$\begin{cases} i_{\rm u}(t) = -i_{\rm w}(t') = i_{\rm a} \\ i_{\rm v}(t) = -i_{\rm u}(t') = i_{\rm b} \\ i_{\rm w}(t) = -i_{\rm v}(t') = i_c. \end{cases} \tag{5}$$

Current waveforms of Bridge III are also plotted in Figs. 4 and 5.

B. Soft Switching Under Small Inductive Loads ($\varphi \in [0, \pi/6]$)

Case 1 ($\omega t \in [\pi/6, \pi/3 + \varphi] \subset$ P2), Fig. 4(a): $i_{\rm rec}$ switches from $-i_{\rm b}$ to $i_{\rm a}$ when WT turns off, and $-i_{\rm b} > i_{\rm a} > 0$. While their body diodes conduct, switches Q1–Q4 have no effect on the operation. The converter has 11 operating modes within each half switching cycle, as illustrated in Fig. 4(a). The analysis starts at t_1 with zero $V_{\rm rec}, i_{\rm rec}$, and $i_{\rm tr}$. Load currents $i_{\rm a}, i_{\rm b}$, and i_c circulate among the three legs of Bridge III before t_1.

Mode 1 (t_1–t_2): Switch K2 turns off with zero current at t_1; switches WT and WB of Bridge III commutate under ZVS. Both voltages $V_{\rm pri}$ and $V_{\rm rec}$ are zero.

Mode 2 (t_2–t_3): K1 turns on at t_2. Because of the existence of leakage inductance, the transformer current $i_{\rm tr}$ can only rise at

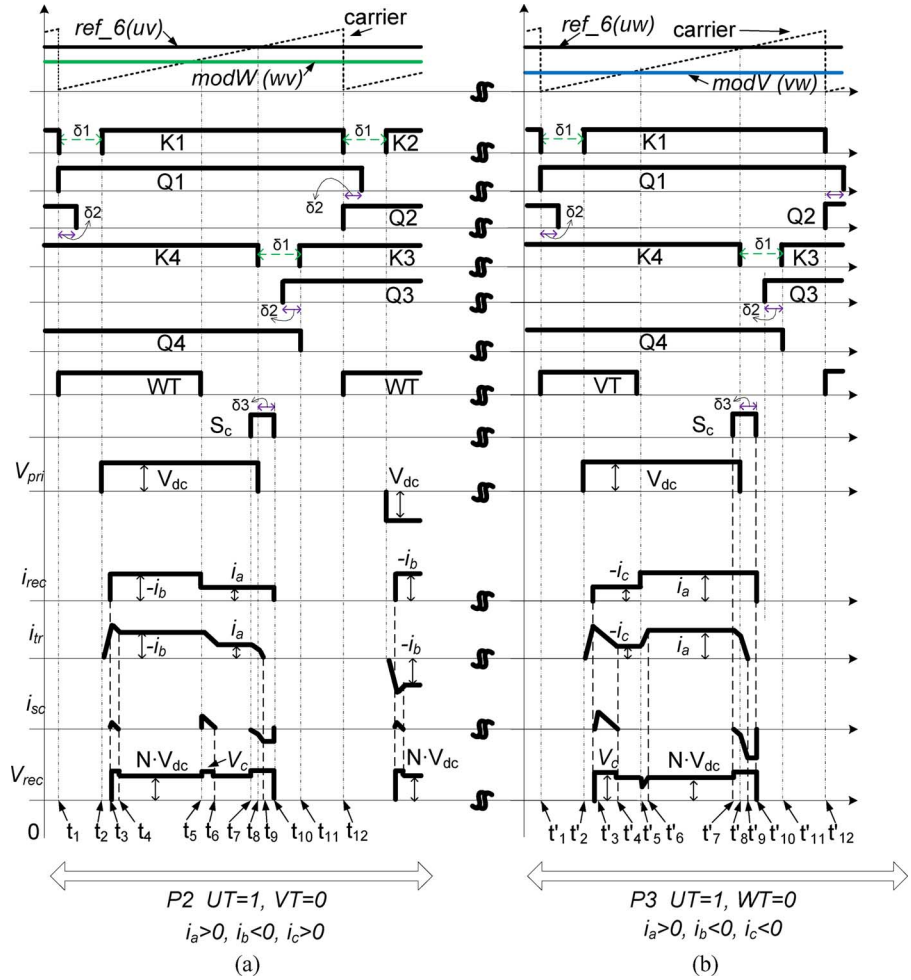


Fig. 4. Switching waveforms of an RHFL converter with small inductive loads using the proposed scheme and operating at (a) P2 and (b) P3.

a finite rate determined by $V_{\rm dc}/(NL_{\rm k})$. Therefore, the turn-on loss of K1 is small, although it is not strictly ZCS.

Mode 3 (t_3–t_4): $i_{\rm tr}$ reaches $-i_{\rm b}$ at t_3. After that, the transformer leakage inductance resonates with the parasitic capacitance. $V_{\rm rec}$ increases rapidly, then clamped to V_c. K1 and K4 conduct to transfer power to the secondary side. The stored energy in the leakage inductance is recovered to the capacitor C_c. Currents of the transformer and clamp capacitor are

$$i_{\rm tr}\left(t\right) = i_{\rm tr}\left(t_3\right) - \frac{NV_{\rm dc} - V_c}{N^2 L_{\rm k}} t \tag{6}$$

$$i_{\rm sc}\left(t\right) = i_{\rm tr}\left(t\right) - \left(-i_{\rm b}\right). \tag{7}$$

This mode ends when $i_{\rm sc}$ decays to zero.

Mode 4 (t_4–t_5): The body diode of S_c blocks, and

$$V_{\rm rec} = NV_{\rm dc} \tag{8}$$

$$i_{\rm tr}\left(t\right) = i_{\rm rec}\left(t\right) = -i_{\rm b}. \tag{9}$$

Mode 5 (t_5–t_6): WT turns off and WB turns on at t_5. $i_{\rm rec}$ changes from $-i_{\rm b}$ to $i_{\rm a}$. Diode of S_c conducts. $i_{\rm tr}$ and $i_{\rm sc}$ change in the same way as given in (6) and (7). This mode ends when $i_{\rm sc}$ decays to zero.

Mode 6 (t_6–t_7): The body diode of S_c blocks, and

$$V_{\rm rec} = NV_{\rm dc} \tag{10}$$

$$i_{\rm tr}\left(t\right) = i_{\rm rec}\left(t\right) = i_{\rm a}. \tag{11}$$

Mode 7 (t_7–t_8): At t_7, S_c turns on under a small voltage. $i_{\rm tr}$ decreases with a rate determined by

$$i_{\rm tr}\left(t\right) = i_{\rm a} + \frac{NV_{\rm dc} - V_{\rm c}}{N^2 L_{\rm k}} t \tag{12}$$

$$i_{\rm sc}\left(t\right) = i_{\rm tr}\left(t\right) - i_{\rm a} \tag{13}$$

$$V_{\rm rec} = V_c. \tag{14}$$

$i_{\rm rec}$ is now supplied by both the transformer and capacitor C_c.

Mode 8 (t_8–t_9): At t_8, switch K4 turns off. Primary side voltage becomes zero, and $i_{\rm tr}$ decays to zero rapidly with a rate determined by $V_c/(N^2 L_{\rm k})$.

Mode 9 (t_9–t_{10}): At t_9, current $i_{\rm tr}$ equals zero. The diodes on Bridge II turn off lossless. After t_9, $i_{\rm rec}$ is only supplied by C_c.

Mode 10 (t_{10}–t_{11}): S_c turns off at t_{10}. Parasitic capacitor discharges and $V_{\rm rec}$ decays to zero as does $i_{\rm rec}$. Load currents will circulate among Bridge III.

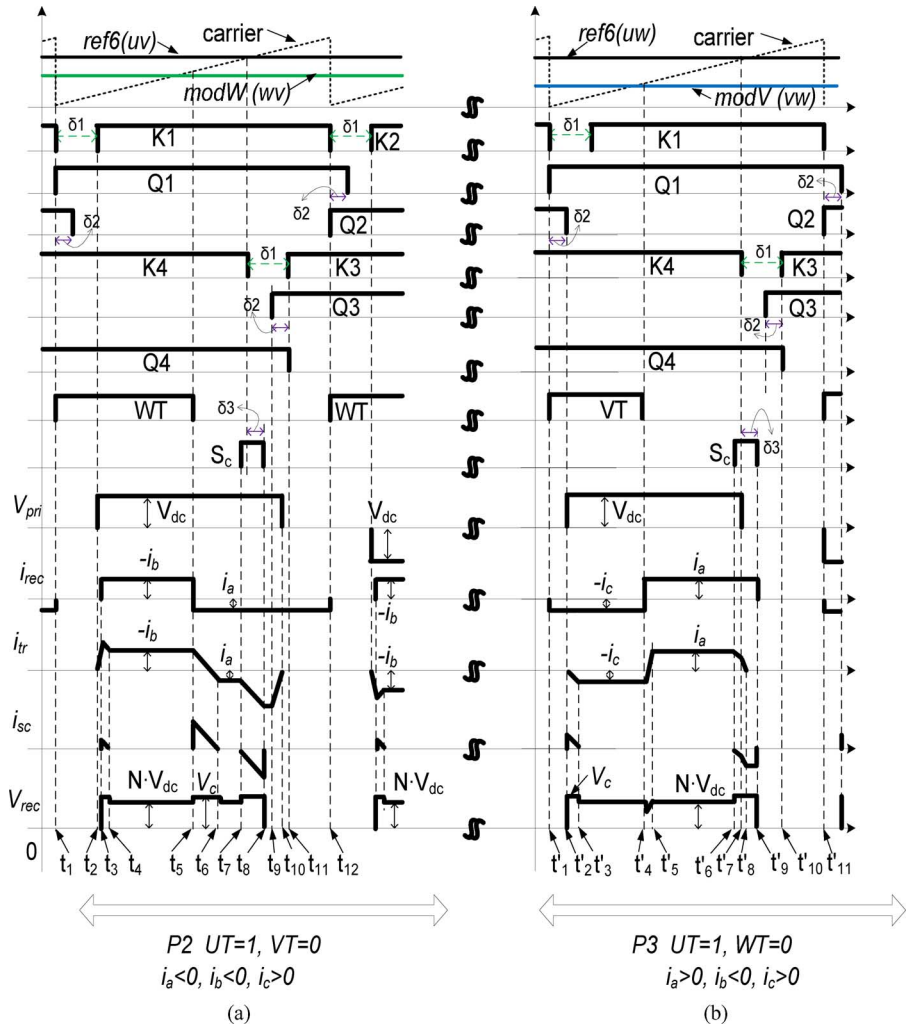


Fig. 5. Switching waveforms of an RHFL converter with large inductive loads using the proposed scheme and operating at (a) P2 and (b) P3.

Mode 11 (t_{11}–t_{12}): $V_{\rm rec}$, $i_{\rm sc}$, $i_{\rm tr}$, and $i_{\rm rec}$ are all zero. K3 turns on at ZCS at t_{11}. In order to ensure ZCS operation, the time $\delta 3$ (between the two falling edges of K4 and S_c) should satisfy

$$\delta 3 > \frac{N^2 L_{\rm k} i_{\rm tr}\left(t_7\right)}{V_c}. \tag{15}$$

Equation (16) should be satisfied for avoiding the short-circuiting of C_c

$$\delta 1 > \delta 2 + \delta 3. \tag{16}$$

K1 turns off with ZCS at t_{12}. The next half-cycle repeats with zero-voltage turn-on of WT.

According to the aforesaid analysis, switches K1 and K2 have ZCS OFF and ZCS ON, while switches K3 and K4 have ZCS ON. Switch S_c turns on at ZVS. Currents of Q1–Q4 decay to zero before the associated switches begin to sustain reverse-biased voltage (after $V_{\rm rec}$ rises). Hence, diodes of Q1–Q4 have lossless turn-off, thus eliminating reverse-recovery problems.

Case 2 ($\omega t' \in [\pi/2, 2\pi/3 + \varphi] \subset$ P3), Fig. 4(b): In P3, $u(t)$–$w(t)$ is the modulation reference for Bridges I and II, while $v(t)-w(t)$ is used to modulate switches on leg V. Switches UT and WB remain ON in P3. Consequently, $i_{\rm rec}$ switches from $-i_c$ to $i_{\rm a}$ whenever VT turns off. The 11 operating modes ($t'_1 - t'_{12}$) at P3 are similar to the modes (t_1–t_{12}) at P2. The soft-switching scheme is also applicable. However, since $0 < -i_c < i_{\rm a}$, the increase in $i_{\rm rec}$ may cause a narrow dent on $V_{\rm rec}$ during the interval ($t'_5 - t'_6$), as shown in Fig. 4(b).

Case 3 ($\omega t \in [\pi/3 + \varphi, \pi/2] \subset$ P2): $0 < -i_{\rm b} < i_{\rm a}$, the operating modes are similar to Case 2 and the soft switching of Bridge II summarized in Case 1 is valid as well.

Case 4 ($\omega t' \in [2\pi/3 + \varphi, 5\pi/6] \subset$ P3): $-i_c > i_{\rm a} > 0$, the operating modes are similar to Case 1, so is the soft switching.

Therefore, when $\varphi \in [0, \pi/6]$, no switching loss appears on Bridges I and II except the hard turn-off on switches K3 and K4. The switching loss of a MOSFET during one switching cycle can be calculated using the widely accepted estimation equation

$$\Delta E_{\rm K}\left(t\right) = \frac{1}{2} V_{\rm dc}\left(t_{\rm ON} + t_{\rm OFF}\right) i_{\rm k}\left(t\right) \times 2 + \frac{1}{2} V_{\rm dc}^2 C_{\rm oss} \times 2 \tag{17}$$

where $i_{\rm k}$ is the load current and $V_{\rm dc}$ is the steady-stage voltage after a MOSFET turns off. Parameters $t_{\rm ON}$ and $t_{\rm OFF}$ are the turn-on and turn-off time, respectively [22]. The multiple 2 appears because the MOSFET is turned off twice in one switching period (f_s Hz). The second term of (17) is often referred to as output capacitor ($C_{\rm oss}$) loss and reflects the additional turn-on losses caused by the discharging of the output capacitor during the turn-on. This term, however, has been found to be redundant in (17) as explained in [32]. Furthermore, it will be relatively small for the MOSFETs applied to Bridge I, which requires low-voltage-rating switches. Therefore, this term is not considered in this paper.

If other conditions are the same, $t_{\rm OFF}$ is less than $T_{\rm OFF\_M}$, the maximal turn-OFF time with the rated continuous current. Thus, the turn-off loss of a MOSFET during one switching cycle can be rewritten from (17) as

$$\Delta E_{\rm OFF\_K}\left(t\right) \le \left(\frac{1}{2}V_{\rm dc}T_{\rm OFF\_M}\right) i_{\rm k}\left(t\right) \times 2 = 2E_{\rm OFF\_K}\, i_{\rm k}\left(t\right). \tag{18}$$

C. Soft Switching Under Large Inductive Loads ($\varphi \in [\pi/6, \pi/2]$)

Case 5 ($\omega t \in [\pi/6, \varphi] \subset$ P2), Fig. 5(a): current $i_{\rm rec}$ is not always larger than zero in this case since $-i_{\rm b} > 0$, but $i_{\rm a} < 0$. The converter has 11 operating modes, as illustrated in Fig. 5(a). $i_{\rm rec}$ equals $i_{\rm a}$ before t_1. It is freewheeling through switches Q2 and Q4. $i_{\rm tr} = 0$, $V_{\rm rec} = 0$, and $V_{\rm pri} = 0$.

Mode 1 (t_1–t_2): Switch K2 turns off under zero current; Q1 turns on under zero voltage at t_1. Switches WT and WB commutate under zero voltage, thus causing $i_{\rm rec}$ to change from $i_{\rm a}$ to zero. Q2 turns off under zero voltage. Voltage $V_{\rm pri}$, $V_{\rm rec}$, and $i_{\rm tr}$ remain at zero until K1 turns on.

Mode 2 (t_2–t_3) to Mode 6 (t_6–t_7) resemble the corresponding five modes under the same numbers in Case 1. K1 turns on with ZCS at t_2 due to the transformer leakage inductance. After t_6, current $i_{\rm tr}$ is less than zero, current flowing in Bridge II shifts from body diodes of Q1–Q4 to their IGBTs, and diodes in Bridge I conduct current.

Mode 7 (t_7–t_8): S_c turns on under near zero-voltage condition. The transformer current increases as

$$i_{\rm tr}\left(t\right) = i_{\rm a} + i_{\rm sc}\left(t\right) = i_{\rm a} + \frac{V_c - NV_{\rm dc}}{N^2 L_{\rm k}}t. \tag{19}$$

Mode 8 (t_8–t_9): S_c turns off at t_8, which shuts down $i_{\rm sc}$. The parasitic capacitance on the secondary side discharges to maintain the transformer current $i_{\rm tr}$. $V_{\rm rec}$ drops rapidly. K4 turns off lossless before t_8 since its body diode conducts.

Mode 9 (t_9–t_{10}): Switch Q3 turns on under zero voltage at t_9, and $i_{\rm rec}$ starts freewheeling through Q1 and Q3. The leakage current $i_{\rm tr}$ reduces rapidly and the stored energy releases to the primary side.

Mode 10 (t_{10}–t_{11}): $i_{\rm tr}$ equals zero after t_{10}. Diodes on the primary side turn off softly, and therefore, $V_{\rm pri}$ drops to zero. Bridge III input current $i_{\rm rec}$, however, continues to flow through Q1 and Q3.

Mode 11 (t_{11}–t_{12}): $V_{\rm rec}, i_{\rm sc}, i_{\rm tr}$, and $V_{\rm pri}$ are all zero. At t_{11}, Q4 turns off under ZVS (or ZCS), and K3 turns on under ZCS. At t_{12}, K1 turns off under ZCS, and Q2 turns on under ZVS (or ZCS). The next half-cycle repeats with ZVS-turn-on of WT.

Therefore, switches Q1–Q4 have ZVS ON and OFF, while switches K1–K4 have ZCS ON and ZCS OFF. Diodes for all front-end switches have no switching loss. In other words, no switching loss occurs on Bridges I and II for this case.

Case 6 ($\omega t' \in [\pi/2, \pi/3 + \varphi,] \subset$ P3), Fig. 5(b): Before t_1', $i_{\rm rec} = 0$, $i_{\rm tr} = 0$, $V_{\rm rec} = 0$, and $V_{\rm pri} = 0$.

Mode 1 (t_1'–t_2'): Switch Q1 turns on at t_1' with ZVS; switches VT and VB commutate on zero-voltage condition. The resultant $i_{\rm rec}$ changes from zero into $-i_c$. This current is freewheeling through switches Q2 and Q4. Voltage $V_{\rm pri}$ and $V_{\rm rec}$ are still zero. The transformer current $i_{\rm tr}$ also remains at zero.

Mode 2 (t_2'–t_3'): Q2 turns off at t_2'. Current $i_{\rm rec}$ starts flowing through the transformer, and Q1, Q4. Again, the transformer current $i_{\rm tr}$ can only rise at a finite rate. The parasitic capacitor and C_c will conduct the difference between $i_{\rm rec}$ and $i_{\rm tr}$. $V_{\rm rec}$ will be clamped to V_c rapidly. This mode ends at t_3 when $i_{\rm tr}$ reaches $-i_c$. After that, the body diode of S_c blocks.

Mode 3 (t_3'–t_4'): In this interval, $i_{\rm tr}$ equals $-i_c$, and $V_{\rm rec}$ equals $NV_{\rm dc}$. The power is flowing back to the input side. K1 turns on at ZCS since its body diode conducts.

Mode 4 (t_4'–t_5'): VT turns off and VB turns on at t_4'. $i_{\rm rec}$ changes from a negative value, $-i_c$, into a positive value, $i_{\rm a}$. Currents flowing through Q1, Q4 shift from IGBTs to their antiparallel diodes. Currents in K1 and K4 change from their body diodes to the MOSFET channels. Similar to the operations in the interval (t_5'–t_6') of Fig. 4(b), a narrow dent on $V_{\rm rec}$ may occur.

Mode 5 (t_5'–t_6') to *Mode 10* (t_{10}'–t_{11}') resemble the operations between (t_6'–t_{12}') of Case 2 in Fig. 4(b), and the soft switching during these intervals is the same.

Note that, Q3 turns on with ZVS between (t_9'–t_{10}'), and Q4 turns off with ZVS at t_{10}'. We can conclude that both Q1 and Q2 have ZVS ON, while both Q3 and Q4 have ZVS ON and ZVS OFF. As for Bridge I, K3, K4 have ZCS ON, while both K1 and K2 have ZCS ON and ZCS OFF. Switching losses in this case include turn-off losses of Q1, Q2, K3, and K4.

Equation (18) is still applicable for estimating the turn-off loss of K3 and K4. As for Q1 and Q2, their losses can be calculated based on the assumption that switching energy is proportional to the current [19], [23], [24]

$$\Delta E_{\rm OFF\_Q}\left(t\right) = 2E_{\rm OFF\_S}\, i_{\rm w}\left(t\right). \tag{20}$$

$E_{\rm OFF\_S}$ in (20) is the per ampere turn-off energy for an IGBT. Following the same way, the per ampere turn-on energy for an IGBT ($E_{\rm ON\_S}$), and turn-on and turn-off energies for a diode ($E_{\rm OFF\_D}$ and $E_{\rm ON\_D}$) can be denoted accordingly.

Case 7 ($\omega t \in [\varphi, \pi/2] \subset$ P2): Since $-i_{\rm b} > i_{\rm a} > 0$, the operating modes and soft-switching scheme are similar to Case 1.

Case 8 ($\omega t' \in [\pi/3+\varphi, 5\pi/6] \subset$ P3): Since $0 < -i_c < i_{\rm a}$, the operating modes and soft-switching scheme are similar to Case 2.

IV. Analysis and Comparison of Swicthing Losses

A. Switching Losses of Front-End Bridges I and II

Integrating (18) over P2 and P3, the switching losses on the two ranges can be calculated, respectively, as

$$P_{\text{front\_P2}} < \frac{3f_{\text{s}}}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} \left[2E_{\text{OFF\_}K}Ni_{\text{w}}\left(t\right)\right]dt \tag{21}$$

$$P_{\text{front\_P3}} < \frac{3f_{\text{s}}}{\pi}\int_{\frac{\pi}{2}}^{\frac{5\pi}{6}} \left[2E_{\text{OFF\_}K}Ni_{\text{w}}\left(t\right)\right]dt. \tag{22}$$

The switching losses of Bridges I and II for $\varphi \in [0, \pi/6]$) are obtained by averaging (21) and (22)

$$\begin{aligned} P_{\text{front}} &= \frac{1}{2}\left(P_{\text{front\_P2}} + P_{\text{front\_P3}}\right) \\ &< \frac{3f_{\text{s}}}{\pi} I E_{\text{OFF\_}K} N\left[\cos\left(\frac{\pi}{6}+\varphi\right)+\cos\left(\frac{\pi}{6}-\varphi\right)\right]. \end{aligned} \tag{23}$$

Similarly, switching losses of Bridges I and II for $\varphi \in [\pi/6, \pi/2]$) are calculated as

$$\begin{aligned} P_{\text{front}} < \frac{3f_{\text{s}}I}{\pi}\Bigg\{ & E_{\text{OFF\_}K}N\left[1+\cos\left(\frac{\pi}{6}+\varphi\right)\right] \\ & + E_{\text{OFF\_}S}\left[1-\cos\left(\frac{\pi}{6}-\varphi\right)\right]\Bigg\}. \end{aligned} \tag{24}$$

B. Switching Losses of Bridge III

Following the operating principle of the hybrid modulation outlined in [1], [2], and [21], the switching losses of Bridge III can be described by

$$\begin{aligned} P_{\text{III}} = \frac{3f_{\text{s}}}{\pi} I\Bigg\{ & E_{\text{D}}\left[\cos\left(\frac{\pi}{6}+\varphi\right)+\cos\left(\frac{\pi}{6}-\varphi\right)\right] \\ & + \left(\frac{3}{2}E_{\text{D}}+E_{\text{S}}\right)\left[2-\cos\left(\frac{\pi}{6}+\varphi\right)\right. \\ & \left.-\cos\left(\frac{\pi}{6}-\varphi\right)\right]\Bigg\} \end{aligned} \tag{25}$$

for small inductive loads ($\varphi \in [0, \pi/6]$), and

$$\begin{aligned} P_{\text{III}} = \frac{3f_{\text{s}}}{\pi} I\Bigg\{ & E_{\text{D}}\left[1+\cos\left(\frac{\pi}{6}+\varphi\right)\right] \\ & + \left(\frac{3}{2}E_{\text{D}}+E_{\text{S}}\right)\left[\cos\left(\frac{\pi}{6}-\varphi\right)\right. \\ & \left.-\cos\left(\frac{\pi}{6}+\varphi\right)\right]\Bigg\} \end{aligned} \tag{26}$$

for large inductive loads ($\varphi \in [\pi/6, \pi/2]$. In (25) and (26), $E_D = E_{\text{ON\_}D} + E_{\text{OFF\_}D}$, and $E_S = E_{\text{ON\_}S} + E_{\text{OFF\_}S}$.

V. Analysis of Soft-Switching Range

A. Determination of Dead Time $\delta 1$–$\delta 3$

To ensure the zero-voltage turn-on of Q3 and Q4, V_{rec} should equal zero before the turn-on of Q3 or Q4. In other words, the parasitic capacitor C_{Q} must be fully discharged to maintain the transformer current after the turn-off of S_c. The energy required in the leakage inductance should be greater than the stored energy in the capacitor

$$\frac{1}{2}\left(N^2L_{\text{k}}\right)\left(i_{\text{tr}}\left(t_8\right)-i_{\text{a}}\right)^2 \geq \frac{1}{2}C_{\text{Q}}\left(V_c\right)^2 \tag{27}$$

where C_{Q} is the sum of the body capacitances of two switches (C_{oss}), and the transformer parasitic capacitance C_{T} is given by

$$C_{\text{Q}} = \frac{8}{3}C_{\text{oss}} + C_{\text{T}}. \tag{28}$$

Transformer current $i_{\text{tr}}\left(t_8\right)$ in (27) is determined by

$$i_{\text{tr}}\left(t_8\right) - i_{\text{a}} = \frac{V_c - NV_{\text{dc}}}{N^2L_{\text{k}}}\delta 3. \tag{29}$$

Combing (27)–(29) with (15), the lower limit of $\delta 3$ is obtained as

$$\delta 3 \geq \delta 3_{\min}\left(t\right) = \begin{cases} \dfrac{N^2L_{\text{k}}i_{\text{a}}}{V_c}, & \text{if} \quad i_{\text{a}} \geq 0 \\ \dfrac{V_c\sqrt{C_{\text{Q}}N^2L_{\text{k}}}}{V_c - NV_{\text{dc}}}, & \text{if} \quad i_{\text{a}} < 0. \end{cases} \tag{30}$$

Second, the duration from the turn-off of S_c (t_8) to the turn-on of Q3 or Q4 (t_9) has to satisfy

$$t_9 - t_8 = \delta 1 - \delta 2 - \delta 3 \approx \frac{\pi}{2}N\sqrt{L_{\text{k}}C_{\text{Q}}}. \tag{31}$$

The term on the right-hand side of (31) stands for one-fourth of the resonance period of the leakage inductor and the parasitic capacitors on the secondary side.

On the other hand, to ensure ZCS of Q3 and Q4, the overlap time between Q3 and Q4 (or Q1 and Q2) should satisfy

$$\delta 2 \geq \frac{NL_{\text{k}}i_{\text{tr}}\left(t_9\right)}{V_{\text{dc}}} \approx \frac{NL_{\text{k}}i_{\text{a}}}{V_{\text{dc}}}. \tag{32}$$

Combining (30)–(32), the lower limit for $\delta 1$ during the range [π/6, 5π/6] is determined as

$$\begin{aligned} \delta 1 &\geq \delta 1_{\min}\left(\text{t}\right) \\ &= \begin{cases} \dfrac{N^2L_{\text{k}}i_{\text{a}}}{V_c}, & \text{if} \quad i_{\text{a}} \geq 0 \\ \dfrac{\pi N\sqrt{L_{\text{k}}2C_{\text{Q}}}}{2} + \dfrac{NL_{\text{k}}i_{\text{a}}}{V_{\text{dc}}} + \dfrac{V_c\sqrt{2C_{\text{Q}}N^2L_{\text{k}}}}{V_c - NV_{\text{dc}}}, & \text{if} \quad i_{\text{a}} < 0. \end{cases} \end{aligned} \tag{33}$$

Because S_c should be turned off before the turn-on of Q1 or Q2, the upper limit of $\delta 3$ is determined by

$$\delta 3 \leq \delta 3_{\max}\left(t\right) = \frac{\left(1-uv\left(t\right)\right)}{2f_{\text{s}}} - \frac{\pi}{2}N\sqrt{L_{\text{k}}C_{\text{Q}}}. \tag{34}$$

From Figs. 4 and 5, the effective width of V_{rec} can be estimated by

$$\text{width of } V_{\text{rec}} \approx \begin{cases} \dfrac{uv\left(t\right)}{2f_{\text{s}}} - \delta 1, & \text{if} \quad i_{\text{rec}}\left(t_2\right) \geq 0 \\ \dfrac{uv\left(t\right)}{2f_{\text{s}}} - \delta 2, & \text{if} \quad i_{\text{rec}}\left(t_2\right) < 0. \end{cases} \tag{35}$$

Therefore, in order to minimize the impact on the width of V_{rec}, $\delta 1$ and $\delta 2$ should be very small as compared to the first

TABLE I
MAIN COMPONENTS USED IN THE PROTOTYPE

NAME	PART NUMBER	DESCRIPTIONS
K1 – K4	IPP070N06L	60V/80A/6.7mΩ, MOSFET
Q1 - Q4 and UT - WB	IRGB4B60K	600V/6.8A, IGBT
	IDT016S60C	600V/16A, diode
S_c	IRFIB7N50L	500V/6.8A/320mΩ, MOSFET
C_c	0.5uF, 400V	electrolytic capacitor

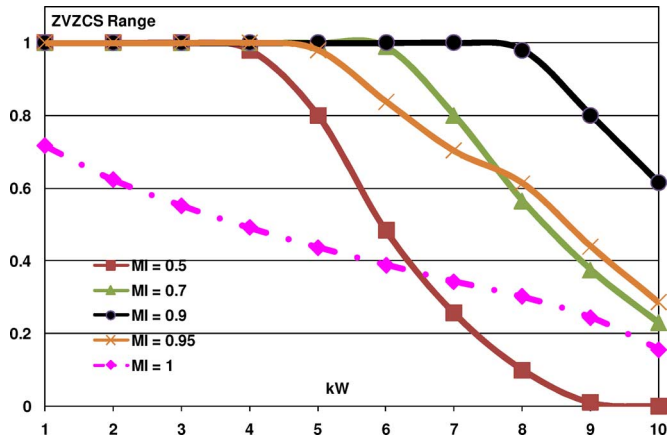


Fig. 6. Predicted ZVZCS range of the front-end bridges with variation in output power and modulation indexes ($L_k = 0.3\ \mu$H, $C_Q = 0.1$ nF, $\varphi = 0°$).

term. The upper limit for $\delta 1$ can be defined as

$$\delta 1 \le \delta 1_{\max}(t) \triangleq 0.1\frac{uv(t)}{2f_s} \ll \frac{uv(t)}{2f_s}. \tag{36}$$

B. ZVZCS Ranges

ZVS or ZCS can be achieved as long as $\delta 1$ and $\delta 3$ are selected properly following the criteria described earlier. However, ZVZCS is impossible if $\delta 1_{\min}(t)$ is less than $\delta 1_{\max}(t)$ or $\delta 3_{\min}(t)$ is less than $\delta 3_{\max}(t)$. The ZVZCS range can be expressed as the percentage of the available ZVZCS time over the whole time of P2 and P3, i.e., one-third of the line-cycle time period. The parametric results of ZVZCS ranges with variation in output power, MI, transformer leakage inductance, and output power factor will be given in the next section to investigate their effect on the soft-switching performance.

VI. SIMULATED AND EXPERIMENTAL RESULTS

An RHFL converter has been designed to validate the proposed soft-switching scheme. The designed input voltage is 40 V dc, and the rated output voltage is 208 V ac (line to line). Switching frequency at Bridge III is 43.2 kHz. Transformer turns ratio is about 1:8.4. The components used for a 1 kVA converter prototype are listed in Table I. The associated switching energy per ampere for each type of switch can be calculated according to its datasheet: $E_{ON_S} = 18.25\ \mu$J/A, $E_{OFF_S} = 11.75\ \mu$J/A, $E_{OFF_K} \approx 1\ \mu$J/A, $E_{OFF_D} = 1\ \mu$J/A, and $E_{ON_D} \approx 0\ \mu$J/A.

Figs. 6–8 show that the ZVZCS range reduces with higher output power, higher leakage inductance, or either too high or too low MIs. The ZVZCS range is less affected by the power factor, especially at low output power. V_c is assumed to be 1.1 NV_{dc} for the earlier analysis.

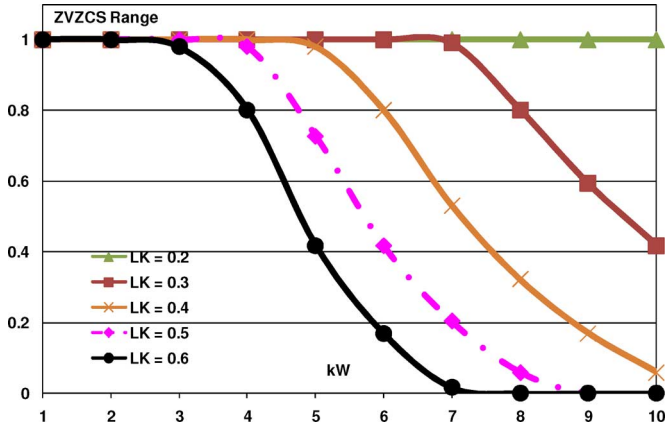


Fig. 7. Predicted ZVZCS range of the front-end bridges with variation in output power and leakage inductances (MI = 0.8, $C_Q = 0.1$ nF, $\varphi = 0°$).

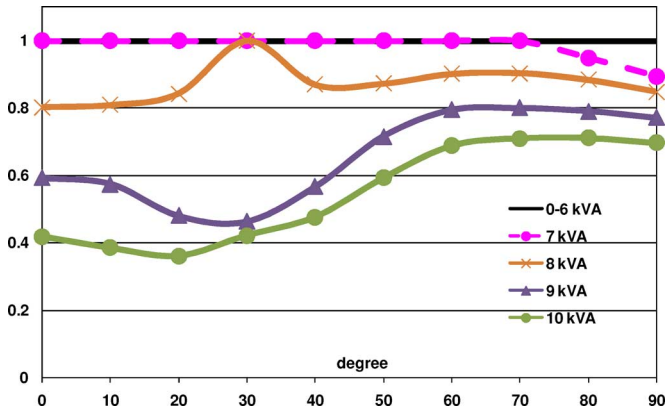


Fig. 8. Predicted ZVZCS range of the front-end bridges with variation in output power and power factors (MI = 0.8, $L_k = 0.3\ \mu$H, $C_Q = 0.1$ nF).

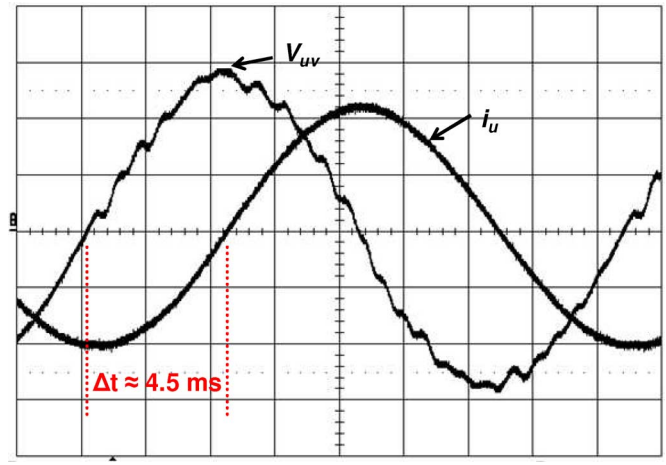


Fig. 9. Output line-to-line voltage (100 V/division, 2 ms/divsion) and phase current (2.5 A/division) at inductive loads with $\varphi \approx 67°$ (60 Hz).

Figs. 9–15 show waveforms of an RHFL converter with the proposed scheme under about 67° inductive loads. Fig. 9 plots the line-to-line output voltage V_{uv} and the phase U current. Drive

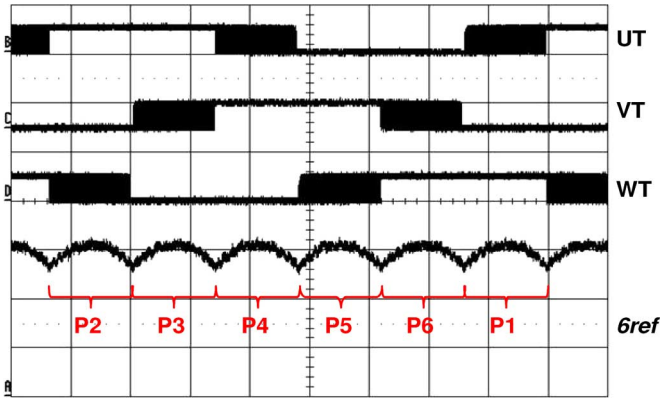


Fig. 10. Gate-drive signals UT, VT, and WT (25 V/division, 2 ms/division) and reference signal ref6(t) (1 V/division) with six segments P1–P6 indicated.

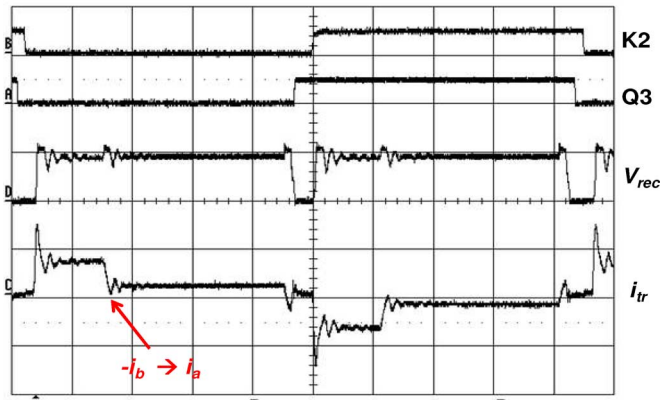


Fig. 11. Gate-drive signals K2, Q3 (25 V/division, 5 μs/division), $V_{\rm rec}$ (250 V/division), and $i_{\rm tr}$ (5 A/division) for Case 7 ($-i_{\rm b} > i_{\rm a} > 0$, $\omega t \in [\varphi, \pi/2] \subset$ P2).

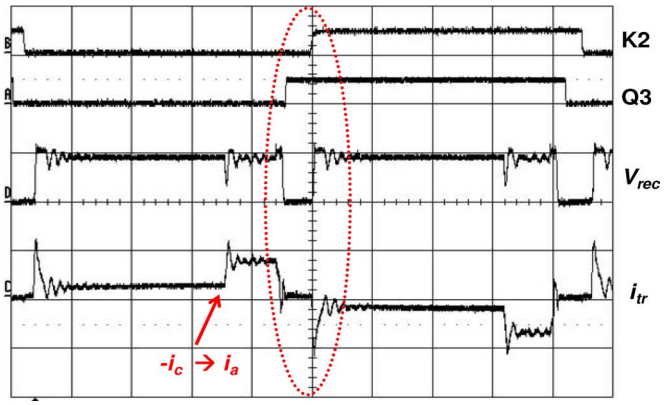


Fig. 12. Gate-drive signals K2, Q3 (25 V/division, 5 μs/division), $V_{\rm rec}$ (250 V/division), and $i_{\rm tr}$ (5 A/division) for Case 8 ($0 < -i_c < i_{\rm a}, \omega t' \in [\pi/3 + \varphi, 5\pi/6] \subset$ P3).

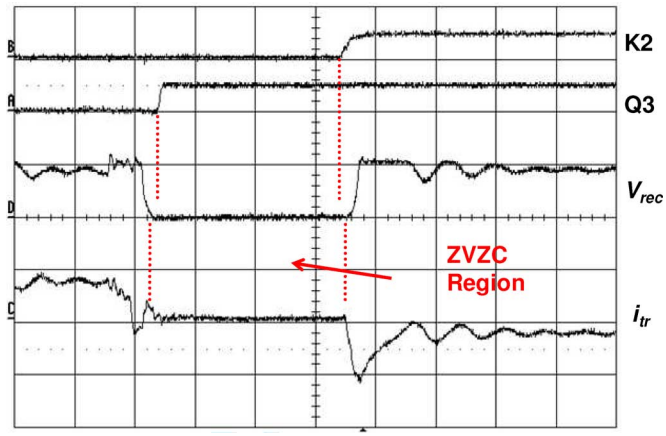


Fig. 13. Expanded picture (1 μs/division) of Fig. 12 around the ZVZC region.

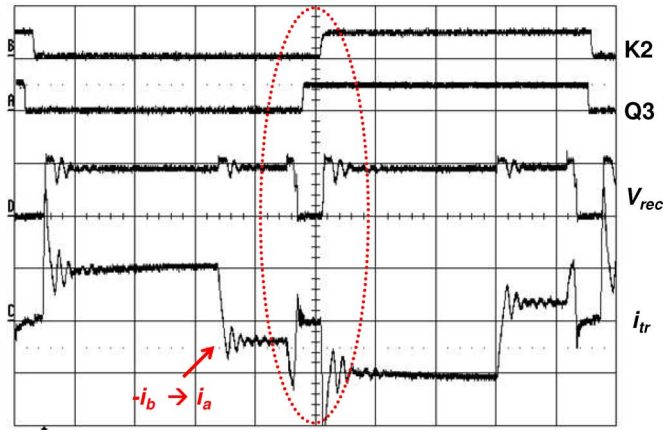


Fig. 14. Gate-drive signals K2, Q3 (25 V/division, 5 μs/division), $V_{\rm rec}$ (250 V/division), and $i_{\rm tr}$ (2.5 A/division) for Case 5 ($i_{\rm a} < 0 < -i_{\rm b}$, $\omega t \in [\pi/6, \pi/6 + \varphi] \subset$ P2).

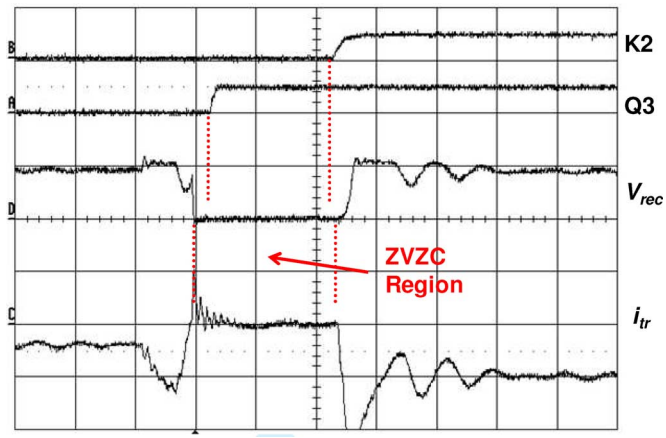
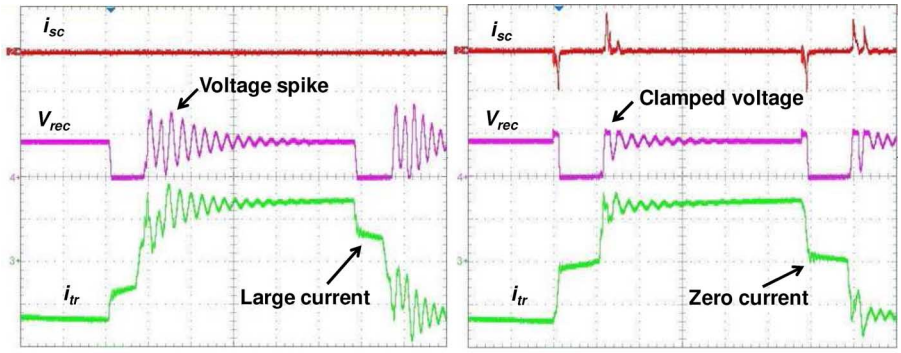


Fig. 15. Expanded picture (1 μs/division) of Fig. 14 around the ZVZC region.

signals for three upper switches on Bridge III and reference signal for Bridges I and II are plotted in Fig. 10. Six segments P1–P6 are also included. As expected, per hybrid modulation [1], [2], [21], only one leg of Bridge III commutates and the remaining legs are either ON or OFF for the whole period of each segment.

The effectiveness of the ZVZCS scheme under large inductive load conditions was verified. Figs. 11, 12, and 14, for Cases 7, 8, and 5, respectively, plot two gate drives K2 and Q3 and the



(a) (b)

Fig. 16. Experimental waveforms of $i_{\rm sc}$ (2.5 A/division, 4 μs/division), $V_{\rm rec}$ (250 V/division), and $i_{\rm tr}$ (2.5 A/division) of the prototype when the proposed soft-switching scheme is disabled (a) and enabled (b).

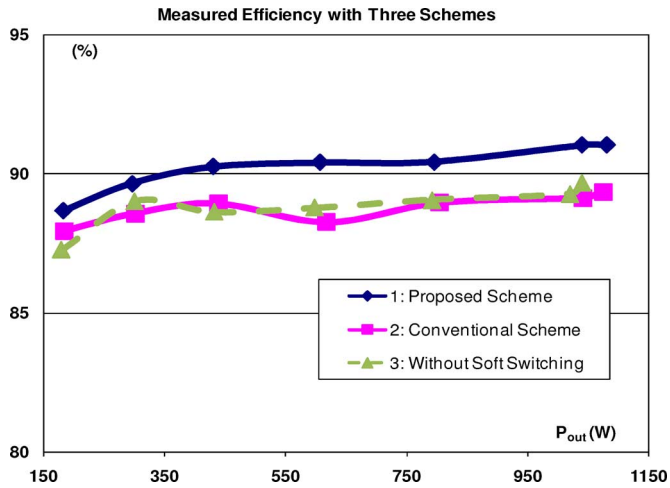


Fig. 17. Measured overall efficiency of an RHFL converter with three modulation schemes under different output powers.

corresponding $V_{\rm rec}$ and $i_{\rm tr}$. The changes of transformer currents due to the commutation of switches on Bridge III are indicated by arrows. The ZC or ZV regions (shown in the dotted circles) of Figs. 12 and 14 are expanded in Figs. 13 and 15, respectively. The waveforms show that the turn-on edges of Q3 and K2 occur inside the ZVZC region for positive and negative $i_{\rm rec}$.

Therefore, Q3 turns on at ZVS, and K2 turns on at ZCS in both cases. In addition, Q4 turns off, and Q2 turns on at ZVS; K3 turns on, and K1 turns off at ZCS since their corresponding edges occur between the two rising edges of Q3 and K2. The same conclusions can be obtained for their complementary switches at the next ZVZC region. Further, the upper and lower switches of Bridge III turn on and turn off under the ZVS condition.

Fig. 16 compares the Bridge II output voltage $V_{\rm rec}$ and the transformer current $i_{\rm tr}$ of the RHFL converter prototype with and without the clamp capacitor C_c connected (thereby the proposed soft switching on the front-end dc/dc can be enabled or disabled). The hybrid modulation is implemented on Bridge III for both cases.

Fig. 17 compares the measured overall efficiency between three modulation schemes: 1) the proposed soft-switching scheme along with the hybrid modulation; 2) a conventional scheme with square-wave modulation and SPWM-3rd; and 3) hybrid modulation on Bridge III but without enabling the ZVZCS scheme on the front-end dc/dc converter. The proposed scheme can achieve the highest efficiency. The measured overall losses can be broken down into conduction and switching losses as given in Table II. The conduction losses are estimated based on the measured currents, while the switching losses are simply the difference between the overall losses and the conduction losses. As can be observed from Table II, the conduction losses are very close for three schemes, and the difference in the overall efficiency is determined by the switching losses. We can also infer that if switching losses become dominant in the overall losses, the proposed scheme will achieve better improvement on the overall efficiency over the conventional schemes.

The ratio of the overall switching losses of the RHFL converter prototype operating with the ZVZCS scheme over the SPWM-3rd scheme is experimentally measured using the method described earlier, and can be theoretically calculated. Both results are plotted in Fig. 18 for different output power factors. The similarity between the measured and calculated values verifies the loss calculation outlined in Section IV. Fig. 19 compares the calculated overall switching losses versus power factors of the RHFL converter prototype with the proposed and the other four conventional schemes mentioned in Section II. The formula used to calculate switch losses for these schemes is given in [21]. Results are normalized with respect to the SPWM-3rd scheme. The switching losses for S_c are not considered for all schemes since they are relatively small. It is concluded from Fig. 19 that the proposed scheme has the lowest overall switching losses during a wide range of power factors, especially when $|\varphi|$ is less than 30°. This is because there is no switching loss on Bridge II if $|\varphi| < 30°$, and the switching losses on Bridge I are small due to the usage of low-voltage, fast-speed MOSFETs. For larger $|\varphi|$, however, Bridge II may have high switching losses due to the utilization of high-voltage, slow-speed IGBTs, which could offset the benefit of switching losses reduction on Bridge III. Therefore, it is more preferable to apply the scheme for the aforementioned low-voltage dc to high-voltage ac applications.

TABLE II
LOSS BREAKDOWN UNDER DIFFERENT OUTPUT POWERS

	Loss Breakdown	P_{out} = 430W	P_{out} = 600W	P_{out} = 800 W	P_{out} = 1040W
Scheme (1)	Overall Loss (W)	46.40	64.50	84.28	102.49
	Conduction Loss (W)	41.83	54.55	67.45	83.63
	Switching Loss (W)	4.57	9.95	16.83	18.86
Scheme (2)	Overall Loss (W)	54.76	82.24	99.95	127.04
	Conduction Loss (W)	42.82	55.62	68.40	84.07
	Switching Loss (W)	11.94	26.62	31.54	42.98
Scheme (3)	Overall Losses (W)	55.39	75.67	97.24	119.67
	Conduction Loss (W)	42.70	55.01	68.29	85.21
	Switching Loss (W)	12.69	20.66	28.95	34.46

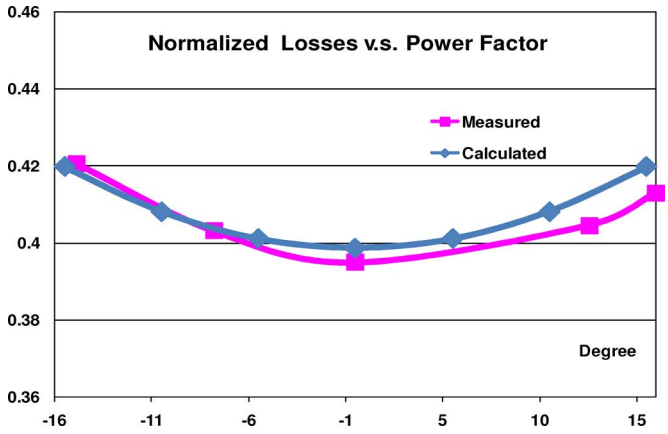


Fig. 18. Measured and calculated ratio of overall switching losses of an RHFL converter with the proposed soft-switching scheme and SPWM-3rd under different power factors.

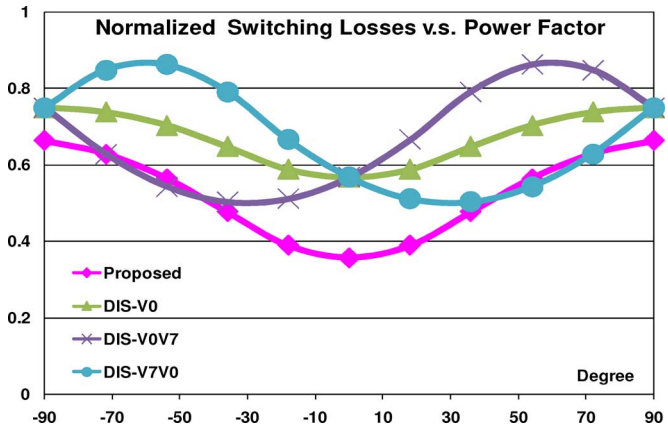


Fig. 19. Comparison of calculated ratio of overall switching losses for an RHFL converter with the proposed soft-switching scheme and other conventional schemes presented in Section II.

VII. CONCLUSION

A soft-switching scheme has been outlined for the front-end bidirectional full-bridge dc/dc converter of an RHFL three-phase PWM converter. It achieves ZCS for the primary side full-bridge active switches or ZVS for the secondary-side full-bridge active switches depending on the direction of the current (or power) flow. The body diodes on both bridges turn off softly, and no reverse-recovery problem arises. The proposed soft-switching scheme is valid for various load conditions, and can reduce the overall switching loss of the RHFL converter (as shown in Fig. 1) without adding a component. It is more suitable for low-voltage dc to high-voltage ac conversion.

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DISCLAIMER

The operation of Bridge III in this paper is covered by S. K. Mazumder, "Hybrid modulation of multiphase converter," USPTO Patent Application DB054 filed by the University of Illinois, Chicago, 2007 [1]. The operational details of the hybrid modulation scheme are outlined in [2] and [21]. They are referred, in brief, in this paper to describe the calculation of the overall loss of the HFL PWM converter operating with the soft-switching scheme for the front-end isolated dc/dc converter and with the aforementioned hybrid modulation scheme for the follow-up converter referred to as Bridge III.

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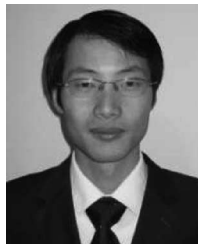

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