A Soft Switching Scheme for Multiphase DC/Pulsating-DC Converter for Three-Phase High-Frequency-Link Pulsewidth Modulation (PWM) Inverter

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***Abstract*—This paper outlines a switching scheme to improve the energy efficiency for an isolated high-frequency multiphase dc/pulsating-dc converter, which is the front end of a three-phase rectifier-type high-frequency-link inverter. Without using any auxiliary circuit, the proposed switching scheme achieves zero-current or zero-voltage switching for the power switches on the front-end multiphase dc/pulsating-dc converter. Moreover, on the back-end pulsating-dc/ac converter, the proposed soft-switching scheme reduces the switching frequency requirements for the associated switchers, which need high-frequency switching. In conjunction with the back-end pulsating-dc/ac converter, operating with a patent-filed hybrid modulation scheme, the proposed switching scheme leads to reduced overall switching loss as compared with other existing schemes. It is more suitable for isolated low-voltage dc to three-phase high-voltage ac applications from the standpoints of cost, efficiency, and footprint.**

***Index Terms*—High efficiency, high-frequency link, isolated three-phase inverter, soft switching.**

I. Introduction

HIGH-FREQUENCY transformer-isolated rectifier-type high-frequency-link (RHFL) pulsewidth modulation (PWM)-based inverter is a suitable topology for high-energy density inverters [1], especially in applications, where galvanic isolation is mandatory and low footprint is a necessity. Fig. 1 shows the schematic for a three-phase high-power high-frequency PWM-RHFL inverter supplied by a low-voltage dc source. It consists of a multiphase dc/pulsating-dc converter as the front end and a three-phase pulsating-dc/ac voltage-source inverter (VSI) as the back end. The multiphase dc/pulsating-dc converter has a structure similar to the conventional fixed-dc-link isolated dc/dc converter as proposed in [2], but without the dc-link filter. As compared to a resonant-link inverter [3], the PWM-RHFL inverter yields lower switch stress, better total harmonic distortion (THD), and eliminates the need for intermediate-stage filters. Further, unlike a PWM cycloconverter-type HFL inverter [4]–[6], the VSI-type structure provides inherent free-wheeling paths in Bridge III (shown in Fig. 1), which simplifies its switching scheme precluding the possibility of disruption of the load current. Therefore, the PWM-RHFL inverter approach, shown in Fig. 1, is better suited for the aforementioned low-voltage dc to three phase high-voltage ac conversion from the viewpoints of cost and portability. Nevertheless, it may experience high-switching loss because of three-stage high-frequency operation.

A novel hybrid modulation scheme outlined in [7]–[9] can reduce the switching loss of Bridge III by reducing its switching requirement and enabling zero-voltage-on. With hybrid modulation, the switches on two legs of Bridge III commutate at line-frequency with negligible switching loss, while the rest two switches on the third leg commutate under hard-switching condition at high frequency, which in [7]–[11] equals twice of the primary side switching frequency. As compared to the conventional SPWM hard-switching schemes, in which all switches operate at high frequency, the hybrid modulation achieves up to a 67% loss reduction on Bridge III. However, the switching loss may be still high, especially when slow switching-speed devices are used. Furthermore, to fully utilize the hybrid modulation, the link voltage needs to be a modulated high-frequency pulsating-dc, whose fundamental frequency equals to six times the output line frequency (i.e., 360 Hz for a 60-Hz output frequency). This requirement may cause relatively higher switching loss on the front-end stages.

This paper proposes a switching scheme based on zero-current-switching (ZCS) and zero-voltage-switching (ZVS) principles for the front-end multiphase dc/pulsating-dc converter shown in the shaded area of Fig. 1. It can not only reduce the switching loss on Bridge I by achieving ZVS/ZCS for the active switches without using any auxiliary circuit but also help to reduce the switching loss on Bridge III by enabling the third leg of Bridge III to operate at the same (instead of twice) switching frequency of the primary side. Therefore, in conjunction with the hybrid modulation, the proposed soft-switching scheme can improve the overall efficiency for the entire RHFL inverter.

This paper includes three more sections. The background and the overview of the proposed switching schemes are first described in Section II, followed by a detailed explanation on operating principles and soft-switching mechanisms in Section III.

Manuscript received July 31, 2009; revised December 7, 2009; accepted January 13, 2010. Date of current version June 18, 2010. The work of S. K. Mazumder was supported by the National Science Foundation under Award 0725887. Recommended for publication by Associate Editor J. A. Pomilio.

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Digital Object Identifier 10.1109/TPEL.2010.2042180

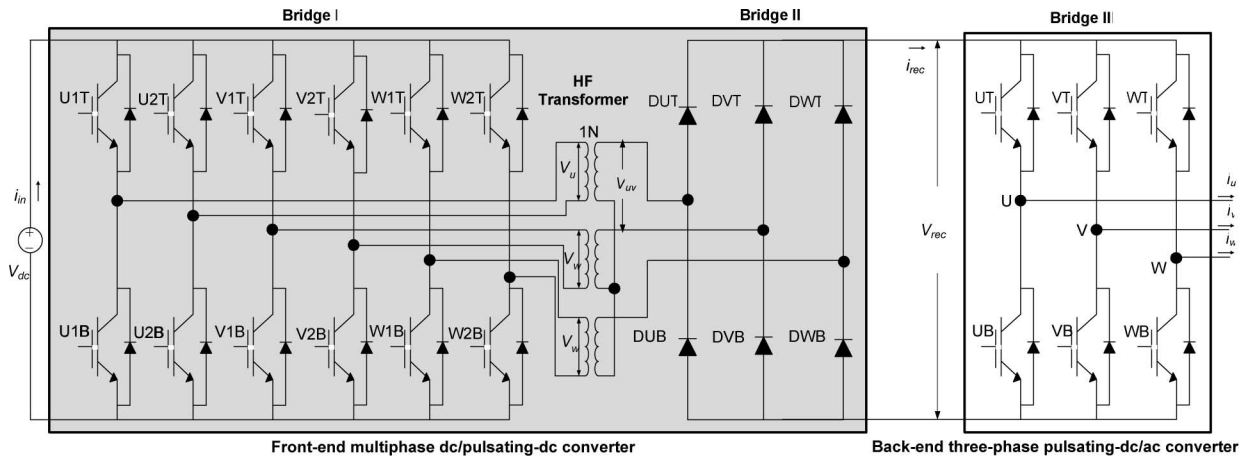

Fig. 1. Schematic of a three-phase RHFL inverter with a multiphase dc/pulsating-dc converter as front-end stage.

Finally, key experimental waveforms of a 3-kW prototype are presented to verify the operation of the converter and evaluate the switching scheme.

II. Proposed Switching Scheme for Front-end Multiphase DC/Pulsating-DC Converter

A. Circuit Schematic and Equivalent Circuit

As shown in the dotted block in Fig. 1, the front-end dc/pulsating-dc converter comprises two stages of conversion: 1) Bridge I: three single-phase high-frequency full-bridge inverters, operating at frequency of f_s, and 2) Bridge II: a three-leg diode rectifier, which outputs a unipolar pulsating-dc voltage with six-pulse envelope. It is noted that, a back-end three-leg pulsating-dc/ac converter (Bridge III) converts this high-frequency pulsating-dc voltage into a line-frequency PWM ac output. Three single-phase 1: N high-frequency (f_s Hz) transformers have Y-connections at secondary side. The inverter, as a whole, is referred as I633 in this paper. Note again that, although the front-end multiphase dc/pulsating-dc converter has a similar structure as a fix-dc-link converter proposed in [2], it does not require an intermediate dc-link filter and the switching schemes would be different.

The inverter I633 is suitable for low-voltage dc to high-voltage ac applications to support three-phase high watt-power loads with high power factor. A typical example is an isolated three-phase or multiphase inverter used in stand-alone bulky power plant [12], [13], or a fuel cell or photovoltaic panels powered grid-connected distributed generation injecting active power to the power grid [14], [15]. Although the diode rectifier is used as Bridge II, the inverter I633 can support limited range of reactive loads in addition to resistive loads. As presented in detail in [9], up to $\pm 30^\circ$ phase displacement is allowed for a balanced three-phase load. Other load conditions are also permitted as long as the currents flowing to Bridge III are nonnegative ($i_{\rm rec} \geq 0$ in Fig. 1).

The inverter I633 can be simplified into an equivalent circuit. As shown in Fig. 2, the outputs of the three single-phase full-bridge converters (Bridge I) are reflected on the secondary side of the transformer and denoted as V_{uo}, V_{vo}, and V_{wo}, respectively. Operating under the hybrid modulation scheme, Bridge III (shown in the dotted block) is modeled as a switching current source antiparalleled by a diode $\rm D_{III}$ [9], [11]. The transformer leakages are assumed to be equal for the three phases and designated by L_K. The output voltage and current of the front-end dc/pulsating-dc converter are referred to as $V_{\rm rec}$ and $i_{\rm rec}$, respectively. The positive directions for all aforementioned parameters are illustrated in Fig. 2. This equivalent model will be used in Section III to analyze soft switching of Bridge I.

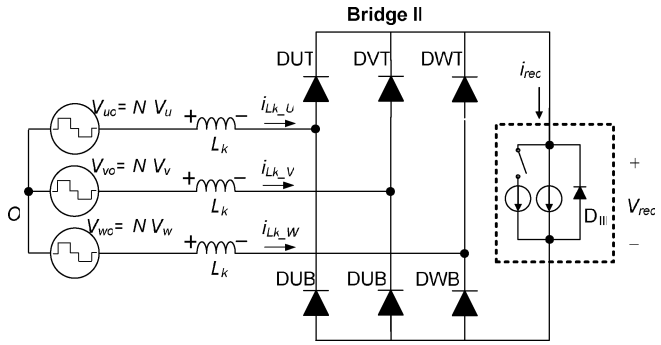

Fig. 2. Equivalent circuit of Fig. 1 by eliminating transformers and simplifying Bridge III

B. General Requirement for Switching Scheme for Bridge I

Phase voltages V_{uo}, V_{vo}, and V_{wo} on the secondary side equal N times the corresponding voltage V_u, V_v, and V_w on the primary side. Each of V_u, V_v, and V_w can be either a two-level ($V_{\rm dc}$ and $-V_{\rm dc}$) or a three-level ($V_{\rm dc}$, $-V_{\rm dc}$, and 0) bipolar voltage depending on the switching schemes of the primary side full-bridges. Only three-level voltage case will be considered in this paper. To utilize a high-frequency transformer (f_s Hz), the average value of each voltage V_u, V_v, and V_w in one switching

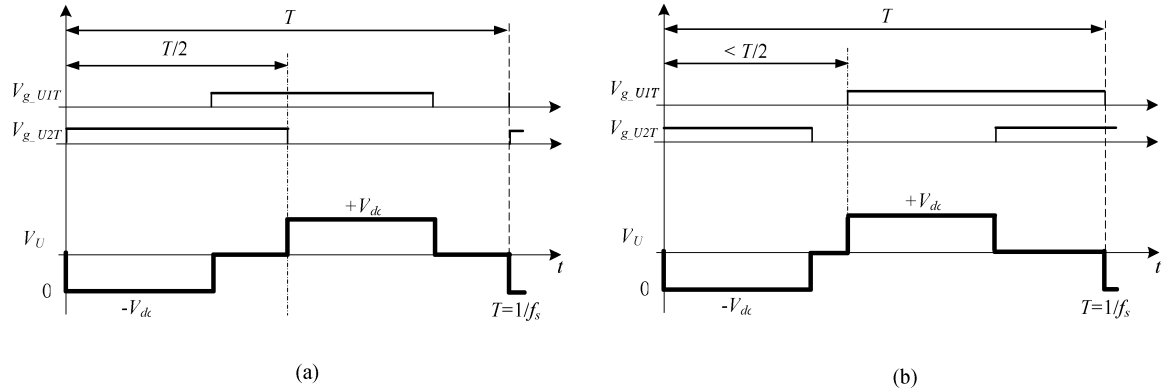

Fig. 3. Two types of phase-shift control for full-bridge based on (a) symmetrical duty cycle and (b) asymmetrical duty cycle.

period $T = 1/f_s$ should equal to zero, i.e.,

$$\begin{cases} \int_0^T V_u \, dt = 0 \\ \int_0^T V_v \, dt = 0 \\ \int_0^T V_w \, dt = 0. \end{cases} \tag{1}$$

Neglecting the transformer-leakage effect, the rectification function of Bridge II can be mathematically expressed as

$$V_{\rm rec} = N \left\{ \max\left(V_u, V_v, V_w,\right) - \min\left(V_u, V_v, V_w,\right) \right\}. \tag{2}$$

In order to utilize the hybrid modulation scheme on Bridge III, the output voltage $V_{\rm rec}$ should be six-pulse modulated [7]–[11]. In other words, the average value of $V_{\rm rec}$ in a particular switching cycle (denoted as T_i) should be proportional to the sample value of a six-pulse reference in the same switching cycle, i.e.,

$$\int_0^T V_{\rm rec} \, dt = 2NV_{\rm dc} \, ref6(T_i) \tag{3}$$

where $ref6(T_i)$ in (3) is the sampled value of the six-pulse reference $ref6(t)$ in the switch cycle T_i. Reference $ref6(t)$ spreads across six regions P1–P6 in one line cycle, and is obtained by rectifying a three-phase ac reference signal $u^*(t)$, $v^*(t)$, and $w^*(t)$, as defined in (4) and (5)

$$ref6(t) = \begin{cases} w^*(t) - v^*(t), & \text{P1:} \quad -\pi/6 \le \omega t < \pi/6 \\ u^*(t) - v^*(t), & \text{P2:} \quad \pi/6 \le \omega t < \pi/2 \\ u^*(t) - w^*(t), & \text{P3:} \quad \pi/2 \le \omega t < 5\pi/6 \\ v^*(t) - w^*(t), & \text{P4:} \quad 5\pi/6 \le \omega t < 7\pi/6 \\ v^*(t) - u^*(t), & \text{P5:} \quad 7\pi/6 \le \omega t < 3\pi/2 \\ w^*(t) - u^*(t), & \text{P6:} \quad 3\pi/2 \le \omega t < 11\pi/6 \end{cases} \tag{4}$$

$$\begin{cases} u^*(t) = m \sin(\omega t) \\ v^*(t) = m \sin\left(\omega t - 2\pi/3\right) \\ w^*(t) = m \sin\left(\omega t + 2\pi/3\right) \end{cases} \tag{5}$$

where m is the amplitude of the three-phase ac signal. For simplicity, $ref6(t)$ is limited to 0 and 1 (i.e., $0 \le ref6(t) \le 1$). Therefore, $m = 0.577$ MI, where MI stands for modulation index, and $0 <$ MI < 1. The three full-bridges need to be switched properly to satisfy the requirements given in (1) and (3).

C. Symmetrical and Asymmetrical Duty-Cycle-Based Phase-Shift Control

Phase-shift control is widely used in two-leg transformer-isolated full-bridge converter to reduce the switching loss by means of achieving zero-voltage turn-ON of switches [16]. Phase-shift control can be implemented using symmetrical and asymmetrical duty-cycle control [17], [18], although symmetrical duty-cycle control is mostly used. Fig. 3 plots the gate signals of the upper two switches for phase *U*, and the obtained output voltage V_U as a general example for a two-leg full-bridge modulated by symmetrical and asymmetrical duty-cycle-based phase-shift control schemes. For symmetrical control, as shown in Fig. 3(a), both upper and lower side switches on the same leg turn ON for same amount of time ($T/2$). As a result, the time distance between the two rising edges or between the two falling edges of V_U is fixed to $T/2$. Note that the gate signals of the lower side switches are omitted in Fig. 3 since they are always complementarily switched as compared to their upper counterparts. On the other hand, for asymmetrical control, one switch may conduct longer time than the other one in the same leg, and the time difference between the two rising edges or between the two falling edges of V_U is adjustable. The difference between Fig. 3(a) and (b) shows that, the asymmetrical duty-cycle-based phase-shift control has one more freedom in determining the positions of the waveforms than the symmetrical control. Fig. 3(a) and (b) indicates that the pulsewidth of voltage V_U for both schemes can be controlled by changing the phase difference between the two upper gate signals.

D. Existing Switching Schemes for Bridge I with Symmetrical Duty-Cycle-Based Phase-Shift Control

All previously proposed schemes apply symmetrical duty-cycle-based phase-shift control to each of three full-bridges on Bridge I. As a result, the obtained three three-level bipolar outputs V_u, V_v, and V_w have the same shapes but different phases. Fig. 4(a) and (b) plots voltages V_u, V_v, V_w, and $V_{\rm rec}$ in switching cycle T_i for two switching schemes proposed in [2] and [11], respectively. As shown in Fig. 4(a) and (b), all positive or negative pulses of V_u, V_v, and V_w have the same width β. In addition, voltage V_u leads V_v by a time of γ_{uv}, and V_v leads V_w by γ_{vw}. In [2], γ_{uv} and γ_{vw} are equal and fixed to $T/3$. As shown in

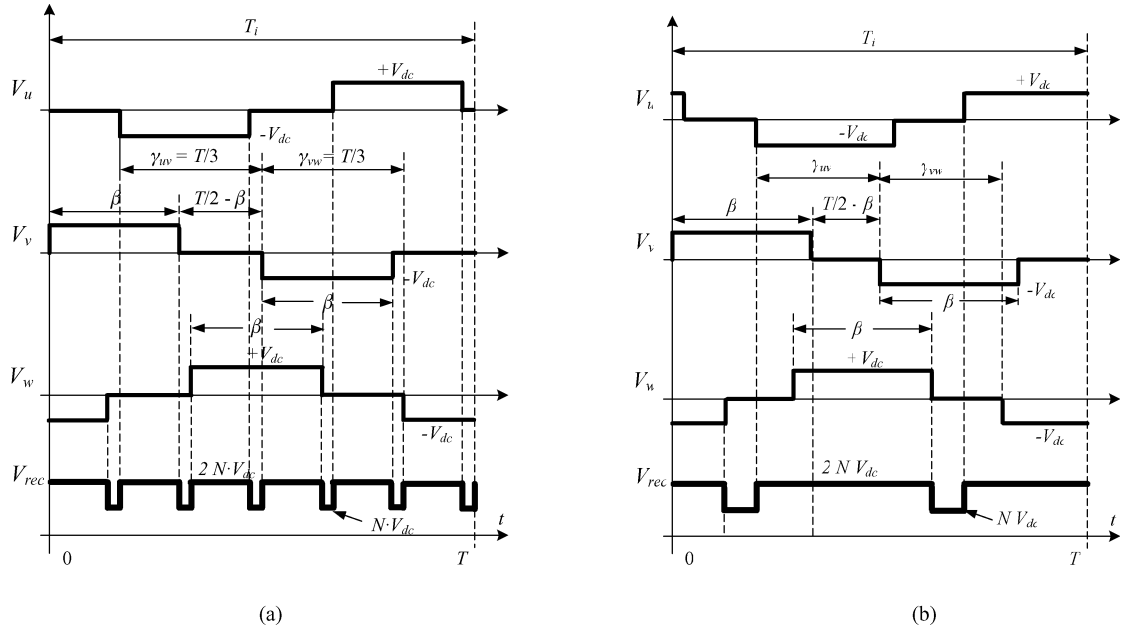

Fig. 4. Two existing switching schemes using symmetrical duty cycle-based phase-shift control for Bridge I: (a) scheme proposed in [2] with 6-f_s pulsating dc and (b) scheme proposed in [11] with 2-fs pulsating dc.

Fig. 4(a), the obtained output voltage $V_{\rm rec}$ will be a pulsating-dc with six times of switch frequency ($6f_s$), if $\beta < T/3$. The average value of $V_{\rm rec}$ over T_i, denoted as $\langle V_{\rm rec}\rangle|_{Ti}$, equals 3β ($2NV_{\rm dc}$) or *ref6*(T_i) T ($2NV_{\rm dc}$), if we let $\beta = (T/3)$ *ref6*(T_i). Huang and Mazumder [11] propos another scheme, which can reduce the pulsating frequency of $V_{\rm rec}$ to twice the switching frequency ($2f_s$) by varying both β and γ, as illustrated in Fig. 4(b). The obtained $\langle V_{\rm rec}\rangle|_{Ti}$ equals *ref6*(T_i) T ($2NV_{\rm dc}$), if $\gamma_{uv} = \gamma_{vw} =$ *ref6*(T_i) $T/2 - \beta/2$.

As explained in [7]–[10], in order to simplify the implementation of hybrid modulation in practice, it is preferable to switch the third leg on Bridge III in synchronism with each pulse of the link voltage $V_{\rm rec}$. In other words, the switching frequency of the third leg on Bridge III under hybrid modulation should be at least $2f_s$ for the aforementioned two schemes. To further reduce the frequency of the output voltage $V_{\rm rec}$, asymmetrical duty-cycle-based phase-shift control can be applied to primary-side full bridges.

E. Proposed Switching Schemes with Reduced Pulsating Frequency

The proposed switching scheme for the frond-end dc/pulsating-dc stage employs asymmetrical duty-cycle-based phase-shift control. It can reduce the frequency of $V_{\rm rec}$ into switching frequency ($1f_s$). The principle is illustrated in Fig. 5 over one switching period. As shown in Fig. 5, the outputs of the three full-bridges V_u, V_v, and V_w are all three-level bipolar voltages. Each voltage has two rising and two falling instants. The time instants when the voltage jumps from zero to a negative value are denoted as t_{u1}, t_{v1}, and t_{w1}, and the time instants when the voltage jumps from zero to a positive value are denoted as t_{u3}, t_{v3}, and t_{w3}, respectively. The time instants for other voltage jump are denoted in a similar manner and are all

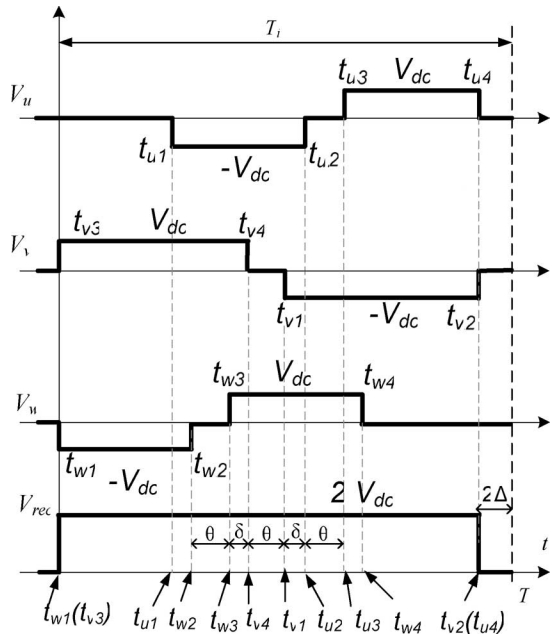

Fig. 5. Proposed switching scheme for Bridge I with 1-f_s pulsating dc.

given in Fig. 5. Thanks to the asymmetrical duty-cycle based control, the aforementioned time instants can be placed freely as long as (1) and (3) satisfy. Equations (1) and (3) can be rewritten, respectively, as

$$\begin{cases} t_{u2} - t_{u1} = t_{u4} - t_{u3} \\ t_{v2} - t_{v1} = t_{v4} - t_{v3} \\ t_{w2} - t_{w1} = t_{w4} - t_{w3} \end{cases} \tag{6}$$

and

$$t_{u4} - t_{w1} = ref6\,(T_i)\,T. \tag{7}$$

According to the proposed scheme, the following additional constraints are added

$$t_{w1} = t_{v3} \text{ and } t_{v2} = t_{u4} \tag{8}$$

$$t_{v4} > t_{w3} \text{ and } t_{u2} > t_{v1} \tag{9}$$

$$t_{w4} > t_{u3} \text{ and } t_{w2} > t_{u1}. \tag{10}$$

Practically, the exact alignment of t_{w1} with t_{v3} and of t_{v2} with t_{u4} may not possible, but the difference should be minimized to reduce the distortion. Equations (6)–(10) lead to a two-level output voltage $V_{\rm rec}$ with pulsating frequency of f_s Hz, which simplifies the control requirement and reduces the switching loss for Bridge III. For further simplicity, we add two more constraints

$$t_{u3} - t_{u2} = t_{v1} - t_{v4} = t_{w3} - t_{w2} \triangleq \theta \tag{11}$$

$$t_{u2} - t_{u1} = t_{v2} - t_{v1}. \tag{12}$$

From (12), we have

$$t_{v4} - t_{w3} = t_{u2} - t_{v1} \triangleq \delta. \tag{13}$$

Combing (6)–(13), the time intervals of $t_{u1} - t_{w4}$ can be expressed as, (14), as shown at the bottom of the page.

The value of δ is usually small as long as (9) is satisfied. As will be explained later, the length of θ should be sufficient for ZCS and the upper limit is given as follows according to (10)

$$7\theta + 6\delta < \mathit{ref6}\,(T_i)\,T. \tag{15}$$

Comparing Fig. 5 with Fig. 4, the frequency of the link voltage $V_{\rm rec}$ is $1f_s$. This reduced the switching frequency on Bridge III by 50% as compared to the existing schemes having $2f_s$ pulsating-dc in [9]–[11]. Moreover, the proposed switching scheme achieves zero-current or zero-voltage turn-ON and zero-current turn-OFF for the active switches on Bridge I without additional components.

III. Operating Principles and Soft Switching of Bridge I

The operating principles of the front-end multiphase dc/pulsating-dc converter (shown in Fig. 1) under the proposed switching scheme and the mechanisms of achieving soft switching (ZCS or ZVS) for Bridge I are presented in this section. The simplified circuit as shown in Fig. 2 is used for the analysis. The transformer leakage effect is considered. The variables used in this section and their positive directions are illustrated in Fig. 2. The analysis is based on the following assumptions.

A. Assumptions

1) Dead time between the two switches on the same leg of Bridge I is required but not considered here.
2) Unless point out specifically, voltage drops of each diode on Bridges II and III, denoted as $V_{\rm FDII}$ and $V_{\rm FDIII}$, respectively, are negligible.
3) The negative rising edge of V_w happens slightly earlier than the positive rising edge of V_v (i.e., $t_{w1} < t_{v3}$ in Fig. 5). The analysis and results will be similar if one assumes $t_{w1} \geq t_{v3}$.
4) All switches are assumed to be ideal.

B. Bridge II Output Current $i_{\rm rec}$

Within one switching cycle, the output current of Bridge II ($i_{\rm rec}$) changes once in every switching cycle due to the hybrid modulation [7]–[9] of Bridge III. This change of the current, however, always occurs within the areas where $V_{\rm rec} \neq 0$ (i.e., $t_{w1} < t < t_{u4}$ in Fig. 5). As will be explained in the following, the changes of $i_{\rm rec}$ in these ranges will not significantly affect the soft-switching performance of Bridge I. Therefore, for simplicity, $i_{\rm rec}$ can be assumed to be constant between t_{w1} and t_{u4}, where $V_{\rm rec} \neq 0$. The value of the current, however, may vary for different switching cycles. For the ith switching cycle (denoted as T_i), the value of the current $i_{\rm rec}$ is denoted as $I_d(T_i)$ for $t_{w1} < t < t_{u4}$. For other areas shown in Fig. 5, where $V_{\rm rec} = 0$, the current $i_{\rm rec}$ will decrease with a rate of $(2V_{\rm FDII} - V_{\rm FDIII})/(2L_K)$. Therefore, Bridge II output current $i_{\rm rec}$ in the switching cycle T_i is given as

$$i_{\rm rec}(t) = \begin{cases} I_d\,(T_i)\,, & \text{if } t_{w1} < t < t_{u4} \\ I_d\,(T_i) - \frac{2V_{\rm FDII} - V_{\rm FDIII}}{2L_K}\,(t - t_{u4})\,, & \text{otherwises} \end{cases}. \tag{16}$$

Depending on the circuit parameters, Bridge II output current $i_{\rm rec}$ can be either larger than zero or equal zero at the end of a switching cycle (i.e., $t = T$). If $i_{\rm rec}(T) > 0$, the circuit is operating in continuous-current mode (CCM) in this cycle. On the other hand, if $i_{\rm rec}(T) = 0$, the circuit is operating in discontinuous-current mode (DCM) in this cycle.

C. Modes of Operations

Fig. 6 shows the waveforms of the gate signals of the upper six switches and the transformer (leakage) current for each of the three phases in a typical switching cycle T_i. The output voltage of Bridge II ($V_{\rm rec}$) considering the transformer leakage effect is also plotted in Fig. 6. The waveform is different from the ideal waveform shown in Fig. 5. The three voltages V_{uo}, V_{vo}, and V_{wo} are appended on top of their corresponding transformer currents. The modes of operation are explained as follows.

The switching-cycle starts at t_1 when switch *W1*T turns OFF while switch *W1B* turns ON, voltage V_{wo} jumps from zero to $-NV_{\rm dc}$. Before t_1 (or $t = t_1-$), $V_{uo} = V_{vo} = V_{wo} = 0$, and $V_{\rm rec} = 0$. Three transformer currents $i_{LK\_U} = i_{\rm rec}(t_1-)$, $i_{LK\_V} = -i_{\rm rec}(t_1-)$, and $i_{LK\_W} = 0$. For CCM

$$\begin{cases} t_{u1} = 2\theta + 2\delta & t_{u2} = 0.5\,[\mathit{ref6}\,(T_i)\,T + \theta] + \delta & t_{u3} = 0.5\,[\mathit{ref6}\,(T_i)\,T + 3\theta] + \delta & t_{u4} = \mathit{ref6}\,(T_i)\,T \\ t_{v1} = 0.5\,[\mathit{ref6}\,(T_i)\,T + \theta] & t_{v2} = \mathit{ref6}\,(T_i)\,T & t_{v3} = 0 & t_{v4} = 0.5\,[\mathit{ref6}\,(T_i)\,T - \theta] \\ t_{w1} = 0 & t_{w2} = 0.5\,[\mathit{ref6}\,(T_i)\,T - 3\theta] - \delta & t_{w3} = 0.5\,[\mathit{ref6}\,(T_i)\,T - \theta] - \delta & t_{w4} = \mathit{ref6}\,(T_i)\,T - 2\theta - 2\delta. \end{cases} \tag{14}$$

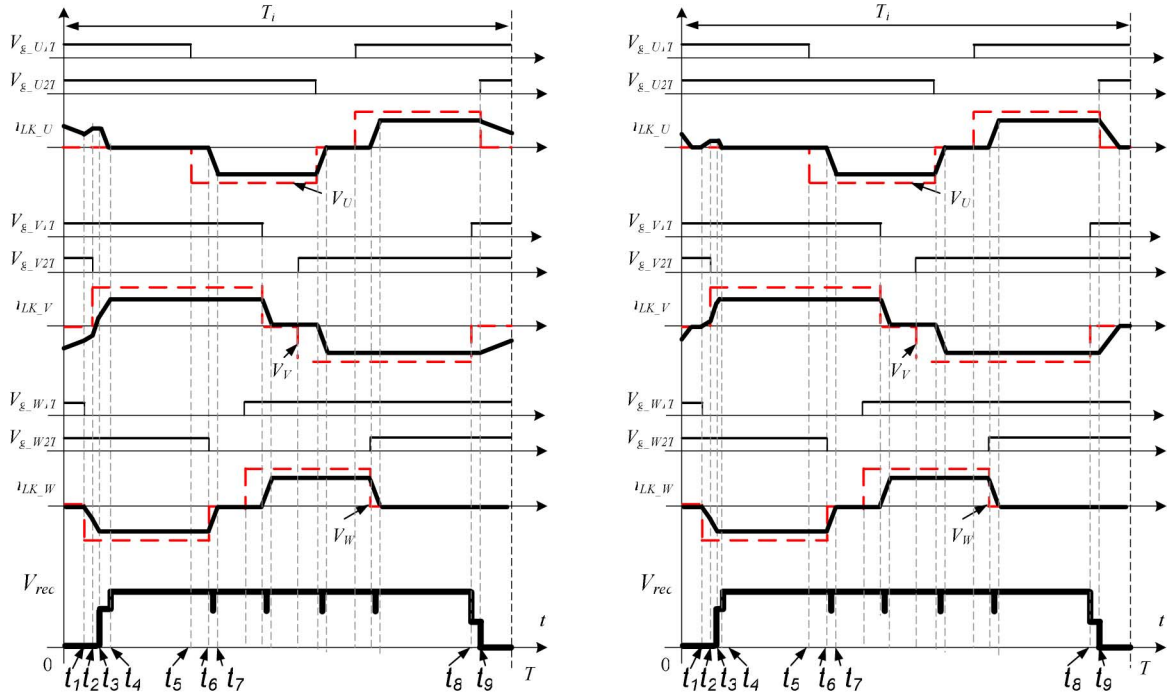

Fig. 6. Gate drive signals for six upper switches and the three-phase leakage currents when Bridge II output current $i_{\rm rec}$ is (a) continuous and (b) discontinuous.

operation, diodes DUT, DVB on Bridge II and D_{III} on Bridge III are conducting at t_1, while for DCM, only D_{III} conducts.

Mode 1 [$t_1 < t < t_2$, Fig. 7(a)]: At t_1, switch *W1T* turns OFF (*W1B* turns ON), and V_{wo} jumps from 0 to $-NV_{\rm dc}$. Diode DWB starts to conduct to share current with DVB. Voltage $V_{\rm rec}$ still remains at 0. The equivalent circuit is shown in Fig. 7(a)

$$\frac{L_K di_{LK\_U}}{dt} = \frac{L_K di_{LK\_V}}{dt} \tag{17}$$

$$\frac{L_K di_{LK\_U}}{dt} - \frac{L_K di_{LK\_W}}{dt} - NV_{\rm dc} = 0 \tag{18}$$

$$\frac{L_K di_{LK\_U}}{dt} + \frac{L_K di_{LK\_V}}{dt} + \frac{L_K di_{LK\_W}}{dt} = \frac{L_K d\left(i_{LK\_U} + i_{LK\_V} + i_{LK\_W}\right)}{dt} = 0. \tag{19}$$

By solving (17)–(19), we obtain

$$\frac{L_K di_{LK\_U}}{dt} = \frac{1}{3}NV_{\rm dc}, \quad \frac{L_K di_{LK\_V}}{dt} = \frac{1}{3}NV_{\rm dc}, \quad \frac{L_K di_{LK\_W}}{dt} = -\frac{2}{3}NV_{\rm dc}. \tag{20}$$

From (20), current i_{LK_W} rises (in negative direction) at a finite rate determined by $(2/3(NV_{\rm dc}))/L_k$. Therefore, the turning on loss of *W*1B is small although the turn-ON is not strictly ZCS. Obviously, switch *W1T* turns OFF under ZCS condition.

Mode 2 [$t_2 < t < t_3$, Fig. 7(b)]: Mode 1 ends at t_2, when *V2T* turns OFF, and *V*2B turns ON. For CCM operation, *V2B* turns ON at ZCS since i_{LK_V} (t_2) is negative. The turn-ON of *V2B* can be also regarded as a ZVS on since the current will first discharge the body capacitor of *V2B* and may conduct through its antiparallel diode. The effectiveness of ZVS relies on whether the leakage current (or energy) is large enough to fully discharge the parasitic capacitors as explained in the conventional dc/dc converter with phase-shift control [16]. Therefore, it is a conditional ZVS turn-ON. For DCM, the turn-ON of *V2B* is not strictly ZCS, similarly as the turn-ON of *W1B* in Mode 1.

At t_2, V_{vo} jumps from 0 to $NV_{\rm dc}$, but diode D_{III} still conducts and $V_{\rm rec}$ remains at 0. Equation (21) can be obtained from the equivalent circuit [shown in Fig. 7(b)]

$$\frac{L_K di_{LK\_U}}{dt} - \frac{L_K di_{LK\_V}}{dt} + NV_{\rm dc} = 0. \tag{21}$$

Combining with (18) and (19), we obtain

$$\frac{L_K di_{LK\_U}}{dt} = 0, \frac{L_K di_{LK\_V}}{dt} = NV_{\rm dc}, \frac{L_K di_{LK\_W}}{dt} = -NV_{\rm dc}. \tag{22}$$

Current i_{LK_U} is unchanged in this mode, while i_{LK_V} and i_{LK_W} increase in positive and negative directions, respectively, with a higher slope than those in Mode 1. Mode 2 ends when i_{LK_W} equals $I_d(T_i)$.

Mode 3 [$t_3 < t < t_4$, Fig. 7(c)]: At t_3, i_{LK_W} reaches-$I_d(T_i)$ and causes D_{III} to block. Voltage $V_{\rm rec}$ rises from zero. The

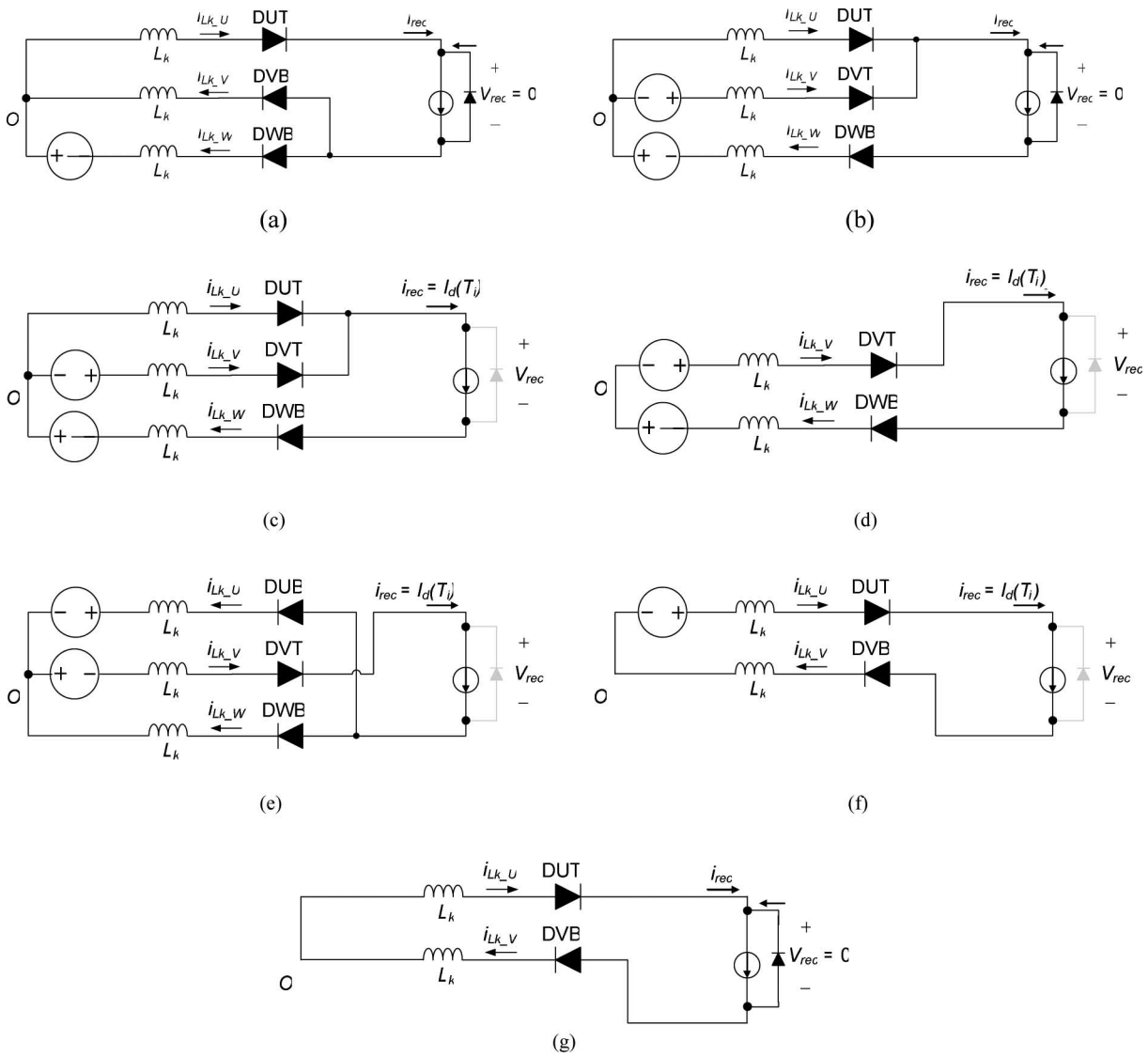

Fig. 7. Modes of operation explained using equivalent circuits: (a) Mode 1 ($t_1 < t < t_2$), (b) Mode 2 ($t_2 < t < t_3$), (c) Mode 3 ($t_3 < t < t_4$), (d) Mode 4 ($t_4 < t < t_5$) and Mode 5 ($t_5 < t < t_6$), (e) Mode 6 ($t_6 < t < t_7$), (f) Mode 7 ($t_8 < t < t_9$), and (g) Mode 8 (CCM) ($t_9 < t < T$).

equivalent circuit changes to Fig. 7(c) with the following:

$$i_{LK\_U} + i_{LK\_V} = I_d\,(T_i) \rightarrow \frac{L_K\, di_{LK\_U}}{dt} = -\frac{L_K\, di_{LK\_V}}{dt} \tag{23}$$

$$\frac{L_K\, di_{LK\_U}}{dt} + V_{\rm rec} - \frac{L_K\, di_{LK\_W}}{dt} - NV_{\rm dc} = 0. \tag{24}$$

Combining (23), (24) with (19) and (21), which still hold in this mode, we obtain $V_{\rm rec} = 3/2(NV_{\rm dc})$ and

$$\frac{L_K\, di_{LK\_U}}{dt} = -\frac{1}{2}NV_{\rm dc}, \qquad \frac{L_K\, di_{LK\_U}}{dt} = \frac{1}{2}NV_{\rm dc},$$
$$\frac{L_K\, di_{LK\_W}}{dt} = 0. \tag{25}$$

Mode 4 [$t_4 < t < t_5$, *Fig. 7(d)]:* At t_4, currents i_{LK_V} and i_{LK_U} reaches $+I_d(T_i)$ and zero, respectively. Current $i_{LK\_W} = -I_d(T_i)$. Voltage across each leakage inductance equals zero. $V_{\rm rec} = 2NV_{\rm dc}$. Diodes DVT and DWB conduct as shown in the equivalent circuit in Fig. 7(d).

Mode 5 ($t_5 < t < t_6$)*:* At t_5, switch $U1T$ turns OFF and $U1B$ turns ON with ZCS. V_{uo} jumps from 0 to -$NV_{\rm dc}$ as a result. However, three leakage currents and $V_{\rm rec}$ remain unchanged. It is because V_{wo} equals V_{uo} and no commutation voltage exists. The equivalent circuit is the same as of Mode 4.

Mode 6 [$t_6 < t < t_7$, *Fig. 7(e)]:* Voltage V_{wo} changes from $-NV_{\rm dc}$ to 0 at t_6 when $W2T$ turns OFF and $W2B$ turns ON. The equivalent circuit [shown in Fig. 7(e)] and the current analysis are similar with Mode 3. Current will shift from phase W to phase U with a rate determined by $NV_{\rm dc}/(2L_K)$ and $V_{\rm rec} = 3/2(NV_{\rm dc})$. This commutation process ends at t_7, when $i_{LK\_U} = -I_d(T_i)$ and $i_{LK\_U} = 0$. $W2B$ turns ON at t_6 with zero-current condition.

Note from Mode 4–6 that, at the negative rising edge of $V_{uo}(t_5)$, switches $U1T$ and $U1B$ have ZCS switching because Phase U current i_{LK_U} remains at zero at this point due to the fact that the current commutation does not happen at t_5 but wait until the followed falling edge of $V_{wo}(t_6)$. Furthermore, switch $W2B$ turns ON with ZCS at t_6 since i_{LK_W} decays and stays at zero after that. Note that, to ensure the ZCS, the length of θ should larger than the time duration of Mode 6.

Three more commutations occur between t_7 and t_8, respectively. Each of them is based on the same operating principles and has similar soft-switching performance as described in Modes 4–6. The switches that turn ON and OFF at the rising edges (positive or negative) of phase voltages (V_{uo}, V_{vo}, or V_{wo}) will have ZCS. The switches that turn ON at the falling edges (positive or negative) of these three voltages will have ZCS. However, the switches that turn OFF at the falling edges of the three voltages will have hard turn-OFF. This performance always holds regardless of the change of $i_{\rm rec}$ as long as the commutation occurs between t_4 and t_8, where $V_{\rm rec} = 2NV_{\rm dc}$ and θ [defined in (11)] is sufficient.

Mode 7 [$t_8 < t < t_9$, Fig. 7(f)]: At t_8, switch $V1B$ turns OFF and switch $V1T$ turns ON, respectively, to bring the voltage V_{vo} back to zero. The output voltage $V_{\rm rec} = 1/2NV_{\rm dc}$. The leakage currents for three phases are not affected because no voltage drop applies across the leakage inductance. Switch $V1T$ turns ON with zero-voltage since the load current will freewheel through its anti-parallel diode after $V1B$ turns OFF. The equivalent circuit is shown in Fig. 7(f).

Mode 8 [$t_9 < t < T$, Fig. 7(g)]: At t_9, switches $U2B$ and $U2T$ turn OFF and turn ON, respectively, to bring the voltage V_{uo} back to zero. Similar to switch $V1T$ in Mode 7, $U2T$ turns ON under conditional ZVS or ZCS condition. All three full-bridges output voltages are $V_{uo} = V_{vo} = V_{wo} = 0$, and $V_{\rm rec} = 0$. Three transformer currents are $i_{LK\_U} = i_{\rm rec}$, $i_{LK\_V} = -i_{\rm rec}$, and $i_{LK\_W} = 0$. Two diodes on Bridge II DUT and DVB conduct. Diode $D_{\rm III}$ on Bridge III also conducts. The equivalent circuit is shown in Fig. 7(g). The Bridge II output $i_{\rm rec}$ decreases at the rate of $(2V_{\rm FDII} - V_{\rm FDIII})/(2L_K)$ as given in (16). This mode ends at the end of this switching cycle.

D. Summary of Soft Switching

The key results of the available soft switching for total 12 switches on Bridge I can be observed from Fig. 4(a) (for CCM) and (b) (for DCM), respectively. They are summarized in Table I. The marks of "ZVS" and "ZCS" in Table I indicate that the particular switch has zero-voltage or ZCS, and "HS" means hard-switching. The marks of "ZVS*" and "ZCS*" indicate conditional zero-voltage or ZCS, respectively. The switches under conditional ZVS turn-ON may still have turn-ON loss since its effectiveness relies on whether the stored leakage energy is large enough to fully discharge the parasitic capacitors. The switches under conditional ZCS turn ON under a nonstrict zero-current condition, but the rising rate of the switch current is limited by the leakage inductances. Table I also shows that, some switches may turn ON under either ZVS or ZCS condition.

TABLE I
SUMMARY OF THE AVAILABLE SOFT SWITCHING OF BRIDGE I

	CCM		DCM	
	U1T	**U2T**	**U1T**	**U2T**
Turn-on	ZCS	ZVS/ZCS	ZCS	ZVS/ZCS
Turn-off	ZCS	HS	ZCS	HS
	V1T	**V2T**	**V1T**	**V2T**
Turn-on	ZVS/ZCS	ZCS	ZVS/ZCS	ZCS
Turn-off	HS	HS	HS	ZCS
	W1T	**W2T**	**W1T**	**W2T**
Turn-on	ZCS	ZVS*/ZCS	ZCS	ZVS*/ZCS
Turn-off	ZCS	HS	ZCS	HS
	U1B	**U2B**	**U1B**	**U2B**
Turn-on	ZCS	ZVS*/ZCS	ZCS	ZVS*/ZCS
Turn-off	ZCS	HS	ZCS	HS
	V1B	**V2B**	**V1B**	**V2B**
Turn-on	ZVS*/ZCS	ZVS*	ZVS*/ZCS	ZCS*
Turn-off	HS	ZCS	HS	ZCS
	W1B	**W2B**	**W1B**	**W2B**
Turn-on	ZCS*	ZVS*/ZCS	ZCS*	ZVS*/ZCS
Turn-off	ZCS	HS	ZCS	HS

TABLE II
MAIN COMPONENTS USED IN PROTOTYPE (X = U, V, W)

NAME	PART NUMBER AND DESCRIPTIONS
X1T,X2T, X1B, X2B	IPP070N06L;MOSFET, 60V/80A/6.7mΩ
XT, XB	SiC MOSFET, 600V/20A, $R_{ds(on)}$ =0.125Ω,
DXT, DXB	IDT016S60C, SiC Schottky Diode, 600V/16A/1.5V_F
Transformers	Nanocrystalline core; Primary: 12T 6 x AWG14; Secondary: 52T, AWG14

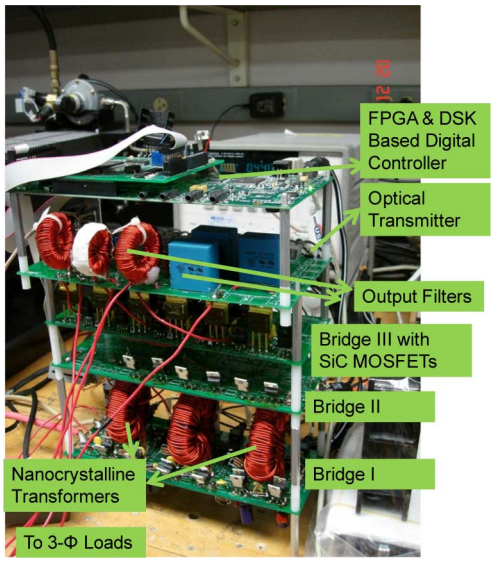

Fig. 8. Picture of the experimental prototype.

IV. EXPERIMENTAL RESULTS

A. Experimental Setup and Component Parameters

A 3-kVA prototype of inverter I633 (schematic shown in Fig. 1) was designed to validate the proposed switching scheme.

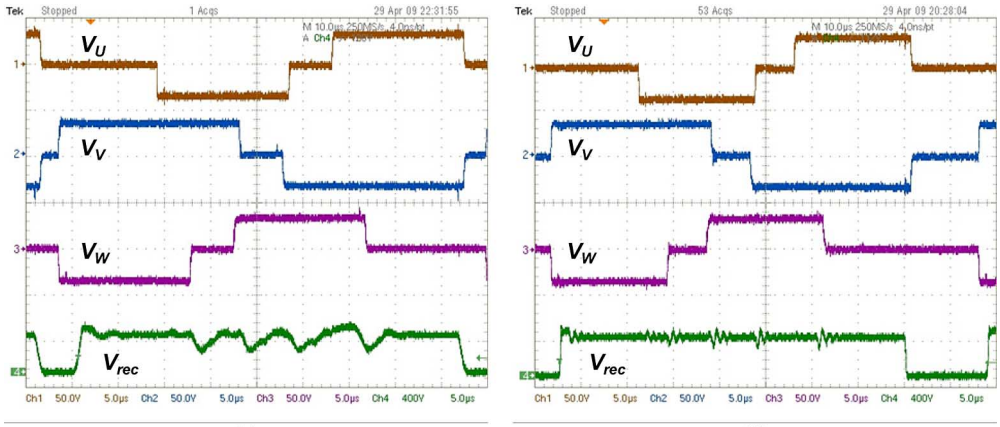

Fig. 9. Experimental voltage waveforms of three full-bridge outputs: V_U (50 V/div.), V_V (50 V/div.), V_w (50 V/div), and Bridge II output $V_{\rm rec}$ (400 V/div.) captured in one switching cycle (5 μs/div.) for (a) CCM and (b) DCM operations.

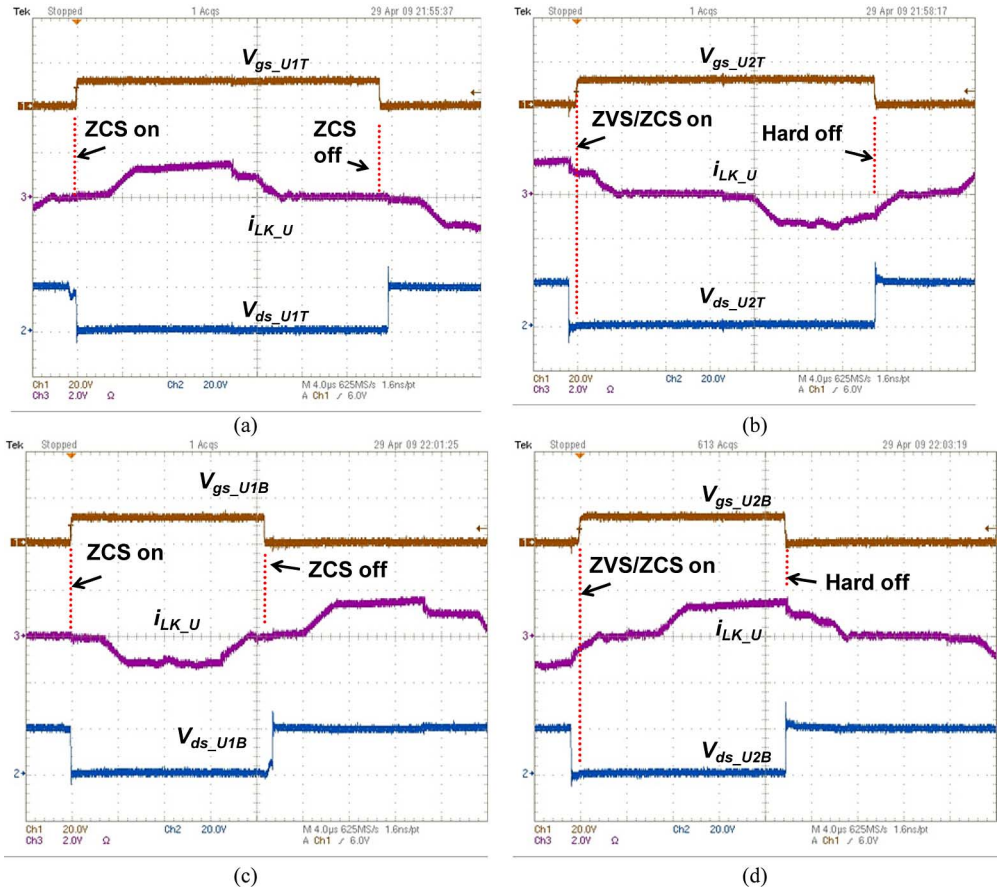

Fig. 10. Soft switching of the four devices on the phase *U* of Bridge I: (a) *U*1*T*, (b) *U*2*T*, (c) *U*1*B*, and (d) *U*2*B* for CCM operation. Waveforms from top-to-bottom for each picture are: gate drive voltage (20 V/div.), transformer U secondary current (20 A/div.), and voltage across the associated device (20 V/div.).

The rated input voltage is 36 V dc and output voltage is 208 V ac (line-to-line). Switching frequency f_s is 21.6 kHz. Transformer turns ratio is around 1:4.2. The components used for the inverter are listed in Table II. The picture of the prototype is shown in Fig. 8.

The prototype was tested for both CCM and DCM operations. To ensure CCM operation, a 56-μH inductor is connected externally at the secondary side of each transformer. No external inductance is used for DCM operation. The experimental results are presented as follows.

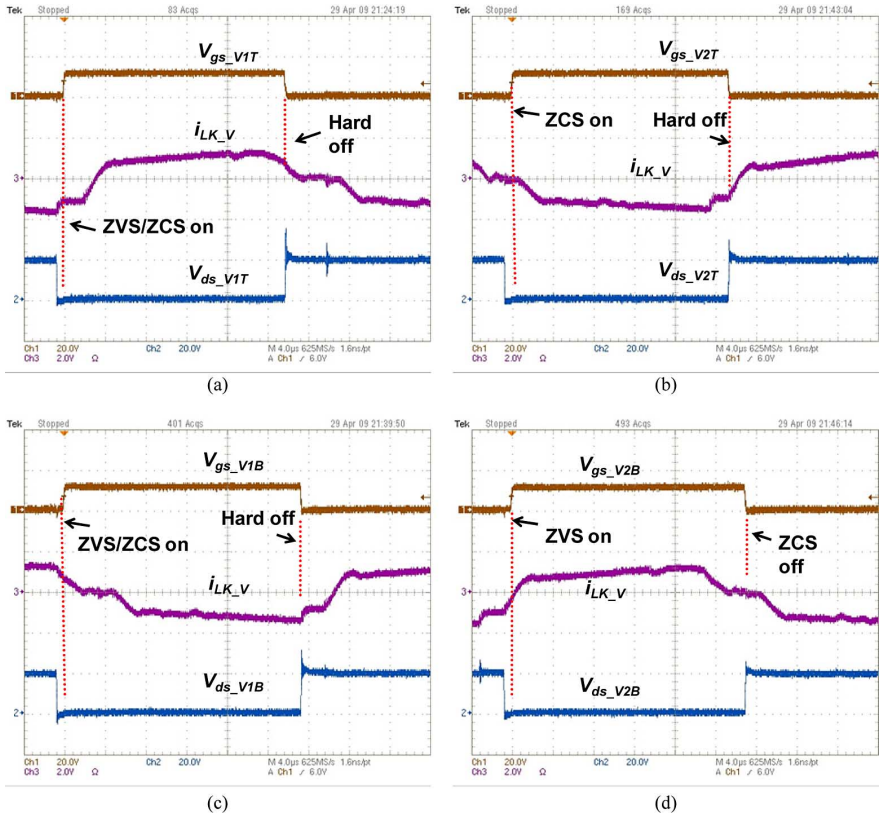

Fig. 11. Soft switching of the four devices on the phase V of Bridge I: (a) $V1T$, (b) $V2T$, (c) $V1B$, and (d) $V2B$ for CCM operation. Waveforms from top-to-bottom for each picture are: gate drive voltage (20 V/div.), transformer V secondary current (20 A/div.), and voltage across the associated device (20 V/div.).

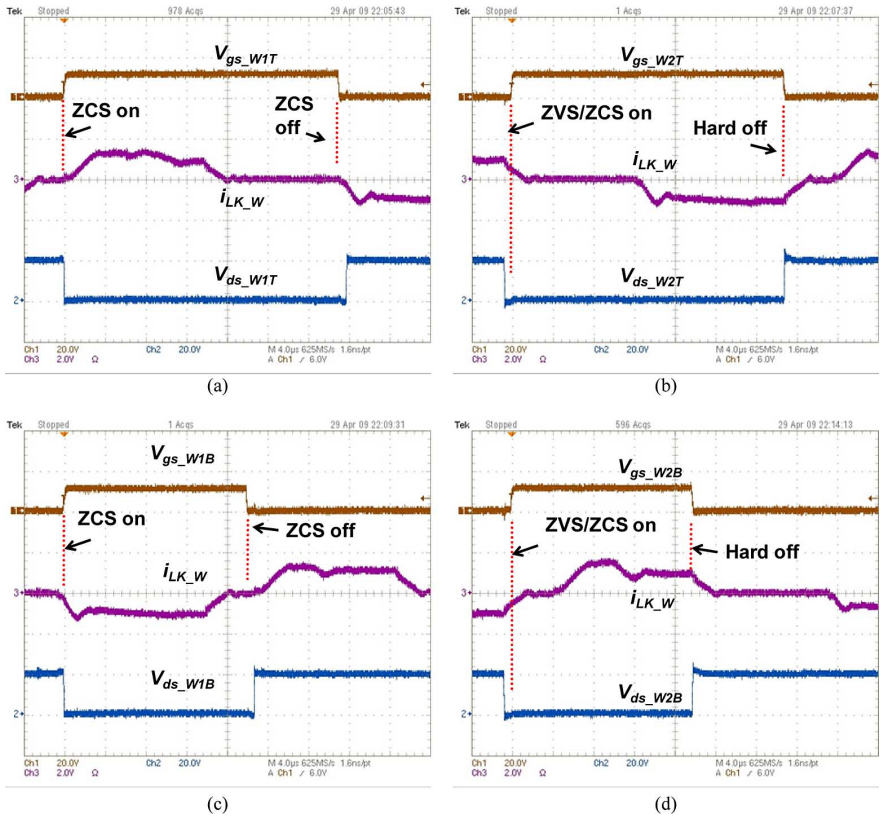

Fig. 12. Soft switching of the four devices on the phase W of Bridge I: (a) $W1T$, (b) $W2T$, (c) $W1B$, and (d) $W2B$ for CCM operation. Waveforms from top-to-bottom for each picture are: gate drive voltage (20 V/div), transformer W secondary current (20 A/div.), and voltage across the associated device (20 V/div.).

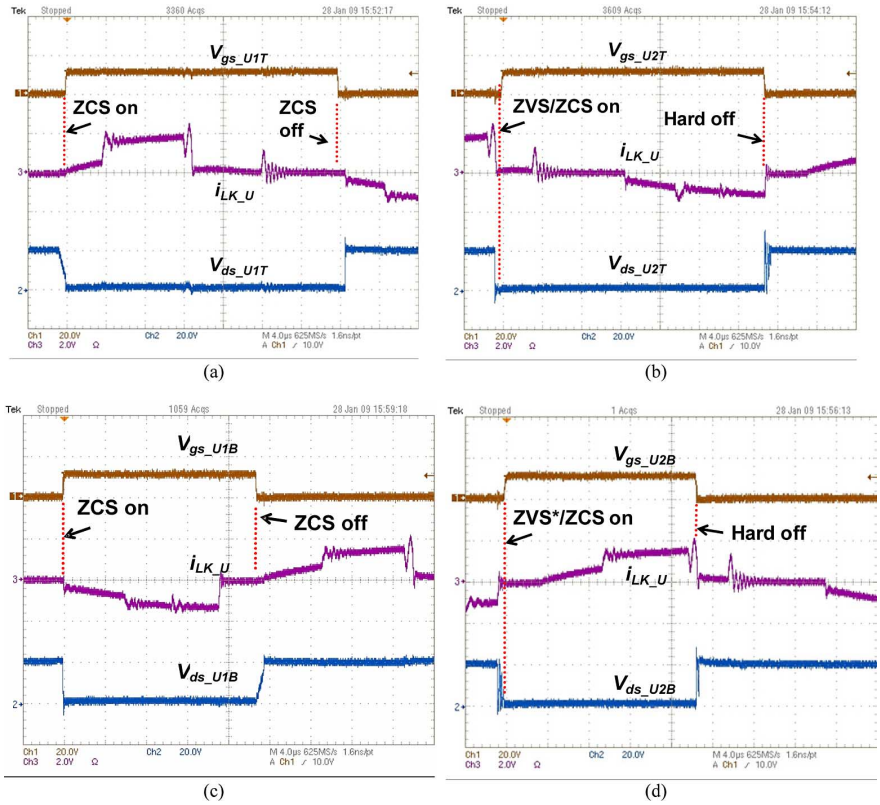

Fig. 13. Soft switching of the four devices on the phase *U* of Bridge I: (a) *U*1*T*, (b) *U*2*T*, (c) *U*1*B*, and (d) *U*2*B* for DCM operation. Waveforms from top-to-bottom for each picture are: gate drive voltage (20 V/div.), transformer *U* secondary current (20 A/div.), and voltage across the associated device (20 V/div.).

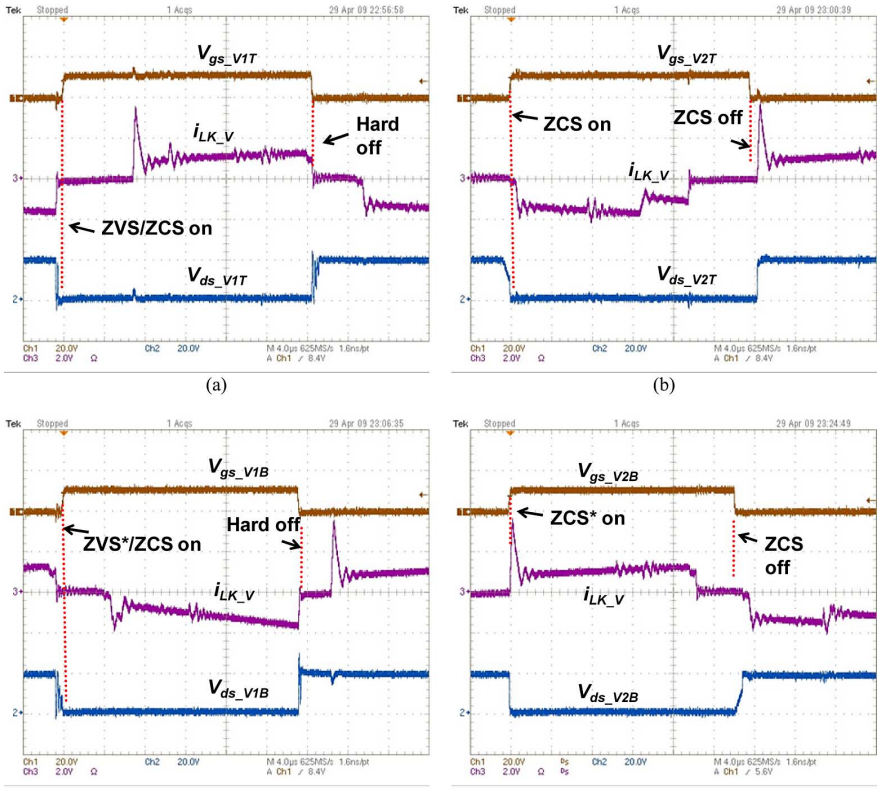

Fig. 14. Soft switching of the four devices on the phase *V* of Bridge I: (a) *V*1*T*, (b) *V*2*T*, (c) *V*1*B*, and (d) *V*2*B* for DCM operation. Waveforms from top-to-bottom for each picture are: gate drive voltage (20 V/div.), transformer V secondary current (20 A/div.), and voltage across the associated device (20 V/div.).

B. Verification of Frequency Reduction

Fig. 9(a) and (b) plots the output voltages generated by three full-bridges (V_U, V_V, and V_w) on Bridge I and Bridge II ($V_{\rm rec}$) for CCM and DCM operations, respectively. Because of the larger leakage inductances, the commutation time is longer for CCM as compared to DCM. This explains why the widths of "glitches" on $V_{\rm rec}$ are longer in Fig. 9(a) than that of in Fig. 9(b). Note from both graphs, the frequency of $V_{\rm rec}$ is the same as other three voltages, i.e., equals switching frequency.

C. Verification of Soft Switching for CCM Operation

Figs. 10–12 plot the turn-ON and turn-OFF intervals for each of the twelve switches on Bridge I when Bridge I is operating in CCM (external inductances are used). Results verify the soft-switching performance summarized in Table I. As shown in Fig. 10(a) and (c), switches *U*1*T* and *U*1*B* turn ON and turn OFF under ZCS, while Fig. 10(b) and (d) indicates that switches *U*2*T* and *U*2*B* turn ON under ZVS/ZCS since each turn-ON instant occurs when the associated transformer current is flowing through the antiparallel diode of the device. Finally, *U*2*T* and *U*2*B* turn OFF with hard-switching as shown in Fig. 10(b) and (d), respectively.

As shown in Fig. 11(a) and (c), switches *V*1*T* and *V*1*B* turn ON with ZVS/ZCS since the turn-ON occurs when the associated transformer current is flowing through the antiparallel diode of the device. Similarly, *V*2*B* turns ON with ZVS thanks to the sufficient leakage inductance. Fig. 11(b) indicates that switch *V*2*T* turns ON with ZCS. Among all four switches, only *V*2*B* turns OFF with ZCS, others turn OFF under hard-switching condition.

Fig. 12(a)–(d) shows that switches *W*2*T* and *W*2*B* turn ON with ZVS/ZCS. Switch *W*1*T* turns ON under ZCS. Switch *W*1*B* also turns ON under ZCS because the current rises at a very small rate limited by the large leakage inductances. As for the turn-OFF, *W*1*T* and *W*1*B* have ZCS OFF but *W*2*T* and *W*2*B* have hard turn-OFF.

D. Verification of Soft Switching for DCM Operation

Figs. 13–16 plot the turn-ON and turn-OFF intervals for each of 12 switches on Bridge I when Bridge I is operating in DCM. Results verify the soft-switching performance summarized in Table I.

The soft switch performance of devices on phase *U* in DCM is very close to the performance in CCM, except that the turn-ON of switch *U*2*B* is a conditional ZVS since the stored leakage energy may not be sufficient.

Comparison between Figs. 11 and 14 shows that the devices on phase *V* have very close soft switch performance for DCM operation as compared to CCM operation, with following two exceptions: 1) switch *V*2*B* turns ON under a nonstrict ZCS condition in DCM (shown in Figs. 14(d) and 15, respectively), while under a conditional ZVS condition in CCM [shown in Fig. 11(d)]; and 2) switch *V*2*T* turns OFF under a ZCS condition in DCM operation [shown in Fig. 14(b)], while it turns OFF under hard-switching condition in CCM operation [shown in Fig. 11(b)].

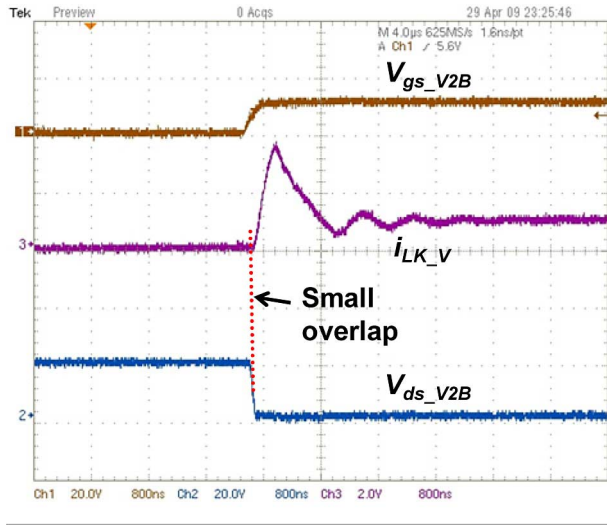

Fig. 15. Magnified view of Fig. 14(d) (800 ns/div.) showing the small overlap between the current and voltage during the turn-ON interval of *V*2*B*.

Similarly, the devices on phase *W* have very close soft switch performance between DCM and CCM operations. The only difference between Figs. 12 and 16 is the turn-ON of *W*1*B*. The current rising rate is higher when the converter is operating in DCM. Therefore, it is a nonstrict ZCS in DCM.

E. Efficiency Comparisons with Existing Schemes

Fig. 17 compares the measured overall efficiency of the prototype (inverter I633) under resistive loads operating with three different switching strategies: 1) the symmetrical duty-cycle-based phase-shift control with dc output as proposed in [2] is applied to Bridge I, and SPWM with 1/6 third harmonic injection [19] is used on Bridge III; 2) the symmetrical duty-cycle-based phase-shift control with twice-frequency pulsating-dc output, which was proposed in [11], is used on Bridge I, and hybrid modulation on Bridge III; and 3) the proposed soft-switching scheme with asymmetrical duty-cycle-based phase-shift control is used on Bridge I, and hybrid modulation on Bridge III. All test conditions are the same for these three strategies. No external inductor was used. As shown in Fig. 17, along with the hybrid modulation scheme on Bridge III, the proposed soft-switching scheme on Bridge I led to higher overall efficiency than the previous schemes. In addition to the soft switching, other two major factors contributing to the overall high efficiency are: 1) the usage of highly efficient power semiconductor devices such as very low on-resistance Si MOSFETs on Bridge I, SiC MOSFETs on Bridge III [20], and low forward-voltage drop SiC Schottky diodes on Bridge II; and 2) the usage of advanced core material for transformers [21], which improves transformer design with less core loss and less copper loss than the traditional ferrite core.

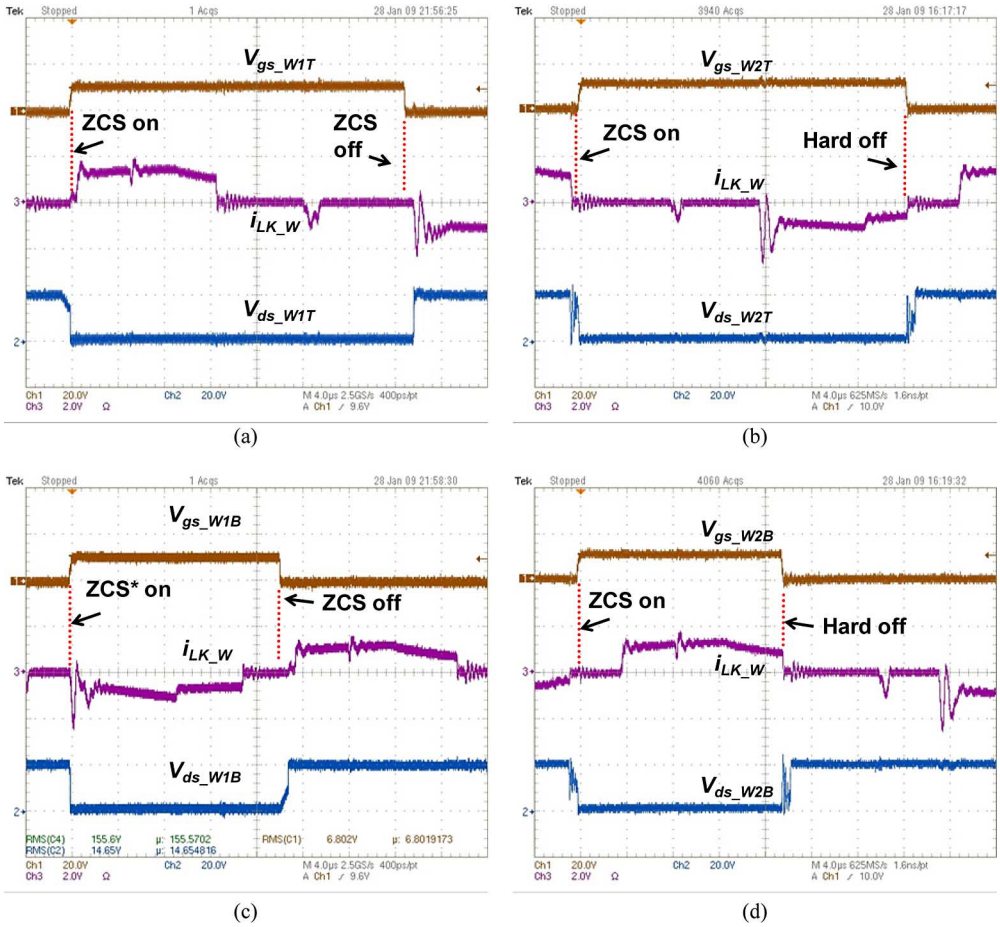

Fig. 16. Soft switching of the four devices on the phase W of Bridge I: (a) $W1T$, (b) $W2T$, (c) $W1B$, and (d) $W2B$ for DCM operation. Waveforms from top-to-bottom for each picture are: gate drive voltage (20 V/div.), transformer W secondary current (20 A/div.), and voltage across the associated device (20 V/div.).

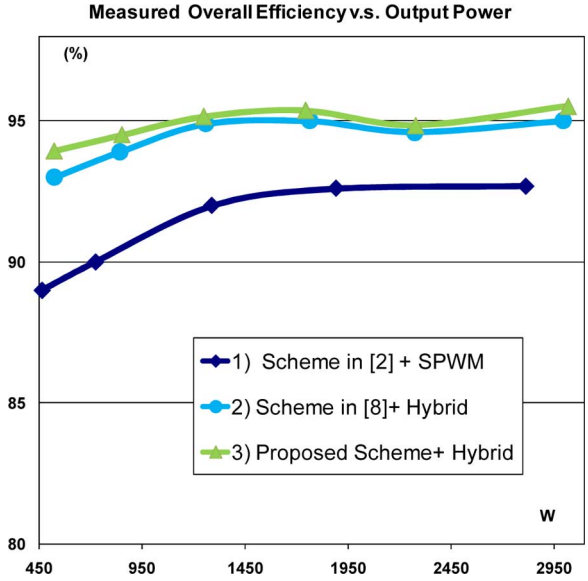

Fig. 17. Measured overall efficiency under resistive load versus output power for different switching strategies.

V. Conclusion

A soft-switching scheme is presented and verified in this paper for an isolated multiphase dc/pulsating-dc converter, which is the front-end stage of a three-phase RHFL. The proposed scheme reduces the frequency of the pulsating-dc output, which normally equals twice or higher of the switching frequency, thereby reducing the switching requirement (i.e., switching loss) for the back-end pulsating-dc/ac converter. Moreover, the proposed scheme achieves soft switching for the power switches on the front-end dc/pulsating-dc converter without adding auxiliary circuit. In conjunction with the hybrid modulation scheme on the back-end pulsating-dc/ac converter, this switching scheme leads to less overall switching loss than other existing schemes.

Acknowledgment

The hybrid modulation scheme for Bridge III in this paper is covered by S. K. Mazumder, "Hybrid modulation of multiphase converter", USPTO Patent Application DB054 filed by the University of Illinois, Chicago, in 2007. Any opinions, findings, conclusions, or recommendations expressed herein are those of the authors and do not necessarily reflect the views of the National Science Foundation.

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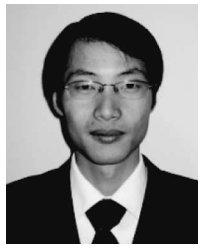

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