Wireless PWM Control of a Parallel DC–DC Buck Converter

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***Abstract*—We demonstrate a new concept for wireless pulse-width modulation (PWM) control of a parallel dc–dc buck converter. It eliminates the need for multiple physical connections of gating/PWM signals among the distributed converter modules. The new scheme relies on radio-frequency (RF) based communication of the PWM control signals from a master to the slave modules. We analyze the system stability and demonstrate the experimental effectiveness of the wireless control scheme for a two-module parallel buck converter for 10-kHz and 20-kHz switching frequencies and for channel lengths of 1.5 and 15 ft, respectively. The proposed control concept may lead to easier distributed control implementation of parallel dc–dc converters and distributed power systems, and may lead to redundancy that is achievable using droop method. It may also be used as a backup for wire-based control of parallel converters to provide fault tolerance.**

***Index Terms*—Buck converter, master–slave control, parallel dc–dc converters, radio frequency, wireless.**

I. Introduction

PARALLELING of dc–dc converters, such as the one illustrated in Fig. 1, yields many desirable features: enhanced reliability, increased power-output capability, expandability, reconfigurability and redundancy, and on-site repair when hot plug-in capability is incorporated [1]–[6]. One of the commonly used methods, for stabilization of parallel dc–dc converters, is the conventional droop method [3], [5], which is illustrated in Fig. 2(a). Droop method, which yields high system redundancy, can be accomplished with several classes of converters. The load sharing among the power supplies using this method is entirely dependent on the output voltage setting of each power converter. For this reason, it is not advisable to use the droop method to gain higher current than the maximum current capability of any single converter. It is possible, that one converter alone may drive the load and consequently, either go into overload protection or substantially reduce the lifetime of the converter. Besides, the output voltages in a droop method connection should be adjusted as closely as possible.

To minimize the negative effects of conventional droop and for increased reliability, paralleled dc–dc converters require an active-current-sharing mechanism to ensure even distribution of currents and stresses between the modules. The latter is the same as droop method with the addition of a current-sharing bus, as shown in Fig. 2(b). The essence of current sharing is to monitor

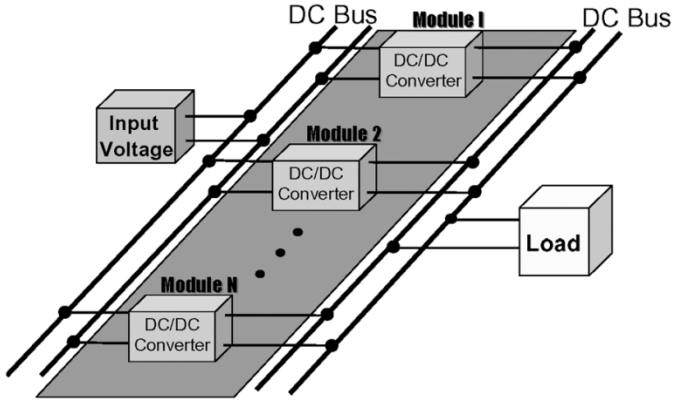

Fig. 1. Parallel dc–dc converter.

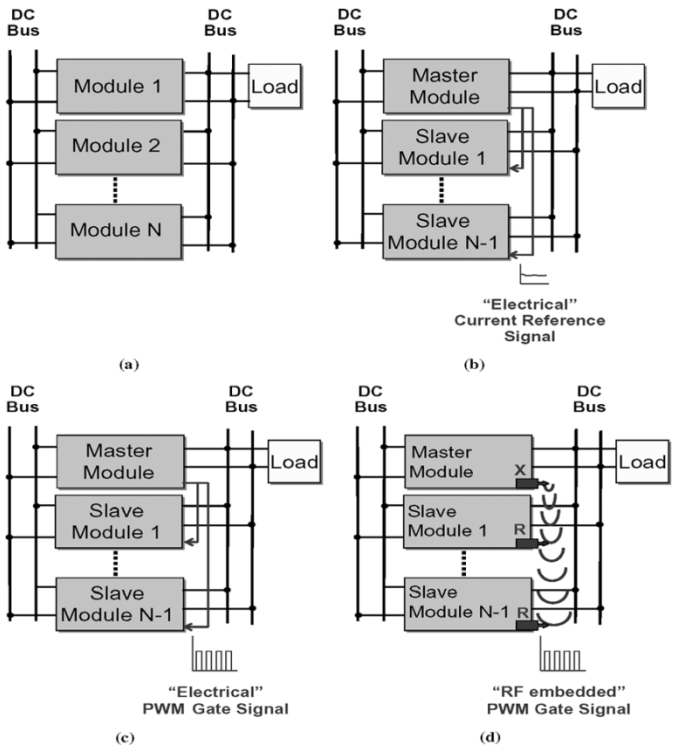

Fig. 2. (a) Droop method, (b) dedicated master–slave current-sharing method, (c) and (d) dedicated master–slave method for distributing the PWM gate signal of the master module among N-1 slave modules electrically and wirelessly, respectively. For (d), the symbols X and R represent the radio-frequency (RF) transmitter and receiver, respectively.

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the difference between the reference current and the output current of each converter and incorporate this information into the control loop. Many effective current-sharing control schemes have been proposed in previous studies, including [1], [4]–[7]. One common current-sharing approach is to employ an active control scheme to force the currents in all but one module of a parallel dc–dc converter to follow the reference current generated by a dedicated module referred to as the master. Such a scheme, also known as dedicated master–slave control scheme [5], [8], ensures that all of the slave modules follow the reference current of the master.

For very low-cost power-electronics applications, an inexpensive version of the master–slave control technique, as shown in Fig. 2(c), is used [9]. In such a scheme, the master module echoes the gating pulse-width modulation (PWM) signals to all other slave modules. With such an implementation, if any slave module were to fail, the overall power system can still be operational. Thus, a certain degree of redundancy is obtained by adopting this configuration. The extension of the low-cost scheme shown in Fig. 2(c), which has so far been primarily limited to single-board applications, to parallel dc–dc converters that are distributed in space has been difficult due to increased multiplicity of physical connections for PWM gate signals.

To avoid this problem, we propose in Fig. 2(d), a new concept, which eliminates the need for multiple physical connections of clock/control signals among the distributed modules. The new control scheme has potential applications for spatially distributed higher power interactive power-electronic networks (IPNs) including naval IPN, microgrids, more electric aircrafts (MEAs), and distributed uniterruptible power supplies (UPSs) [10]–[12]. As shown in Fig. 2(d), the new scheme relies on wireless communication of the PWM gate control signals from the master to the slave modules. In this paper, we demonstrate the distributed wireless PWM control scheme for a parallel dc–dc converter system, comprising two modules. We demonstrate the effectiveness of the wireless control scheme for two different switching frequencies and for module-separation distances as close as 1.5 ft and as far as 15 ft. It is apparent from Fig. 2(a) and (d) that, the wireless master–slave method, achieves a level of redundancy that is very close to that achievable using the droop method. However, unlike the droop method, the proposed method achieves an improved regulation.

II. Control Scheme and Stability Analysis

Fig. 3(a), shows the wireless master–slave PWM control scheme for a parallel dc–dc buck converter comprising two modules—a master and a slave. The master module implements a voltage-mode control to regulate the output voltage. The structure of the compensator is described by the transfer function $H_v(s) = (K/s)((s/\omega_z)+1)/((s/\omega_p)+1)$ [13], where K is the dc gain, ω_z and ω_p are the zero and pole, respectively. The objective of the voltage-mode controller for the master is to regulate the output voltage. This is achieved by comparing the voltage feedback of the output voltage with the reference $(V_{\mathrm{dc\_ref}})$ for the same. The output of the controller, which is an error signal, is compared with a ramp signal, which determines the switching frequency of the converter. The output

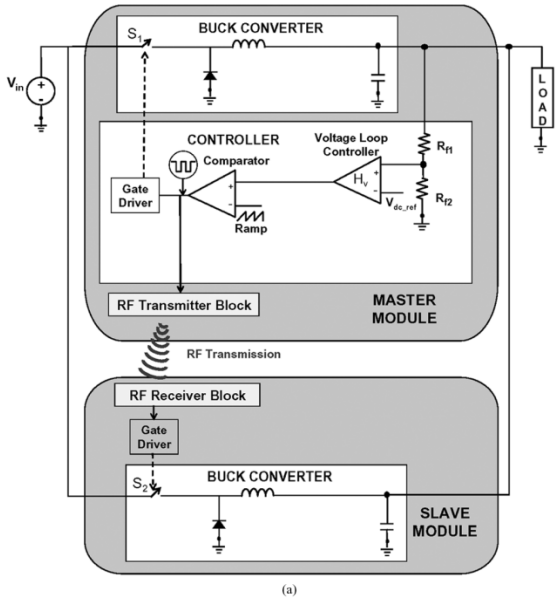

Fig. 3. (a) Control scheme for the experimental parallel dc–dc converter and (b) the experimental setup of the master–slave converter. The distance between the two antennas is 1.5 ft, which is later extended to 15 ft.

of the comparator is the PWM signal, which (after passing it through a gate driver) is used to control the power MOSFET (S_1) of the master buck converter. The same PWM signal is sent wirelessly to the slave module. To achieve this, first the PWM signal is fed to a radio-frequency (RF) transmitter on the master module. The RF transmitter, without digitizing the signal, amplifies and broadcasts it using a 900-MHz[1] carrier and hence, the duty cycle does not change in finite increments. The frequency shift keying (FSK) modulation scheme is used by the RF transmitter. In this modulation, 900-MHz RF signal switches between two frequencies depending on the ON or OFF state of the PWM signal. During the ON duration of the PWM signal one particular frequency is transmitted by the RF transmitter and a second frequency is transmitted for the OFF duration of the PWM signal. This way the PWM signal and the duty ratio are preserved during the transmission. Subsequently, the modulated RF signal is captured by the receiver of the slave module, which is tuned to 900 MHz as well. The

[1]The RF transmitter and receiver used in the experimental setup use 900-MHz frequencies and operate in the unlicensed industrial, scientific, and medical (ISM) band.

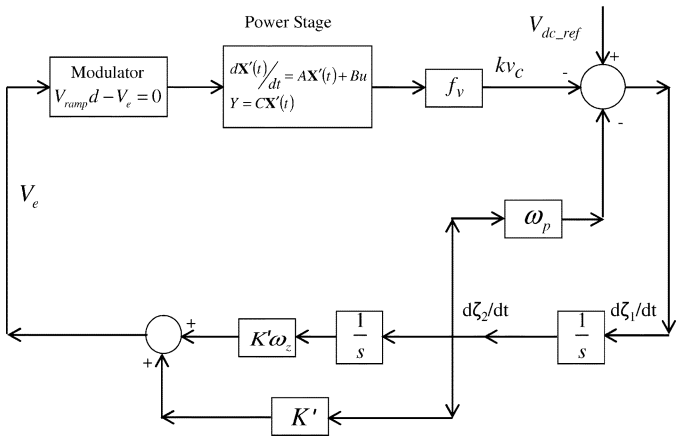

Fig. 4. Equivalent block diagram for the parallel converter with controller only on the master module.

receiver demodulates and amplifies the broadcast signal such that the output of the receiver matches the pattern of the original PWM signal. This signal is then fed to the input of the slave power-MOSFET gate driver, the output of which controls the MOSFET (S_2) and thus, ensures equal power sharing between the master and the slave modules. The bandwidth (BW) of RF transmitter and receiver pair used is 200 Hz–28 kHz and any switching signal within this range can be transmitted using this pair. The BW requirement for the RF transmission increases with the increase in the switching frequency. This requirement can be accomplished by using modules with larger transmission BW, e.g., AR5414 from Atheros. The experimental master–slave modules comprising the buck converter and wireless transmitter and receiver are shown in Fig. 3(b).

The equivalent model of the parallel master–slave system with voltage controller on the master module while the slave module follows the master PWM signal is shown in Fig. 4.

The state space equation for the master–slave power stage is given by

$$\begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r_{L1}}{L_1} & 0 & \frac{-1}{L_1} \\ 0 & \frac{-r_{L2}}{L_1} & \frac{-1}{L_2} \\ \frac{1}{(C_1+C_2)} & \frac{1}{(C_1+C_2)} & \frac{-1}{R(C_1+C_2)} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{S_1}{L_1} \\ \frac{S_2}{L_2} \\ 0 \end{bmatrix} V_{\text{in}}. \quad (1a)$$

The state space equivalent of the controller transfer function is

$$\begin{bmatrix} \frac{d\zeta_1}{dt} \\ \frac{d\zeta_2}{dt} \end{bmatrix} = \begin{bmatrix} -\omega_p & 0 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \zeta_1 \\ \zeta_2 \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} [V_{\text{dc\_ref}} - kv_c]$$
$$V_e = [K' \;\; K'\omega_z] \begin{bmatrix} \zeta_1 \\ \zeta_2 \end{bmatrix} \quad (1b)$$

where $K' = K(\omega_p/\omega_z)$. Combining (1a) with (1b) the state space realization of the overall system is given by

$$\dot{X} = AX + BV_{\text{in}} + B_{\text{rc}}V_{\text{dc\_ref}}$$
$$V_e = CX \quad (1c)$$

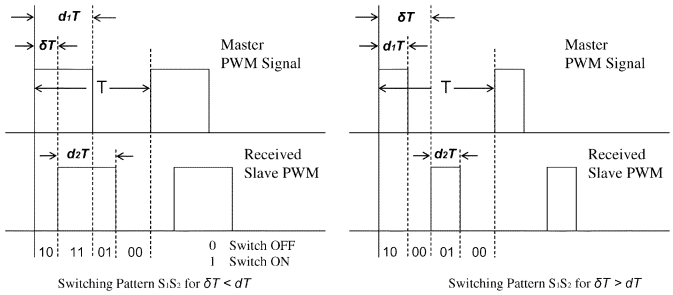

Fig. 5. PWM signal of the master module and the delayed version on the slave module. Simultaneous representation of these two signals determines the switching pattern S_1S_2. Since the slave module follows the signal from the master module the duty ratio (d) is same on both modules ($d_1 = d_2 = d$).

where

$$A = \begin{bmatrix} \frac{-r_{L_1}}{L_1} & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & \frac{-r_{L_2}}{L_1} & \frac{-1}{L_2} & 0 & 0 \\ \frac{1}{(C_1+C_2)} & \frac{1}{(C_1+C_2)} & \frac{-1}{R(C_1+C_2)} & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & -k & 0 & -\omega_p \end{bmatrix}$$

$$B = \begin{cases} B_1 = [1/L_1 \;\; 0 \;\; 0 \;\; 0 \;\; 0]^T, & \text{for } S_1S_2 = 10 \\ B_2 = [1/L_1 \;\; 1/L_2 \;\; 0 \;\; 0 \;\; 0]^T, & \text{for } S_1S_2 = 11 \\ B_3 = [0 \;\; 1/L_2 \;\; 0 \;\; 0 \;\; 0]^T, & \text{for } S_1S_2 = 01 \\ B_4 = [0 \;\; 0 \;\; 0 \;\; 0 \;\; 0]^T, & \text{for } S_1S_2 = 00 \end{cases}$$

$$B_{\text{rc}} = [0 \;\; 0 \;\; 0 \;\; 0 \;\; 1]^T$$

and

$$C = [0 \;\; 0 \;\; 0 \;\; K'\omega_z \;\; K'].$$

The state vector $X = [i_1 \;\; i_2 \;\; v_c \;\; \xi_2 \;\; \xi_1]^T$ combines the states of the voltage mode controller on master module and the states of master–slave power stages. When the signal is transmitted from the master module wirelessly it experiences a delay (δT) before activating the switch on the slave module. The switching patterns of the two switches in one switching cycle are shown in Fig. 5. Below we obtain the steady state solution for the case when $\delta T < dT$ A similar derivation can be done for the case when $\delta T > dT$. For the interval $0 \le t \le \delta T$ the switching state S_1S_2 is 10 and the system state equation is given by

$$X_{kT+\delta T} = e^{A\delta T}X_{\text{kT}} + [e^{A\delta T} - I]A^{-1}B_1V_{\text{in}} + [e^{A\delta T} - I]A^{-1}B_{\text{rc}}V_{\text{dc\_ref}} \quad (2a)$$

where X_{kT} is the value of X at the end of the kth switching cycle. Similarly, the state equations for switching states 11, 01, 00, respectively, are

$$X_{kT+dT} = e^{A(d-\delta)T}X_{kT+\delta T} + \left[e^{A(d-\delta)T} - I\right]A^{-1}B_2V_{\text{in}} + \left[e^{A(d-\delta)T} - I\right]A^{-1}B_{\text{rc}}V_{\text{dc\_ref}} \quad (2b)$$

$$X_{kT+(\delta+d)T} = e^{A\delta T}X_{kT+dT} + [e^{A\delta T} - I]A^{-1}B_3V_{\text{in}} + \left[e^{A\delta T} - I\right]A^{-1}B_{\text{rc}}V_{\text{dc\_ref}} \quad (2c)$$

$$X_{kT+T} = e^{A(1-d-\delta)T}X_{kT+(d+\delta)T} + \left[e^{A(1-d-\delta)T} - I\right]A^{-1}B_4V_{\text{in}} + \left[e^{A(1-d-\delta)T} - I\right]A^{-1}B_{\text{rc}}V_{\text{dc\_ref}}. \quad (2d)$$

Combining the state (2a)–(2d) over one switching cycle we obtain

$$\begin{aligned} &X_{kT+T} \\ &\quad = f(X_{kT}, d, V\text{in}, \delta) \\ &\quad = e^{AT}X_{kT} + \begin{pmatrix} \left[e^{AT} - e^{A(1-\delta)T}\right]A^{-1}B_1 \\ + \left[e^{A(1-\delta)T} - e^{A(1-d)T}\right]A^{-1}B_2 \\ + \left[e^{A(1-d)T} - e^{A(1-d-\delta)T}\right]A^{-1}B_3 \\ + \left[e^{A(1-d-\delta)T} - I\right]A^{-1}B_4 \end{pmatrix} V_{\text{in}} \\ &\qquad + [e^{AT} - I]A^{-1}B_{\text{rc}}V_{\text{dc\_ref}} \end{aligned} \tag{3}$$

and the auxiliary equation for the switching condition of the closed loop feedback system is

$$\begin{aligned} &\eta(X_{kT}, d, V\text{in}, \delta) \\ &\quad = C\left(e^{AdT}X_{kT} + \begin{Bmatrix} \left[e^{AdT} - e^{A(d-\delta)T}\right]A^{-1}B_1 \\ + \left[e^{A(d-\delta)T} - I\right]A^{-1}B_2 \end{Bmatrix} V_{\text{in}}\right. \\ &\qquad \left. + [e^{AdT} - I]A^{-1}B_{\text{rc}}V_{\text{dc\_ref}}\right) - V_{\text{ramp}}d = 0. \end{aligned} \tag{4}$$

We obtain the equilibrium solution ($X_{kT+T} = X_{kT} = X$) for the system as

$$\begin{aligned} X = &\left[I - e^{AT}\right]^{-1} \\ &\times \left\{ \begin{pmatrix} \left[e^{AT} - e^{A(1-\delta)T}\right]A^{-1}B_1 \\ + \left[e^{A(1-\delta)T} - e^{A(1-d)T}\right]A^{-1}B_2 \\ + \left[e^{A(1-d)T} - e^{A(1-d-\delta)T}\right]A^{-1}B_3 \\ + \left[e^{A(1-d-\delta)T} - I\right]A^{-1}B_4 \end{pmatrix} V_{\text{in}} \right. \\ &\left. + [e^{AT} - I]A^{-1}B_{\text{rc}}V_{\text{dc\_ref}} \right\}. \end{aligned} \tag{5}$$

Solving (4) for duty ratio d and substituting in (5) we get equilibrium point solution for the states of the system. Now for small disturbances in the states, the duty ratio, the delay, and the input voltage we obtain

$$\begin{aligned} x = X + \tilde{x}, \quad d = D + \tilde{d}, \quad \delta = \Delta + \tilde{\delta}, \\ v_{\text{in}} = V_{\text{in}} + \tilde{v}_{\text{in}}, \quad y = Y + \tilde{y} \end{aligned} \tag{6}$$

and using (6) we linearize the system about the equilibrium point to obtain

$$x_{(k+1)T} \approx \frac{\partial f}{\partial x}\tilde{x}_{kT} + \frac{\partial f}{\partial d}\tilde{d} + \frac{\partial f}{\partial v_{\text{in}}}\tilde{v}_{\text{in}} + \frac{\partial f}{\partial \delta}\tilde{\delta} \tag{7}$$

$$0 \approx \frac{\partial \eta}{\partial x}\tilde{x}_{kT} + \frac{\partial \eta}{\partial d}\tilde{d} + \frac{\partial \eta}{\partial v_{\text{in}}}\tilde{v}_{\text{in}} + \frac{\partial \eta}{\partial \delta}\tilde{\delta}. \tag{8}$$

It follows from (8) that

$$\tilde{d} = -\left[\frac{\partial \eta}{\partial d}\right]^{-1}\left[\frac{\partial \eta}{\partial x}\tilde{x}_{kT} + \frac{\partial \eta}{\partial v_{\text{in}}}\tilde{v}_{\text{in}} + \frac{\partial \eta}{\partial \delta}\tilde{\delta}\right]. \tag{9}$$

Using the result from (9) and substituting it in (7) we obtain

$$x_{(k+1)T} \approx \tilde{A}\tilde{x}_{kT} + \tilde{B}\tilde{v}_{\text{in}} + \tilde{C}\tilde{\delta}$$

where

$$\tilde{A} = \frac{\partial f}{\partial x} - \frac{\partial f}{\partial d}\left[\frac{\partial \eta}{\partial d}\right]^{-1}\frac{\partial \eta}{\partial x},$$

$$\tilde{B} = \frac{\partial f}{\partial v_{\text{in}}} - \frac{\partial f}{\partial d}\left[\frac{\partial \eta}{\partial d}\right]^{-1}\frac{\partial \eta}{\partial v_{\text{in}}}$$

$$\tilde{C} = \frac{\partial f}{\partial \delta} - \frac{\partial f}{\partial d}\left[\frac{\partial \eta}{\partial d}\right]^{-1}\frac{\partial \eta}{\partial \delta}.$$

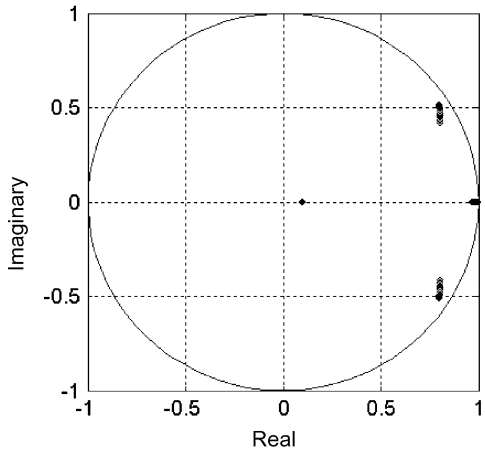

Fig. 6. Eigenvalues for input voltage (V_{in}) variation from 10 V to 40 V at $dT = (1/2)T$.

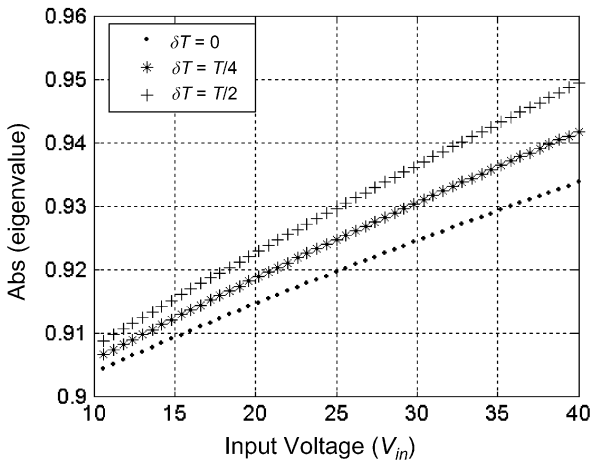

Fig. 7. Effect of input voltage variation on the eigenvalues for different delay variations.

The stability of a given point can be determined by the eigenvalues (Floquet multipliers) of $\tilde{A}$ [14]. For the asymptotic stability all the eigenvalues must lie within the unit circle.

III. Results

We have conducted simulations to analyze the system stability. Fig. 6 shows the plot for eigenvalues for an input voltage variation of 10 to 40 V at a delay $\delta T = T/2$. All the eigenvalues fall within the unit circle and the system remains stable for this delay. In Fig. 7 the effect of the input voltage variation for delay $\delta T = 0, \delta T = (1/4)T$, and $\delta T = (1/2)T$ is shown only for the complex pair of eigenvalues. From the plot it can be seen that the absolute value of the complex conjugate pair of eigenvalues increases with the increase in the delay. But this increase in the absolute value is very small and there is only marginal effect on the system stability.

The power-stage, control, and wireless parameters of the experimental parallel converter, shown in Fig. 3(b), are tabulated in Table I. Using the experimental modules, we conduct three

[2]Ch2 displays the current in "A" while Ch3 displays in "mV" as Ch3 was using a current probe amplifier. The setting for current probe amplifier was "10 mV = 2 A."

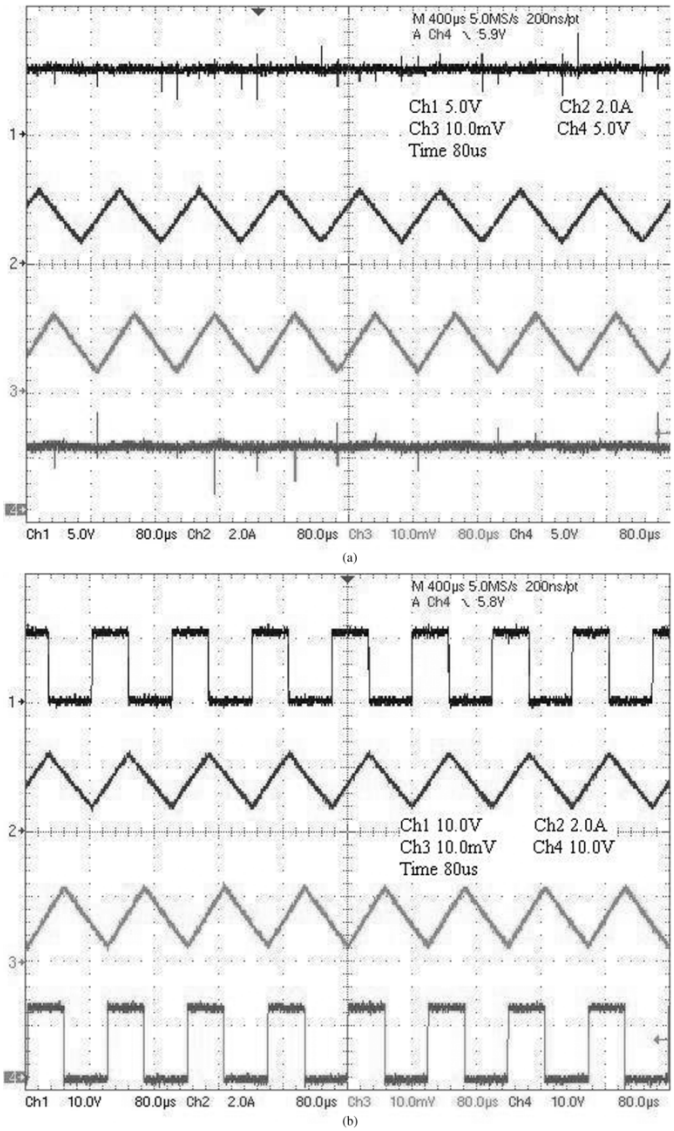

Fig. 8. Results for master and slave at a distance of 1.5 ft and at a switching frequency of 10 kHz. (a) Master and slave output voltages (Ch1 and Ch4) and inductor currents (Ch2 and Ch3)[2], respectively. (b) Master and slave PWM signals (Ch1 and Ch4) and inductor currents (Ch2 and Ch3), respectively. The delay between the master and slave waveforms is the sum of the modulation and demodulation delays introduced by the wireless transmitter and receiver respectively and is independent of the PWM signal frequency.

separate tests. First, we obtain the performance of the parallel dc–dc converter by keeping the switching frequency at 10 kHz and the distance between the master and slave modules at 1.5 ft. Fig. 8(a) and (b), demonstrate the effectiveness of the wireless PWM control scheme. They show that the inductor current and gate signals of the slave module follow the same signals of the master module using a small time delay. The delay is due to the RF transmission. However, the mean values of the master and slave inductor currents are the same and so are their output voltages. This establishes even distribution of the load-sharing current.

The delay between the master and slave modules depends mainly on processing time of the RF transmitter and receiver and is almost constant. With the increase in switching frequency the phase lag between the master and the slave modules also increases as explained below. Let δT is the signal time delay from the master module to the slave module and f_s is the switching frequency then the phase lag between the two modules is given by $\Delta\phi = f_s \times \delta T$. Since δT is constant so the phase-lag is a function of the switching frequency. For the RF transmitter and receiver pair used in the setup $\delta T = 20\ \mu$s.

TABLE I
PARAMETERS OF THE MASTER–SLAVE PARALLEL BUCK CONVERTER SYSTEM

Nominal Parameters	Values
Switching frequencies	10 kHz and 20 kHz
Minimum and maximum channel lengths (attempted)	1.5 feet and 15 feet
Bandwidth of the wireless transmitter and receiver	28 kHz
Maximum baud rate of the wireless transmitter	56 kbps
Input voltage	10V
Output load current	2.9A
Output inductance of the master	165 µH
Output inductance of the slave	150 µH
Output capacitance	600 µF
Reference output voltage for the master	2.5 V
Ramp height	8 V
Regulated output voltage	5 V
DC gain (K) of the master voltage-mode controller	3000
Zero (w_{z1}) of the master voltage-mode controller	700 rad/s
Pole (w_{p1}) of the master voltage-mode controller	22,000 rad/s
Logic power supply for the master and slave boards	±15 Vand 5 V

By comparing Figs. 8 and 9, it is obvious that, the increased channel length does not have any appreciable impact on the performance of the parallel dc–dc converter. This is due to the negligible delay introduced by the channel, when the RF signal propagates from transmitting antenna to receiving antenna, as compared to the delay introduced by the transmitter and receiver itself in the process of modulation and demodulation.

Next, we investigate the effect of increasing the switching frequency on the performance of the master–slave module. We fix the switching frequency at 20 kHz, fixing the distance between the master and slave modules at 1.5 ft. The results for this case are shown in Fig. 10. It shows that, the performance of the parallel dc–dc converter is similar to that shown in Fig. 8. The load sharing between the two modules is even; however, the current ripple is smaller because of a twofold increase in the switching frequency. The primary difference between the results of Figs. 8 and 10 is the additional phase lag (the actual time delay remains the same though) between the master and slave responses when the modules are operated at 20 kHz. The additional phase lag between the master and the slave modules for the 20 kHz case is due to the smaller switching period as explained earlier. The delay introduced by the RF transmission leads to interleaving between the master and slave modules for a two module system. But for multiple slave modules, since the same PWM signal from the master module with constant delay will be received by all slave modules, interleaving will not be possible.

Finally, our experiments at 10 kHz as well as 20 kHz and channel lengths of 1.5 and 15 ft, respectively, did not reveal any effect of switching noise on RF transmission. This is because the magnitude of the switching noise signals (generated by the converters) is significantly weaker as compared to the RF signals. This outcome matches the results of [15], which show that the effect of electro-magnetic interference (EMI) due to switching

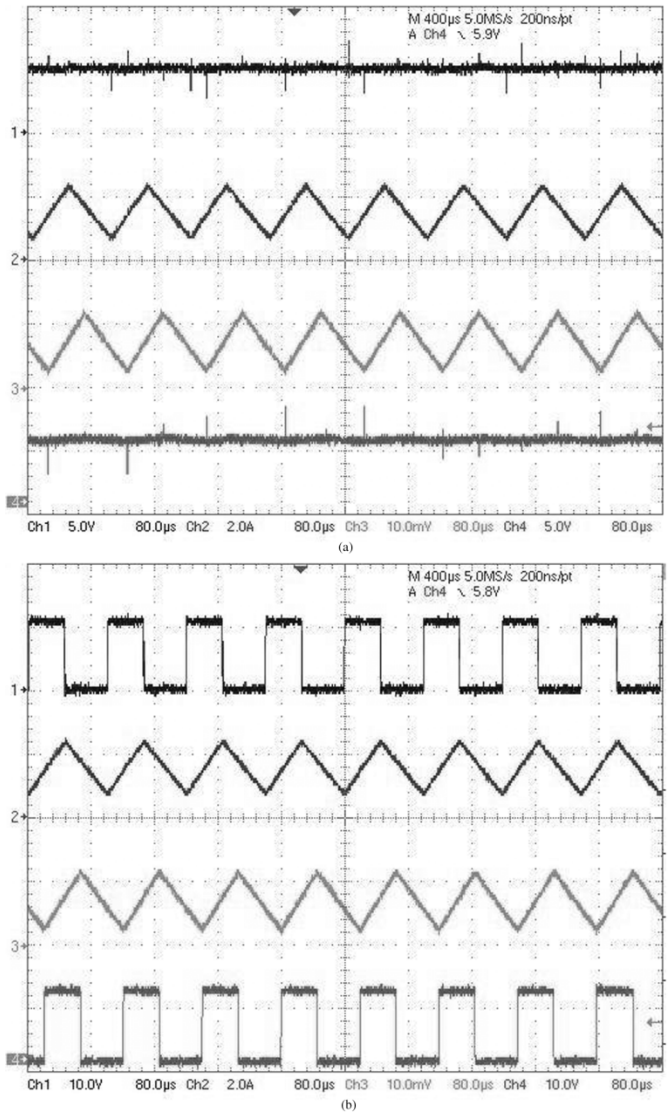

Fig. 9. Results for master and slave at a distance of 15 ft and at a switching frequency of 10 kHz. (a) Master and slave output voltages (Ch1 and Ch4) and inductor currents (Ch2 and Ch3), respectively. (b) Master and slave PWM signals (Ch1 and Ch4) and inductor currents (Ch2 and Ch3), respectively. The delay between the master and slave waveforms is the sum of the modulation and demodulation delays introduced by the wireless transmitter and receiver respectively. However, the increase in the channel length from 1.5 to 15 ft does not have any appreciable impact on the performance of the parallel dc–dc converter.

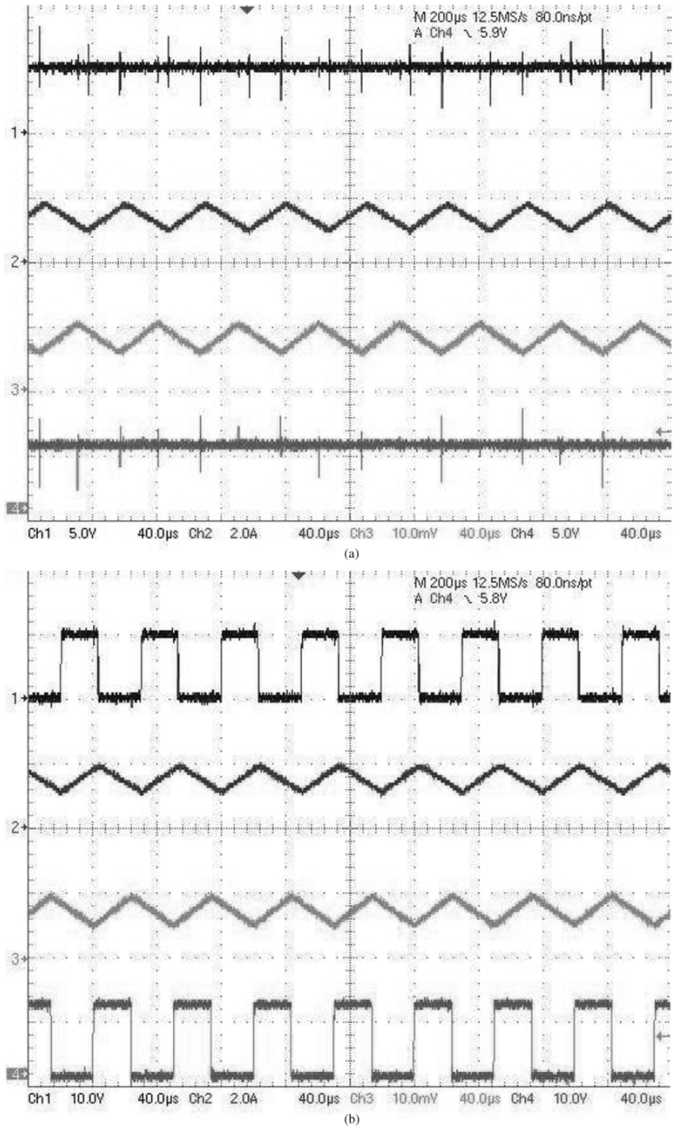

Fig. 10. Results for master and slave at a distance of 1.5 ft and at a switching frequency of 20 kHz. (a) Master and slave output voltages (Ch1 and Ch4) and inductor currents (Ch2 and Ch3), respectively. (b) Master and slave PWM signals (Ch1 and Ch4) and inductor currents (Ch2 and Ch3), respectively. The delay between the master and slave waveforms is the sum of the modulation and demodulation delays introduced by the wireless transmitter and receiver respectively. Although the actual time delay for 10 and 20 kHz operating frequencies remains similar, the phase lag between the master and the slave modules for the 20 kHz case is larger ($\approx$40% of the time period of the PWM signal in contrast to 20% in case of 10 kHz PWM) because of smaller switching period.

reduces with the increase in the frequency because the switching noise signal decays rapidly at higher frequencies. For instance, using the noise-frequency plot of [15] for a frequency below 80 MHz, we determine that the noise signal strength is a negligible -60 dB when a switching system operates at 10 kHz PWM with line voltage of 300 V and a current of 100 A. Needless to say, these voltage and current ratings are significantly higher than that of our experimental prototype.

IV. Conclusion

We demonstrate the effectiveness of a wireless pulse-width modulation (PWM) control scheme for a two-module parallel dc–dc buck converter. One of the parallel modules is assigned as the master while the other as the slave. The master module regulates the output voltage using a voltage-mode control scheme; that is, by comparing a reference voltage with the feedback output voltage and then, generating an appropriate PWM signal (by comparing the error signal with a ramp carrier signal), which modulates the power MOSFET of the buck converter. The PWM signal generated by the master module is then wirelessly transmitted to the slave module, thereby ensuring equal sharing of the load current between the two parallel modules. We tested the master–slave wireless converter system under three conditions: at switching frequency of 10 kHz and with channel lengths of 1.5 and 15 ft, respectively, and at switching frequency of 20 kHz

for a channel length of 1.5 ft. The averaged load current sharing for all the three cases was even. A delay was observed between the master and slave responses, which is attributed to the processing limitation of the wireless transmitter and receiver modules. The effect of this delay on the stability of parallel converter system is studied. From the analysis it is clear that the effect of the delay on the system stability is marginal for delays bounded by half switching cycle.

Although this delay is fixed, it translates to a greater phase shift between the master and slave inductor currents at 20 kHz than that at 10 kHz because of the smaller time period of the former. Finally, we observed that, for the wireless transmitter, which has a range of 90 feet, increase in the channel length from 1.5 ft to 15 ft has no appreciable effect at 10 kHz. The new concept for controlling a parallel dc–dc converter, proposed in this paper, eliminates the need for multiple wire connections of PWM/gate signals among the distributed modules and has applicability for multiple parallel converter topologies. We have extended this concept to dc–ac converters and have applied it to a two-module parallel voltage source inverter (VSI) [12].

The choice of the RF transmitter and receiver pair is dictated by, the switching frequency of the system, number of parallel modules, selection between bandwidth and cost and the spatial distribution of the modules. Also at very high switching frequencies the delay introduced by the RF transmitter and receiver becomes significant and this issue should be addressed in designing the RF interface. One solution can be an ASIC integrating both the control and RF interface on the same chip and hence reducing the delay due to processing on the transmitter and receiver modules.

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