Sequential Co-transmission of High-Frequency Power and Data Signals

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***Abstract*—An approach for *sequential* transmission of high-frequency (HF) power and data signals over a common HF channel (i.e., co-transmission) is outlined. This is in contrast to the conventional power-line communication, where the power and data co-transmission is *simultaneous*. Sequential co-transmission avoids data corruption by temporally distributing power and data signals over an HF channel and limiting their overlap. A data-transfer mechanism to realize the sequential co-transmission approach is outlined. Simple transmitter and receiver circuits, synthesized without the use of any analog-filtering circuitry are designed and a modified asynchronous serial-communication-interface protocol is implemented for ensuring the integrity of the transmitted data. The sequential HF power and data co-transmissions are experimentally validated using a closed-loop distributed dc/dc converter operating in switching frequency range of 100 kHz.**

I. Introduction

ADDING a communication link for information exchange (for monitoring load, fault, system and maintenance status, control parameters, etc.) to an existing power system with limited overhead cost has always been of perpetual interest [1]–[4]. Conventionally, power-line communication (PLC), which is typically used for smart metering [1] and system monitoring applications [3], is realized by superimposing high-frequency (HF) data signal over a 60/50-Hz low-frequency (LF) power signal [5], as illustrated in Fig. 1(a). Owing to the wide separation between the frequency spectrums of these two signals (LF power signal and HF data signal), simple but large reactive couplers along with line traps and low-order analog-filtering circuits are needed for such a PLC to couple and extract data to and from the power line. Further, in [6]–[12], a new form of PLC for motor-drive applications, with simultaneous transmission of HF data signal over an HF power signal is illustrated for transmitting information over an HF PWM link. However, such a PLC yields temporal overlap between the HF power and HF data signals, which following Shannon's theorem [13], reduces the channel capacity for data transmission because of background noise generated by the average current flowing through the network. This results in an increased probability of data failure at higher noise levels. For instance, in [6], up to a 90% reduction in data rate is reported as the amplitude of the PWM signal is enhanced; further, for a PWM frequency exceeding 10 kHz, all data signals are lost. Additional, in [7] for a system working at 12 kHz, a complete loss of communication is reported at the PWM switching instants.

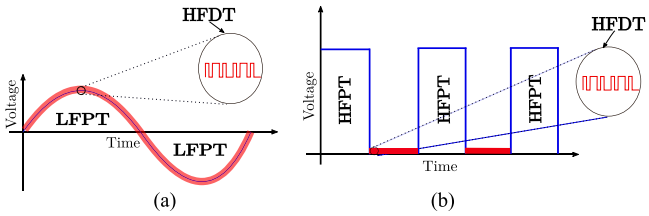

Fig. 1. Illustrations for (a) conventional PLC with simultaneous LF power and HF data transmissions (LFPT, HFDT), and (b) *sequential* HFPT and HFDT.

In view of these limitations of *simultaneous* PLCs, Fig. 1(b) outlines a scheme for *sequential* co-transmission of HF power and HF data signals. In this scheme, power and data networks are linked over the HF channel mutually exclusively, thereby ideally eliminating any temporal overlap between the HF power and HF data signals. Additionally, as will be discussed in Section III, the proposed approach can also help in simplifying the data coupling/decoupling design by eliminating the need for any complex analog-filtering circuitry.

An overview of the proposed approach is outlined in Section II, while details of the concept-validating experimental prototype are provided in Section III. The sequential HF power-and-data co-transmission approach is implemented on a distributed dc/dc converter for which the closed-loop control algorithm is discussed in Section IV and the experimental results are provided in Section V. Finally, conclusions of the letter are brought out in Section VI.

II. Overview of Sequential Power and Data Co-transmission over an HF Channel

In Fig. 2, $\mathrm{PN}_{n\mathrm{T}}$ ($\mathrm{PN}_{n\mathrm{R}}$) and $\mathrm{DN}_{n\mathrm{T}}$ ($\mathrm{DN}_{n\mathrm{R}}$) refer to the nth power and data transmitter (receiver) nodes, while $\mathrm{S}_{n\mathrm{PT}}$ ($\mathrm{S}_{n\mathrm{DT}}$) and $\mathrm{S}_{n\mathrm{PR}}$ ($\mathrm{S}_{n\mathrm{DR}}$) are switches that connect and dis-

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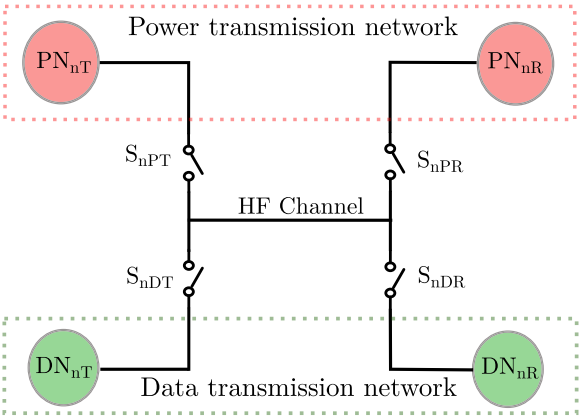


Fig. 2. Overview of supporting power and data co-transmission over an HF channel.

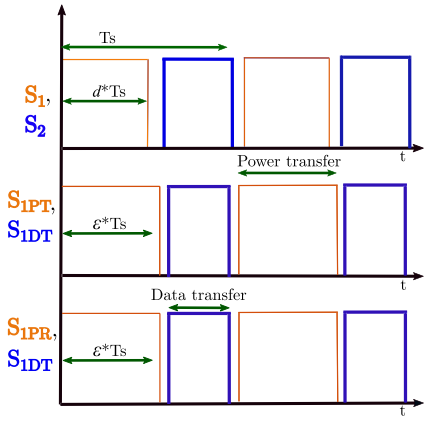


Fig. 4. Timing diagram for the operation of the switches.

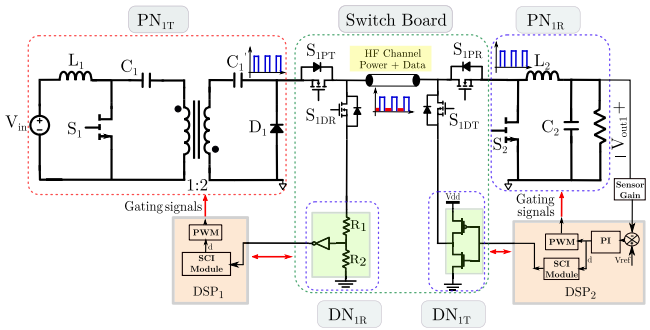


Fig. 3. Schematic of the distributed dc/dc converter, showing $\mathrm{PN_{1T}}$, $\mathrm{PN_{1R}}$, $\mathrm{DN_{1T}}$, $\mathrm{DN_{1R}}$, and the HF channel. $\mathrm{DSP_1}$ ($\mathrm{DSP_2}$) coordinates locally with $\mathrm{PN_{1T}}$ ($\mathrm{PN_{1R}}$) for gating and feedback signals, $\mathrm{DN_{1T}}$ ($\mathrm{DN_{1R}}$) regarding data communication, and switch board regarding sequential power and data co-transmission. Control approach implemented in $\mathrm{DSP_1}$ and $\mathrm{DSP_2}$ are also illustrated, with V_{ref} representing the reference for regulating the output voltage.

connect nth power (data) nodes from the common HF channel. The switches follow the Boolean logic: $\overline{\mathrm{S}_{n\mathrm{PT}}} \bar{\oplus} \overline{\mathrm{S}_{n\mathrm{PR}}} = 1$, $\overline{\mathrm{S}_{n\mathrm{DT}}} \bar{\oplus} \overline{\mathrm{S}_{n\mathrm{DR}}} = 1$, $\mathrm{S}_{n\mathrm{PT}} \oplus \mathrm{S}_{n\mathrm{DT}} = 1$, and $\mathrm{S}_{n\mathrm{PR}} \oplus \mathrm{S}_{n\mathrm{DR}} = 1$, where $\bar{\oplus}$ and $\oplus$ represent XNOR and XOR logic operators, respectively. This ensures that, the transmitting and receiving power (data) switches are synchronized, while the corresponding switches that support power and data transfers operate complementarily. When both $\mathrm{S}_{n\mathrm{PT}}$ and $\mathrm{S}_{n\mathrm{PR}}$ are turned on, $\mathrm{PN}_{n\mathrm{T}}$ and $\mathrm{PN}_{n\mathrm{R}}$ are connected and power is transmitted over the HF channel. Similarly, when $\mathrm{S}_{n\mathrm{DT}}$ and $\mathrm{S}_{n\mathrm{DR}}$ are turned on, data are transferred between $\mathrm{DN}_{n\mathrm{T}}$ and $\mathrm{DN}_{n\mathrm{R}}$ over the HF channel.

III. Details of the Validation Prototype

To obtain an HF channel for sequential co-transmission of power and data, a dc/dc converter is modified as shown in Fig. 3 for distributed realization. The modified circuit has three elements: transmitting and receiving power nodes $\mathrm{PN_{1T}}$ and $\mathrm{PN_{1R}}$, respectively, data transmitter and receiver nodes $\mathrm{DN_{1T}}$ and $\mathrm{DN_{1R}}$, respectively, and switches $\mathrm{S_{1PT}}$ ($\mathrm{S_{1DT}}$) and $\mathrm{S_{1PR}}$ ($\mathrm{S_{1DR}}$) which are used to connect and disconnect the power (data) nodes from the common HF channel. Coded data are sent to $\mathrm{DN_{1T}}$ by $\mathrm{DSP_2}$, which are synchronized to $\mathrm{DSP_1}$ and provides the gating signals for $\mathrm{S_{1PR}}$, $\mathrm{S_{1DT}}$, and $\mathrm{S_2}$. $\mathrm{DSP_1}$ decodes the received data on $\mathrm{DN_{1R}}$ and provides the gating signals for $\mathrm{S_1}$, $\mathrm{S_{1PT}}$, and $\mathrm{S_{1DR}}$.

A timing diagram for the distributed dc/dc converter is provided in Fig. 4. Switches $\mathrm{S_1}$ and $\mathrm{S_2}$ are the power switches and are complimentary to each other. Duty cycle (d) of $\mathrm{S_1}$ determines the output voltage of the distributed dc/dc converter [14]. Transfer switches $\mathrm{S_{1PT}}$ and $\mathrm{S_{1PR}}$ are synchronized to each other and are complementary to the data switches $\mathrm{S_{1DR}}$ and $\mathrm{S_{1DT}}$. $\mathrm{S_{1PT}}$ and $\mathrm{S_{1PR}}$ are also synchronized to $\mathrm{S_1}$ and have a duty cycle (ε) given by $\varepsilon = d + \delta$, where δ is the additional duty cycle added to provide a conducting path for the transformer leakage current through $\mathrm{S_{1PT}}$ and $\mathrm{S_{1PR}}$ to the load when $\mathrm{S_1}$ is turned off. The value of δ depends on the stored leakage energy in the HF transformer.

When $\mathrm{S_{1PT}}$ and $\mathrm{S_{1PR}}$ are active, power is transferred from $\mathrm{PN_{1T}}$ to $\mathrm{PN_{1R}}$, this duration is marked as the power transfer in Fig. 4. For the remaining switching-cycle time (T_s), the HF channel is available for data transmission, which is enabled by turning on $\mathrm{S_{1DR}}$ and $\mathrm{S_{1DT}}$ as illustrated in Fig. 4. The durations for power and data transmissions depend on the value of d. If a low (high) converter output voltage is required, a low (high) d is needed and hence, the time duration for data transmission in T_s is increased (decreased). However, when d is low, for a given channel capacity, data rate can be increased to enhance data baud rate.

Next, a brief description of the data-transfer mechanism used in Fig. 3 is provided.

A. Data-Transmitter and Data-Receiver Nodes

A simple data-transmitter circuit, as shown in Fig. 3 ($\mathrm{DN_{1T}}$), is implemented using an inverting gate-driver IC, which receives data directly from $\mathrm{DSP_2}$ and eliminates the need for any data-amplifier circuitry. An inverting gate-driver IC (IXDI609SIA), with a maximum propagation delay of 60 ns, is chosen and its output voltage peak is fixed at 5 V. A 5 V (0 V) on the gate-driver output corresponds to 0 (1) digital bit being transmitted by the

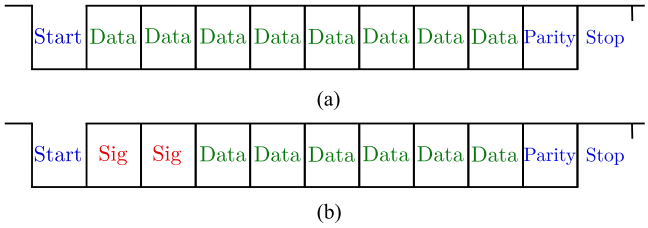


Fig. 5. (a) Asynchronous SCI data-transfer format and (b) modified asynchronous SCI data-transfer format.

DSP_2. The output pin of the gate driver is directly connected to the source of S_{1DT} as illustrated in Fig. 3. Data are only transmitted when S_{1DR} and S_{1DT} are turned on.

A resistive data-receiver circuit is designed to recover the transmitted data signals on the HF channel, as is shown in Fig. 3 (DN_{1R}). The output of the DN_{1R} is fed to the DSP_1 through a digital-isolator interface followed by a logic inverter to recover the transmitted data from DN_{1T}.

B. Data-Transfer Protocol

Serial-communication-interface (SCI) module with data-transfer packet shown in Fig. 5(a) available in the TI's TMS320F28335 DSP is used as the mechanism for asynchronous data transfer [15]. To achieve a robust and reliable data transfer via the HF channel, precursor signature bits along with the already available parity check bits are added to the data being transmitted from DN_{1T}. A total of 11 bits of data as shown in Fig. 5(b), comprising 1 start, 2 signatures, 6 information, 1 parity, and 1 stop bit are transmitted in every data packet. SCI clock frequency of 37.5 MHz is chosen that yields a maximum baud rate of 4.68 Mbps. The maximum number of bits in a packet is limited because of the selected SCI protocol. Different protocols with added data bits can be used to further increase the number of data bits sent in every switching cycle.

IV. Control Approach for the Distributed Converter

Flowcharts explaining the control approach implemented (in DSP_1 and DSP_2) to regulate the output voltage of the distributed dc/dc converter are provided in Figs. 6(a) and 6(b), respectively. As shown in Fig 6(b), at the onset of each switching cycle, output voltage of the converter is sensed and fed to a PI compensator in DSP_2 that generates the required closed-loop duty cycle. This duty cycle is then converted to an 8-bit data format comprising of two precursor signatures bits (detailed in Section III-B).

Next, during the interval of data transfer, marked in Fig. 4, the duty cycle data are transmitted from DN_{1T} to DN_{1R} via the HF channel. Once this data packet reaches the Rx buffer in DSP_1, its precursor signature bits are matched with the stored signature. If the match is good, an acknowledgment is sent to DSP_2 and the duty cycle of PN_{1T} and PN_{1R} are updated in next switching cycle.

If the data received by DSP_1 are corrupted and the matching fails, then no acknowledgment is sent to DSP_2. In such a scenario, duty cycle for each power node remain unchanged and equal to the last successfully transmitted duty cycle. During this period, the distributed converter continues to operate in quasi-closed loop and achieves a quasi-steady state with the delayed duty cycle, until satisfactory communication between the transmitter and the receiver is re-established.

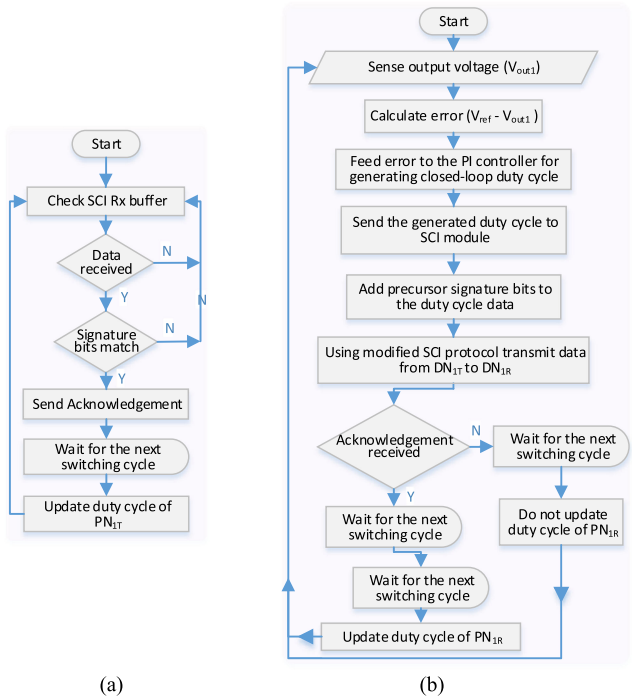


Fig. 6. Flowcharts of control approaches implemented in (a) DSP_1 and (b) DSP_2.

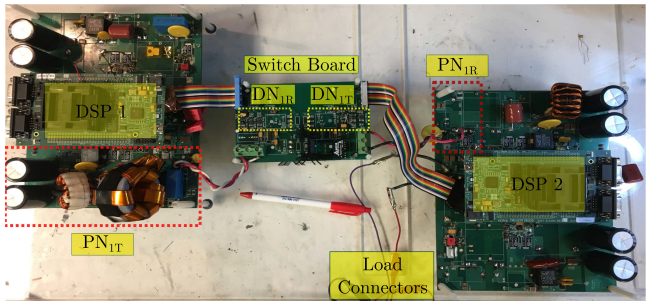


Fig. 7. Experimental prototype of the distributed dc/dc converter shown in Fig. 3.

V. Results

An experimental realization for the circuit, as shown in Fig. 3, is demonstrated in Fig. 7. PN_{1T}, PN_{1R}, and switch board are experimentally realized on separate PCBs and are connected using short twisted wires. TI's TMS320F28335 DSP is selected for generating the gating signals for all the switches and for implementing the modified SCI protocol. The DSP control code is written in C language using TI's Code Composer Studio V3.3. Variation in the duration of power-transfer signal and

TABLE I
SPECIFICATIONS OF THE DISTRIBUTED DC/DC CONVERTER

Transformer turns ratio	Switching frequency	L_1	L_2	C_1	C_1'
2	100 kHz	50 μH	100 μH	6.8 μF	1.5 μF

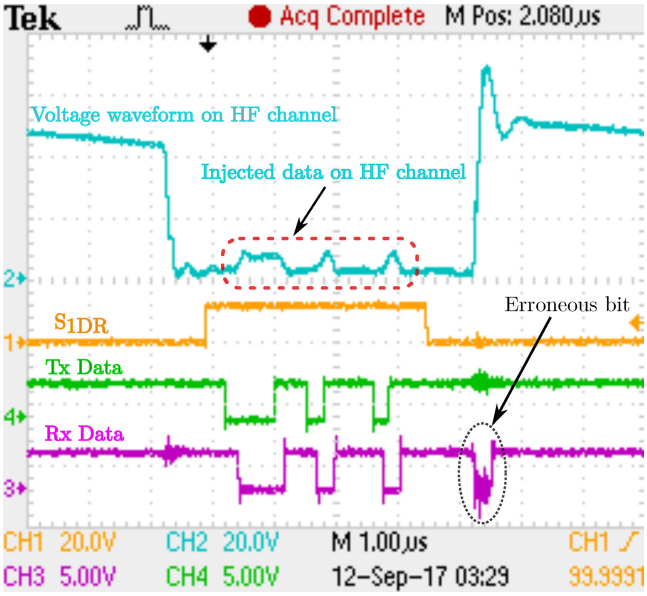


Fig. 8. Experimental waveform (channel 2) shows the sequential co-transfer of HF power and data over the HF channel. Embedded data signals (channels 3 and 4), which are transmitted from DSP2, when S_{1DR} (channel 1) is high, to DSP1 are shown on channels 4 and 3, respectively.

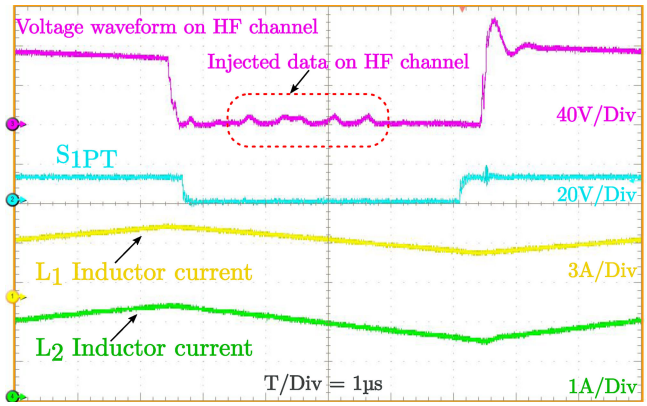


Fig. 9. Experimental waveform (channel 3) shows the sequential co-transfer of HF power and data over the HF channel. Only when S_{1PT} (channel 2) is turned on, the magnitudes of the input and output inductor currents (channels 1 and 4) increase indicating transfer of power between PN_{1T} and PN_{1R} over the HF channel.

TABLE II
EFFECT OF THE FREQUENCY OF POWER TRANSFER ON DATA RATE

Frequency of power transfer (kHz)	80	90	100	110	120
Data rate (Mbps)	4.68	4.68	4.68	4.68	4.68

the variation in the data packets for PN_{1T} (PN_{1R}) and DN_{1R} (DN_{1T}) are handled by DSP_1 (DSP_2). PCB traces on the switch board is used as the HF channel for sequential cotransfer of HF power and data signals.

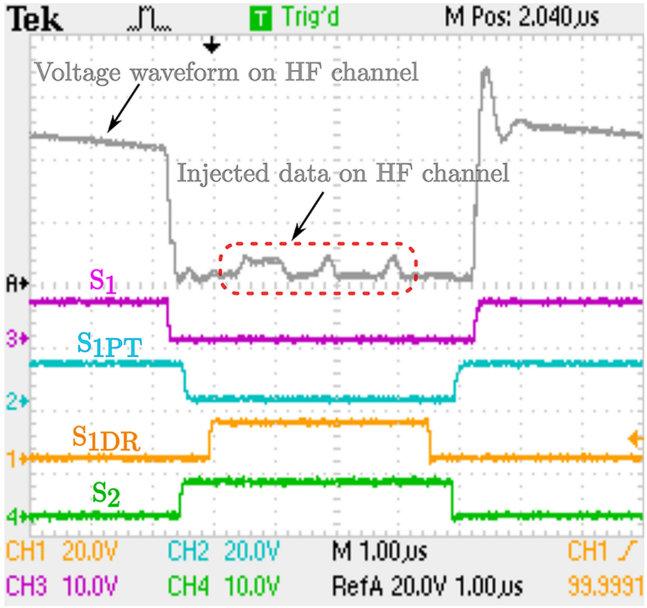
Power-stage parameters are derived using [14] and are captured in Table I. Experimental result for an input voltage of 20 V and a duty cycle of 57% are provided in Figs. 8 and 9. The initial result, in Fig. 8 (channel 2), demonstrates the co-transmission of the high-voltage power and low-voltage data signals. In the above trace, the embedded data signals, which are transmitted from DSP_2, when S_{1DR} is high, to DSP_1 are shown on channels 4 and 3, respectively. A delay of 340 ns is observed between the transmitted and received data signals due to the propagation delay incurred in the digital components and the HF channel. Further, occurrence of an erroneous bit at the onset of the power signal is observed in the received data, this is caused by the voltage drop across R_1 and R_2 in DN_{1R} by the charging current needed to turn off S_{1DR}. This erroneous data bit is rejected in DSP_1 using the modified SCI protocol, which is outlined in Section III-B.

With reference to the cotransfer signal shown on channel 3, Fig. 9 validates the transfer of power when S_{1PT} turned on. During this time, power transfers from the dc source in PN_{1T} to the output load in PN_{1R} over the HF channel. This is indicated by the increase in the magnitudes of the input and output inductor currents. Similarly, when S_{1PT} is turned off, one can observe that, magnitudes of the input and output inductor current decrease.

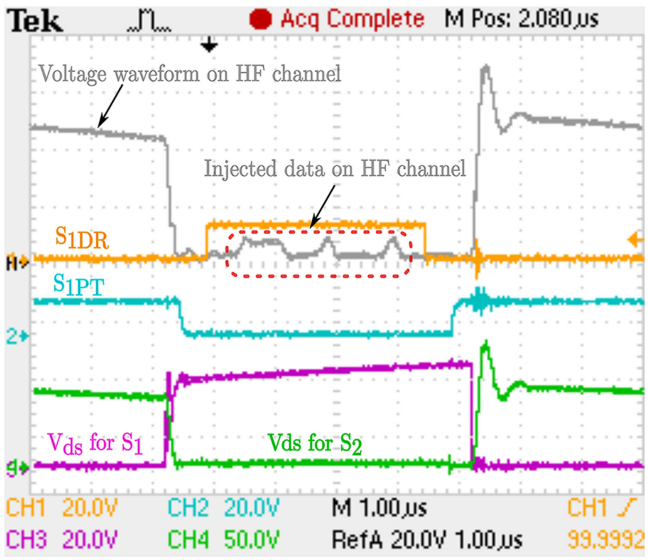
Finally, with reference to the same cotransfer signal, shown in Fig. 8, the status of the local switches S_1 and S_2 in PN_{1T} and PN_{1R}, with reference to S_{1PT} and S_{1DR}, are shown in Fig. 10(a). They comply with the timing diagram in Fig. 4. Fig. 10(b) shows the corresponding drain to source voltage (V_{ds}) across S_1 and S_2.

To test the dependence of data rate on the frequency of power transfer in the proposed sequential cotransfer, the experimental converter is tested by changing the frequency of power transfer between 80 kHz and 120 kHz. Experimental measurements from the test are listed in Table II. A maximum data rate of 4.68 Mbps is obtained irrespective of the frequency of power transfer.

Next, the distributed dc/dc converter is subjected to a cyclic load transient from 36 W to 48 W with a frequency of 20 Hz using Agilent 6060B dc electronic load. A PI compensator-based closed-loop voltage-control approach illustrated in Fig. 3 is implemented in DSP_2 to track a 30 V dc at the output with a fixed input dc voltage of 20 V. The PI compensator is tuned to achieve an acceptable tradeoff between output-voltage regulation and dynamic response. As explained in Section IV, duty cycle computed in DSP_2 is later transferred to DSP_1 over the HF channel for generating gating pulses for S_1, S_{1PT}, and S_{1DR}. In Fig. 11, output voltage (V_{out1}) is plotted along with the output load current of the distributed dc/dc converter. It is observed that the closed-loop converter tracks the output voltage with a



(a)



(b)

Fig. 10. Experimental waveform (Ref A) shows the sequential cotransfer of HF power and data over the HF channel, along with (a) gating signals for S_1, S_{1PT}, S_{1DR}, and S_2, and (b) V_{ds} waveforms across switches S_1 and S_2.

continually changing load current with the help of the duty cycle information being transmitted in every switching cycle.

Further, to emulate the effect of communication failure, the distributed dc/dc converter was subjected to a delay of n switching cycle, i.e., the closed loop duty cycle was updated once in n switching cycles. As explained in Section IV, during this delayed period, the converter runs with the last successfully transmitted duty cycle value. For a $V_{\rm ref}$ of 30 V and $n = 14$, simulation along with experimental results for the state error trajectories of the output voltage ($e_{V\,\rm out} = V_{\rm ref} - V_{\rm out1}$) are provided in Figs. 12(a) and (b), respectively. It can be observed that the state error trajectory of the output voltage converges for both the delayed and non-delayed system showing its reachability.

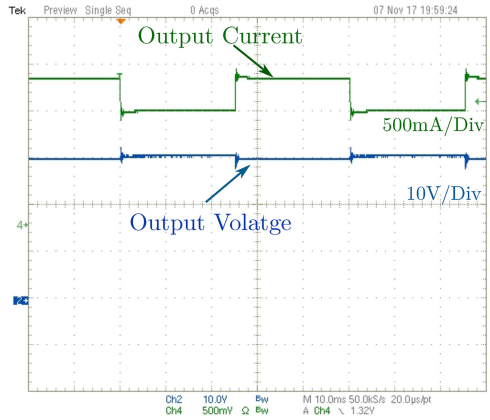


Fig. 11. Converter output-voltage and output-current waveforms during a cyclic 20-Hz load variation between 48 W and 36 W. A PI compensator is designed to track the output voltage of 30 V given an input voltage of 20 V.

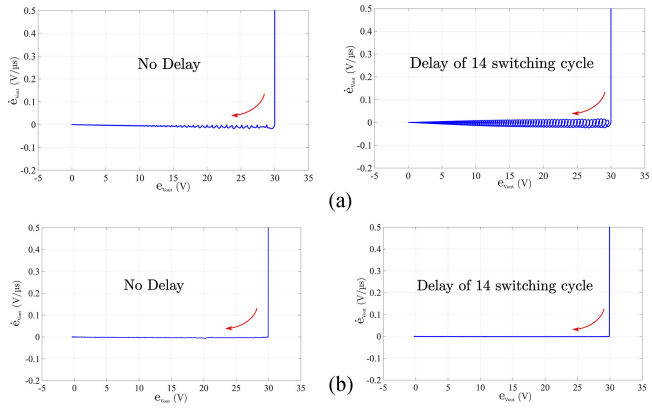


Fig. 12. (a) Simulated and (b) experimental results for the state error trajectories of the output voltage with no delay and a delay of 14 switching cycle. Converges of state error trajectory guarantees the reachability of the delayed and non-delayed system.

VI. Conclusion

An approach for cotransfer of HF power and data signals over a common HF channel is outlined and validated using an experimental dc/dc converter. It is experimentally demonstrated that the data transfer rate in a sequential cotransfer is independent of the frequency of power transfer. Further, it is shown that no complex analog-filtering circuitry is required for coupling and decoupling data signals on the HF channel, as is usually the case in conventional PLC. In the experimental converter, transitional coupling between the power- and the data-transmissions nodes is observed due to non-ideal behavior of the semiconductor devices. To eliminate data corruption caused by it, a modified SCI protocol is implemented. Also, steady-state stability of the system during an event of communication failure is established both using simulation and experimental results. A maximum data baud rate of 4.68 Mbps is achieved for a power transfer frequency varying between 80 kHz and 120 kHz.

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