A DC/DC Modular Current-Source Differential-Mode Inverter

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***Abstract*— A single-stage differential-mode current-fed zero-current-switching inverter has been designed. This inverter has two modules of dc/dc converters that are connected differentially to the input source. This inverter does not require 60-Hz transformer, front-end dc/dc converter, and can boost a low-voltage input to ac output using a compact low-turns-ratio transformer because of the added voltage gain of the topology. Main switches of the inverter are soft switched. The inverter requires a smaller high-frequency transformer because of high-frequency switching, bipolar transformer current, and voltage in every switching cycle, and because the transformer sees only half of the input current. The modularity of the inverter extends the scope of the topology to be used as a dc/dc converter, single-phase inverter, and also the possibility of extending the topology to both split phase and three phase. A harmonic-compensation control is designed and implemented to reduce the total harmonic distortion of the output waveform using a proportional-resonant controller. The design and the analysis of the inverter have been validated using simulation results in the Saber simulator.**

***Index Terms*— Current-source inverter, differential mode, high-frequency link, modulation, renewable/alternative energy, switch-mode power supply.**

I. Introduction

SEVERAL single-stage inverters, both isolated and nonisolated inverters have been proposed in the past for applications, including solar energy. One of the single-stage topologies outlined in [1] achieves dc/ac conversion by connecting the inputs of two identical dc/dc boost converters in parallel with a dc source and the load is connected across the outputs of the two dc/dc converters. As opposed to a conventional buck voltage source inverter, this topology can generate an output voltage higher than the input voltage. However, the topology has a nonisolated architecture, the switches operate at a low switching frequency, and the size of the magnetics is large leading to a larger footprint for a nonisolated topology.

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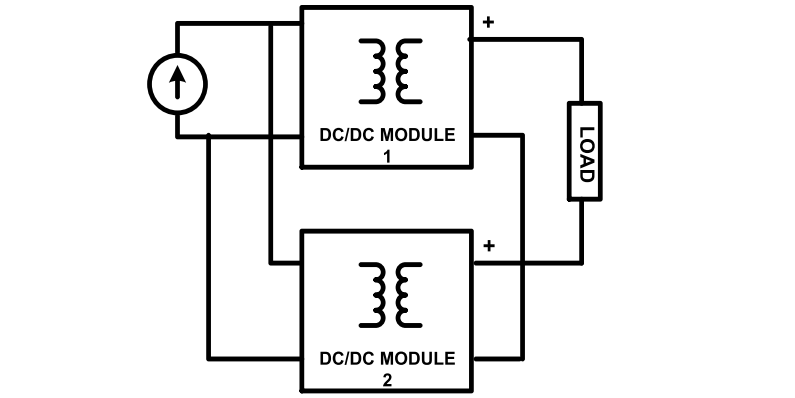
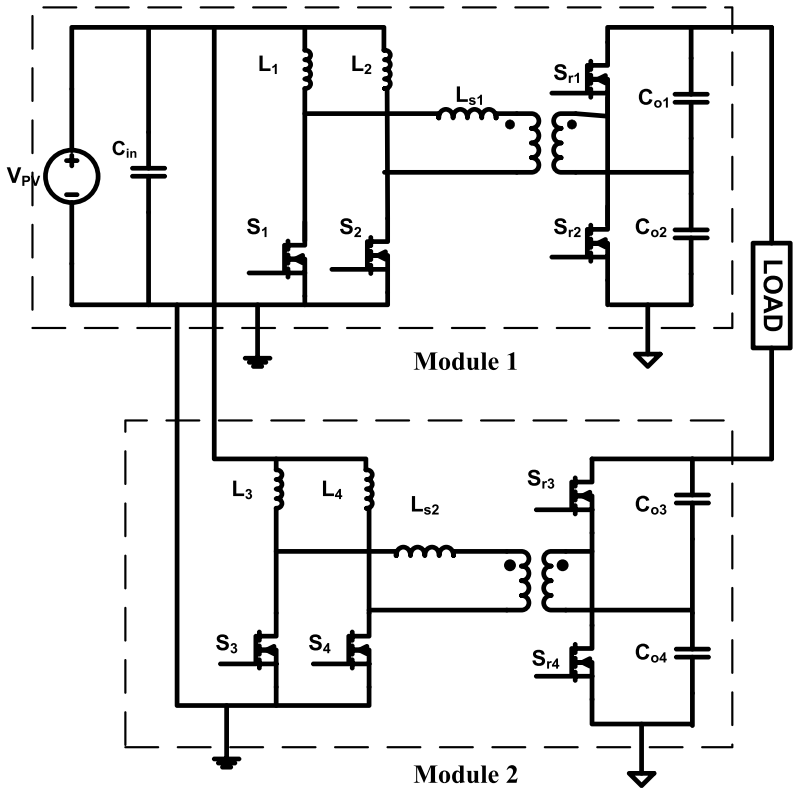
A differential buck–boost inverter, proposed in [2], operates similar to the differential boost inverter in [1]. This inverter can produce an output voltage either higher or lower than the input dc voltage. Another single-stage buck–boost topology was outlined in [3] and overcomes the disadvantage of small input voltage range of the buck–boost topology proposed in [2]. However, this inverter requires a split input dc voltage source. Two sets of input voltage sources and buck–boost chopper type circuits are connected in antiparallel to the output capacitor, which generates the output. Both the chopper circuits are operated at fixed-frequency in a discontinuous conduction mode. Both the buck–boost topologies do not provide a high-frequency galvanic isolation and operate at a low switching frequency; however, they have lower component count. Overall, one of the common challenges with the buck–boost derived topologies is the high peak inductor current stress due to the sudden transfer of energy through the inductors from source to load during each switching cycle. A single-stage flyback inverter topology was described in [4]. It comprised bidirectional flyback converters that are connected in parallel to the input voltage source and the load is connected across the two converters. The major advantage of this topology over the above-mentioned topologies is the galvanic isolation provided by the high-frequency transformers in both the flyback converters. However, the galvanic isolation in this topology requires an increased footprint. The switches also incur the switching losses and, hence, are limited to low switching frequency operation. In [5], a single-stage full-bridge buck–boost inverter is outlined. Even though the inverter topology has four power switches and two diodes, only two switches are soft switched. In addition, the generated sinusoidal waveform consists of quasi-sinusoidal pulses. This topology also does not isolate the source and the load or grid. A single-stage buck–boost pulsewidth modulation power inverter is provided in [6]. It has two buck–boost choppers forming a four switch bridge and an additional two more power switches for synchronous commutation in each half cycle of the output. The major advantage of this topology is the galvanic isolation provided by the high-frequency transformer. However, this topology is only suitable for low-power applications with a reported maximum power of 140 W. Finally, another single-stage topology, employing differential Ćuk topology [7] achieves a direct dc/ac conversion by connecting the load differentially across two bidirectional dc/dc Ćuk converters and by modulating them sinusoidally with 180° phase difference. This topology utilizes only four main switches, making the inverter topology simple and



(a)



(b)

Fig. 1. (a) and (b) Architecture and topology of the proposed differential-mode ZCS inverter.

reducing the cost. The differential Ćuk inverter also has room for magnetics integration, thereby reducing the footprint of the inverter. However, this topology while employing continuous modulation scheme does not employ any loss-mitigating techniques for the main switches and need special care for alleviating voltage spikes.

Several single-stage direct-power-conversion architectures proposed in the past [8]–[19] have increased footprint, no galvanic isolation, lower boost capability, stresses in the power switches due to hard switching, and stress in the components due to spikes that arise because of difference in the energies between the source and the load and are not suitable for medium-power applications. The proposed inverter [shown in Fig. 1(b)] is based on such a topological approach. It is a differential-mode [Fig. 1(b)] current-fed zero-current-switching (ZCS)-based voltage-doubling photovoltaic (PV) inverter. This inverter has the following features:

1) boosts low-voltage (30–60 V) input to a 120 V [root mean square (rms)]/60-Hz output;
2) does not require a bulky line transformer;
3) does not require a front-end dc/dc converter;
4) has inherent voltage boost/gain property, thereby reducing the reliance on the transformer turns ratio;
5) voltage-doubling half-bridge reduces the need to two secondary switches and the transformer turns ratio to half;
6) a smaller isolation transformer is needed because the inverter switches at 100 kHz, the transformer voltage and current are bipolar in every switching cycle, and

only half the input current flows through the transformer at any given instant of time;

7) since the operation of the inverter is in differential mode, the ZCS scheme for individual dc/dc converters [20] retains in effectiveness for the inverter.

II. Principle of Operation

The basic inverter has two individual dc/dc converter modules, as shown in Fig. 1(a). The primaries of the two individual dc/dc converters, sourced by the PV energy source, are connected in differential mode and the output of the proposed current-sourced inverter is the difference in the outputs of the two individual dc/dc converter modules. Each module has two primary-side switches, namely, S_1 and S_2 and S_3 and S_4 and corresponding secondary-side switches S_{r1} and S_{r2} and S_{r3} and S_{r4}, respectively. The switching frequency of the inverter is 100 kHz. The switches in each module are modulated, so that the individual converters produce a dc-biased sine wave output, so that each converter only produces a unipolar voltage. The modulation of each converter is 180° out of phase with the other, so that the voltage excursion at the load is maximized. That is, switch pairs S_1 and S_2 and S_3 and S_4 are operated in the same way but with a phase difference of 180°. Since the load is connected differentially across the converters, the dc-bias appearing at either end of the load with respect to ground gets cancelled and the differential dc voltage across the load is zero. Switch pairs S_1–S_{r1}, S_2–S_{r2}, S_3–S_{r3}, and S_4–S_{r4} are triggered with complementary pulses. Under hard-switching condition, the output voltages of the individual converters are given by the following equations:

$$V_{o1} = \frac{2nV_{\rm PV}}{1-d_1}, \quad V_{o2} = \frac{2nV_{\rm PV}}{1-d_2}$$

where d_1 and d_2 are the duty ratios of the primary-side switches of the first and second modules, respectively, described in Section III-B. The symbol n represents the turns ratio of the transformers in both the modules. The output voltage of the inverter is the difference in the output voltages of the individual dc/dc converter modules and is given by the following equations:

$$V_o = V_{o1} - V_{o2}, \quad V_o = \frac{2nV_{\rm PV}}{1-d_1} - \frac{2nV_{\rm PV}}{1-d_2}$$
$$V_o = 2nV_{\rm PV}\left[\frac{d_1-d_2}{(1-d_1)(1-d_2)}\right].$$

Let $d_1 = D + D^{'}\sin(\omega t)$ and $d_2 = D - D^{'}\sin(\omega t)$, then the voltage gain of the inverter is given by the following equation:

$$\frac{V_o}{V_{\rm PV}} = 4n\sin(\omega t)\left[\frac{D^{'}}{(1-D)^2 - D^{'2}\sin^2(\omega t)}\right].$$

The voltage gain of the inverter depends on the transformer turns ratio and the duty ratio. Thus, an optimum balance between the turns ratio (n) and the duty ratio is the key. The primary-side switches have a duty ratio range of 50%–100%. The inverter cannot be operated below a duty ratio of 50% to avoid a condition of inconsistency in the input inductors currents. Finally, the overall timing sequence of the inverter [shown in Fig. 1(a)] is shown in Fig. 2. Using that as a reference, the hard- and soft-switching modes of the inverter are shown.

A. Hard-Switched Inverter Modes

The hard-switched modes of the topology in Fig. 1(b) are presented in Fig. 3(a)–(f). When S_1 and S_2 or S_3 and S_4 of each of the modules are turned ON simultaneously, the boost mode of the individual converter is initiated. During this mode, the output capacitors of one module feed energy to the output capacitors of the other module through the load. For all other switching configurations, there is an exchange of power between the primary and the secondary of the individual dc/dc converter module as well as from one dc/dc converter module to another. In addition, in these modes, there is a localized charging of output capacitor of one of the dc/dc converter modules. The direction of power flow between the individual modules depends on the time-domain voltage and current waveforms. For instance, for a unity-power-factor passive load, during a positive line cycle of the output voltage (across the load), power flows from the PV source via the upper module to the bottom module, while during the negative half cycle, power flows via bottom module to the upper module. The operation of the inverter in the positive half cycle of the output is analyzed by the following modes.

Mode 1: Fig. 3(a) represents the hard-switched mode of the inverter. During this interval, the primary-side switches of both the modules, S_1, S_2, S_3, and S_4, are turned ON. Hence, current in both the transformers is zero. Power to the load is supplied by the output capacitors of the upper module C_{o1} and C_{o2}. The output capacitors of the lower module, C_{o3} and C_{o4}, are charged in this mode. The lower dc/dc converter acts as the receiving module in this mode. The input current in the upper and lower modules from the PV source is given by $i_{\rm in1}$ and $i_{\rm in2}$, respectively. The currents through the primary-side switches are given by the following equations:

$$i_{s1} = i_{s2} = \frac{i_{\rm in1}}{2}, \quad i_{s3} = i_{s4} = \frac{i_{\rm in2}}{2}.$$

Mode 2: Fig. 3(b) represents the hard-switched mode of the inverter. In this interval, the primary-side switches of the upper and lower modules, S_1 and S_3, respectively, and the secondary-side switches of the upper and lower modules, S_{r2} and S_{r4}, respectively, are turned ON. The negative current raises through the leakage of the upper module's transformer, L_{s1}, and the current through switch S_1 raises with the same slope as the current through L_{s1}. Output capacitor C_{o2} of the upper module is charged and capacitor C_{o1} discharges through the load C_{o3} and the secondary of the transformer of the lower module. Output capacitor C_{o4} of the lower module is also charged in this mode. The current through the leakage inductance L_{s2} of the transformer in the lower module is positive and begins to increase with the same slope as the current through the leakage inductance L_{s1}. The currents through the primary-side switches and the leakage inductors are given by the following equations:

$$i_{\rm Ls1} = -\frac{V_{o1}}{2nL_{s1}}(\Delta t), \quad i_{\rm Ls2} = \frac{V_{o2}}{2nL_{s2}}(\Delta t)$$
$$i_{s1} = \frac{i_{\rm in1}}{2} + i_{\rm Ls1}, \quad i_{s3} = \frac{i_{\rm in2}}{2} + i_{\rm Ls2}$$

where Δt is the time interval for Mode 2.

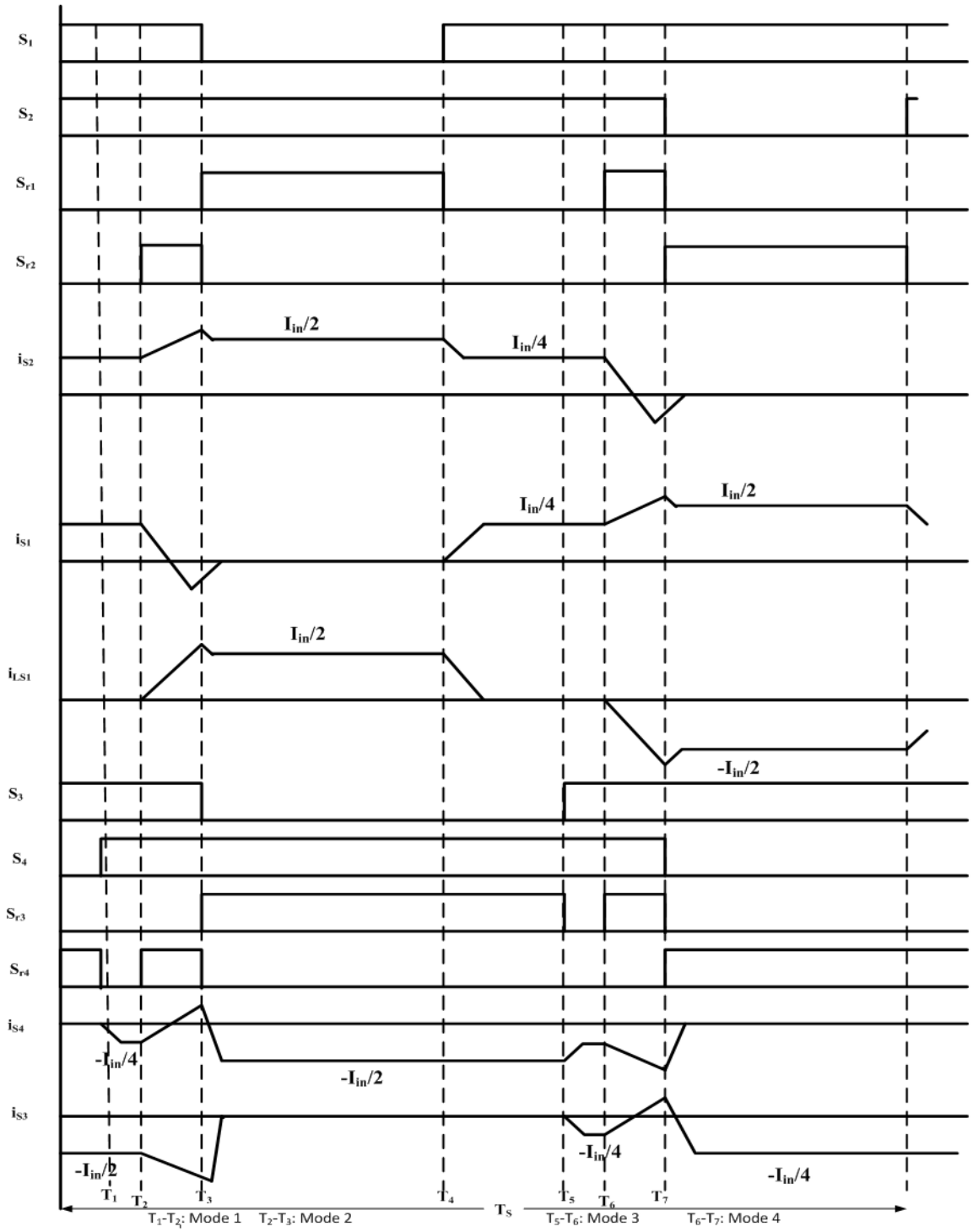


Fig. 2. Timing diagram of the inverter shown in Fig. 1b during one switching cycle for positive half cycle of the load.

Mode 3: Fig. 3(c) represents the hard-switched mode of the inverter. This mode is similar to the mode1 where all of the primary-side switches in both the modules are turned ON and all of the secondary-side switches in both the modules are turned OFF. The current through the transformers in both the modules is zero. The output capacitors of the upper module feed the load and the lower module.

Mode 4: Fig. 3(d) represents the hard-switched mode of the inverter. In this mode, the primary-side switches of the upper and lower modules, S_2 and S_4, respectively, and the secondary-side switches of the upper and lower modules, S_{r1} and S_{r3}, respectively, are turned ON. The current through the primary-side switch in the upper module, S_1 in Mode 3, is diverted to L_{s1} due to the voltage across the primary of the upper transformer, which in turn, is due to the voltage

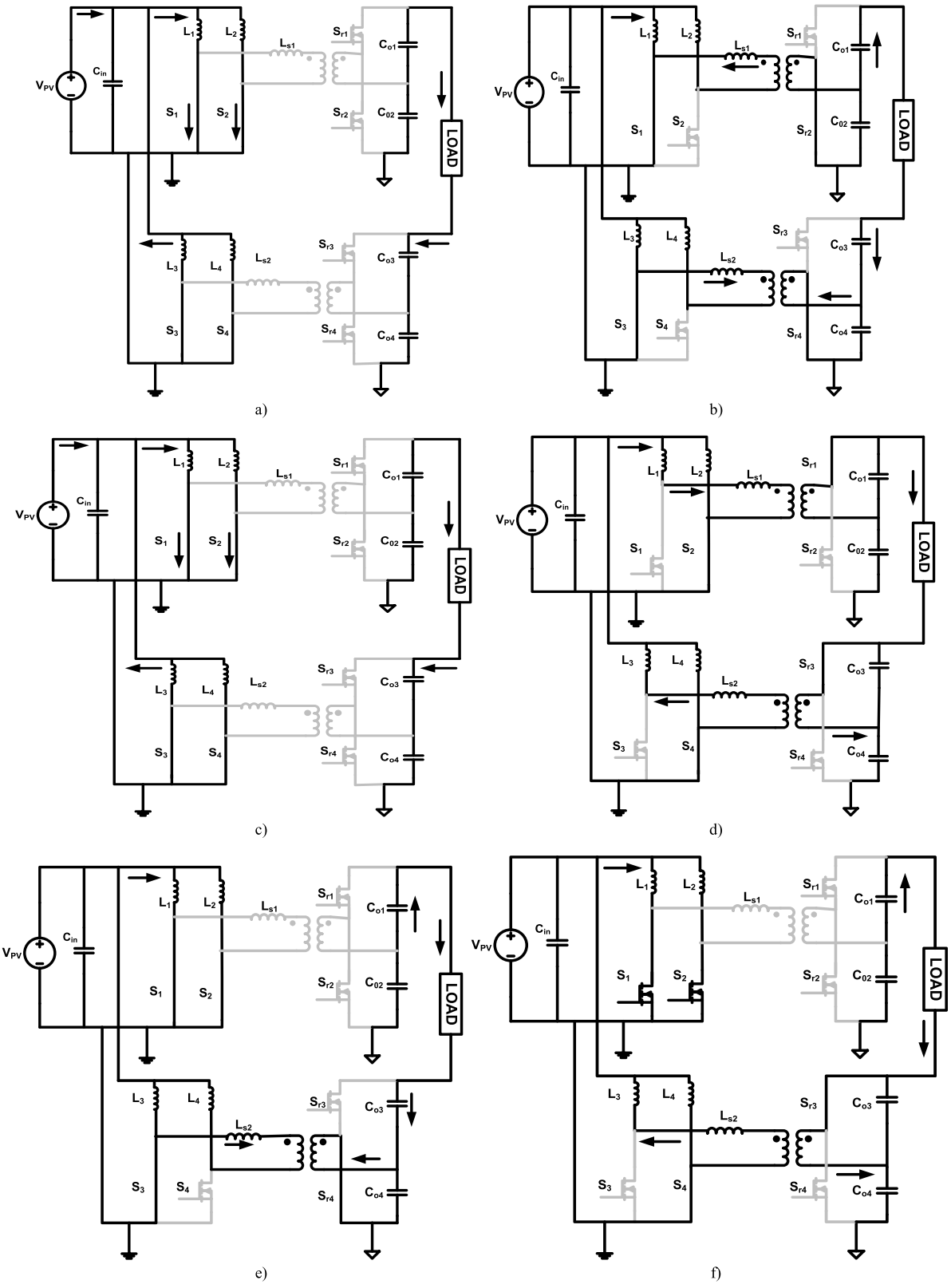


Fig. 3. Hard-switching modes of the inverter shown in Fig. 1(b). (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

across the output capacitor of the upper module, C_{o2}. Output capacitors C_{o1} and C_{o3} are charged by the PV source. Output capacitor C_{o2} discharges through the load, the transformers' secondary, and C_{o4}. The current through S_2 and the negative current through L_{s2} rise with the same slope as the current through L_{s1}. The currents through the primary-side switches

TABLE I
POSSIBLE SWITCHING STATES OF THE INVERTER UNDER HARD-SWITCHED OPERATION

Switching states of the inverter	S_1	S_2	S_3	S_4
a.	1	1	1	1
b.	1	0	1	0
c.	0	1	0	1
d.	1	1	1	0
e.	1	1	0	1
f.	0	1	1	1
g.	1	0	1	1

and the leakage inductors are given by

$$i_{\mathrm{Ls1}} = \frac{V_{o1}}{2nL_{s1}}(\Delta t), \quad i_{\mathrm{Ls2}} = -\frac{V_{02}}{2nL_{s2}}(\Delta t)$$
$$i_{s2} = \frac{i_{\mathrm{in1}}}{2} + i_{\mathrm{Ls1}}, \quad i_{s4} = \frac{i_{\mathrm{in2}}}{2} + i_{\mathrm{Ls2}}.$$

Mode 5: Fig. 3(e) represents the hard-switched mode of the inverter. In this mode, the primary-side switches of the upper module, S_1 and S_2, the primary-side switch of the lower module, S_3, and the secondary-side switch of the lower module, S_{r4}, are turned ON. The current through the transformer in the upper module is zero. Output capacitors of the upper module, C_{o1} and C_{o2}, discharge through the load, the output capacitor of the lower module, C_{o3}, and the secondary of the transformer of the lower module. Output capacitor C_{o4} of the lower module is also charged in this mode. The current through the leakage inductance of the lower module, L_{s2}, is positive. The currents through switches S_3 and L_{s2} are given by

$$i_{s3} = \frac{i_{\mathrm{in2}}}{2} + i_{\mathrm{Ls2}}, \quad i_{\mathrm{Ls2}} = \frac{V_{o2}}{2nL_{s2}}(\Delta t).$$

Mode 6: Fig. 3(f) represents the hard-switched mode of the inverter. In this mode, the primary-side switches of the upper module, S_1 and S_2, the primary-side switch of the lower module, S_4, and the secondary-side switch of the lower module, S_{r3}, are turned ON. The current in the transformer of the upper module is zero. Output capacitors of the upper module, C_{o1} and C_{o2}, discharge through the load, the secondary of the transformer of the lower module, and capacitor C_{o4}. Output capacitor of the lower module, C_{o3}, is also charged in this mode. The currents through L_{s2} and switch S_4 are given by

$$i_{\mathrm{Ls2}} = -\frac{V_{o2}}{2nL_{s2}}(\Delta t), \quad i_{s4} = \frac{i_{\mathrm{in2}}}{2} + i_{\mathrm{Ls2}}.$$

Modes 5 and 6 determine the maximum point and the zero crossing of the output. The zero crossing occurs when difference in the output of the two modules is zero; while the maximum point occurs when the difference of the individual outputs is maximum. The feasible switching states of the inverter are provided in Table I. The first set of three switching states (i.e., a–c) forms major part of a switching cycle. The last set of four switching states (i.e., d–g) exists for a shorter duration and may exist either in the positive half cycle or in the negative half cycle. Switching states, d–g, occur in the vicinity of the maximum, the minimum, or the zero-crossing point of the output voltage.

B. Zero-Current-Switching Inverter Modes

For the ZCS-based soft-switched operation, in between Modes 1–6, every time a primary switch has to be turned OFF, one secondary switch is also turned ON for a very short duration, leading to additional modes, as shown in Fig. 4. For instance, secondary-side switch S_{r2} is turned ON before the turn-OFF of primary-side switch S_1 in the upper module. The duration for which S_{r2} has to be turned ON depends on the current through switch S_1. The following modes are the additional ZCS modes of the inverter. The ZCS inverter modes build on [20], which addresses dc/dc converter; for the differential-mode inverter outlined in this paper, there are some operational differences since each dc/dc module is subjected to time-varying operation.

Mode 1→2 [Fig. 4(a)]: This mode is introduced to turn-OFF primary-side switches S_2 and S_4 in the top and bottom modules, respectively, before Mode 2. Secondary-side switches S_{r1} and S_{r3} are turned ON to aid the ZCS of S_2 and S_4 in Mode 2. When S_{r1} is turned ON, the voltage across output capacitor C_{o1} is applied across the secondary of the transformer. This causes a voltage at the primary of the transformer, and hence, the current through switch S_2 is diverted to leakage inductor L_{s1}, allowing the switch to turn-OFF in ZCS condition. Capacitor C_{o2} discharges through the load, C_{o3}, and the secondary of the transformer.

Mode 3→4 [Fig. 4(b)]: This mode is introduced to turn-OFF primary-side switches S_1 and S_3 in the top and bottom modules, respectively, before Mode 4. Secondary-side switches S_{r2} and S_{r4} are turned ON to aid the ZCS of S_1 and S_3. When S_{r2} is turned ON, the voltage across output capacitor C_{o2} is applied across the secondary of the transformer. This causes a voltage at the primary of the transformer, and hence, the current through switch S_1 is diverted to leakage inductance L_{s1}, allowing the switch to turn-OFF in ZCS condition. In this mode, capacitor C_{o1} discharges through the load, capacitor C_{o3}, and the secondary of the transformer.

Mode 4→5 [Fig. 4(c)]: This mode is introduced to turn-OFF primary-side switch S_4 in the bottom module by turning ON secondary switch S_{r3} before Mode 5. When switch S_{r3} is turned ON, the voltage across output capacitor C_{o3} is applied across the secondary of the lower transformer. This causes voltage across the primary of the transformer, and hence, the current through primary switch S_4 is diverted to leakage inductance L_{s2}. Thus, S_4 turns OFF in ZCS condition.

Mode 5→6 [Fig. 4(d)]: This mode is introduced to turn-OFF the primary-side switch of the bottom module S_3 by turning ON S_{r4} before Mode 6. When switch S_{r4} is turned ON, the voltage across output capacitor C_{o4} is applied across the secondary of the lower transformer. This causes voltage across the primary of the transformer, and hence, the current through switch S_3 is diverted to leakage inductor L_{s2}, thereby enabling ZCS turn-OFF of switch S_3. This additional duty ratio of the secondary-side switches is represented as d_r.

III. INVERTER POWER-STAGE DESIGN

The power-stage specifications of the differential inverter are as follows:

1) input voltage (V_{PV}): 36 V;

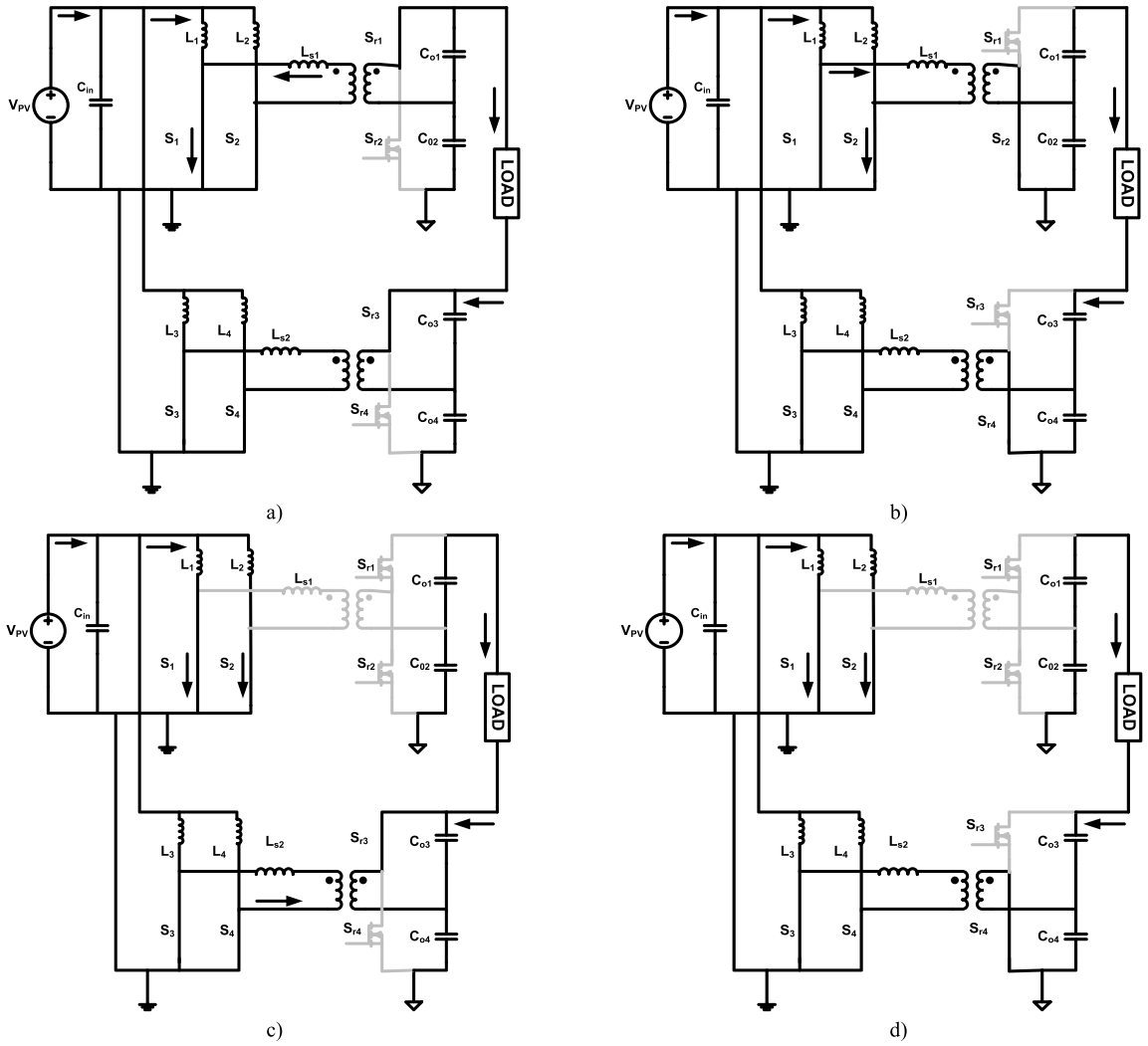


Fig. 4. Soft-switching modes of the inverter shown in Fig. 1(b). (a) Mode 1→2. (b) Mode 3→4. (c) Mode 4→5. (d) Mode 5→6.

2) rms output voltage (V_{orms}): 120 V;
3) output power (P_o): 500 W;
4) switching frequency (f_s): 100 kHz.

The lower limit of the duty ratios of the two modules, d_1 and d_2, is 0.5 to avoid a condition of inconsistency in the currents through the input inductors. For further analysis, the constant offset D is fixed at 0.64 and the upper and lower limits of d_1 and d_2 vary between 0.5 and 0.78. The key factors that influence the design of the inverter are outlined below.

A. Input Inductors

The design of the input inductors for the current-source inverters has important tradeoff with regard to the size. The larger the input inductors, the lower the current ripple and, hence, the PV average power loss. The input inductors in both the modules are identical. The average energy stored in the inductors is given by the following equation:

$$E_L = \frac{1}{2} L i_L^2$$

where i_L is the current through the input inductor. Larger energy storage (lower current ripple) ensures a lower average PV power loss. But, larger the input inductor, the size and the losses associated with the inductor also increase. Fig. 5 shows the various values of input inductors as a function of input current ripple and size (number of windings for a given wire dimension). The optimum value of input inductor is chosen as 500 μH.

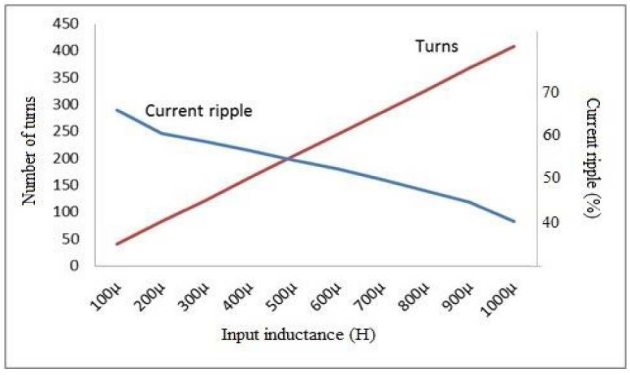


Fig. 5. Input inductor versus input current ripple versus number of turns in the input inductors.

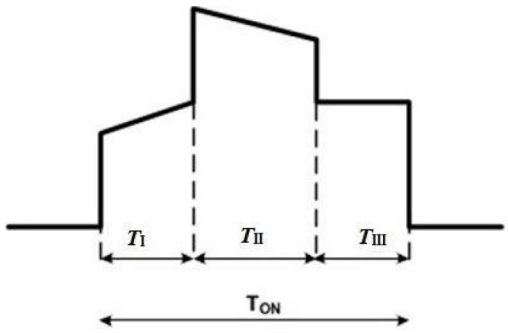


Fig. 6. Current through a primary-side switch.

B. Primary-Side Switches

The primary-side switches S_1, S_2, S_3, and S_4 of both the modules are operated in a sinusoidal manner with a duty ratio range of 50%–100% having a constant dc offset. The duty ratios of the primary-side switches are given by the following equations:

$$d_1 = D + D^{'}\sin(\omega t), \quad d_2 = D - D^{'}\sin(\omega t)$$

where D is the constant dc offset in the duty ratios. For the analysis, the dc offset D is fixed and the upper and lower limits of d_1 and d_2 vary between 0.5 and 0.78. The maximum voltage across the primary-side switches in both the modules is given by the following equations:

$$V_{\rm sw1} = \frac{V_{o1}}{2n}, \quad V_{\rm sw2} = \frac{V_{o2}}{2n}$$

where V_{o1} and V_{o2} are the output voltages at Module 1 and Module 2, respectively. The current through the primary-side switches in both the modules is given by the following equations:

$$i_{s1} = \frac{i_{\rm in}}{2} + i_{\rm Ls1}, \quad i_{s2} = \frac{i_{\rm in}}{2} + i_{\rm Ls1}$$
$$i_{s3} = \frac{i_{\rm in}}{2} + i_{\rm Ls2}, \quad i_{s4} = \frac{i_{\rm in}}{2} + i_{\rm Ls2}$$

where $\rm I_{Ls1}$ and $i_{\rm Ls2}$ are the currents through the leakage inductances and $i_{\rm in}$ is the current input to the inverter. Fig. 6 shows the current through the primary-side switch during one switching cycle under hard-switching condition. The turn-ON time of the switches during one switching cycle can be divided into three intervals for the ease of the analysis, namely, $T_{\rm I}$, $T_{\rm II}$, and $T_{\rm III}$. Thus, the duty ratio, d_1 (or d_2), of the primary-side switches can be represented as the following equation:

$$T_{\rm ON} = T_{\rm I} + T_{\rm II} + T_{\rm III}.$$

The switches are modulated such that

$$(1 - T_{\rm ON}) = T_{\rm II}.$$

Some important factors that govern the selection of a semiconductor device are the maximum voltage across the switch, the conduction and switching losses, and the switch capacitance. The conduction loss is the energy lost in the switch during the ON-state and it depends on the voltage across the switch and the current through it. The power loss associated with a semiconductor device during conduction is given by the following equation:

$$P_{\rm cond,loss} = \frac{1}{T_{\rm SW}}\int_0^{T_{\rm SW}} r_{\rm ON} i_{\rm sw}(t)^2 dt$$

where $r_{\rm ON}$ is the ON-state resistance of the switch, $T_{\rm SW}$ is the switching period, $i_{\rm sw}(t)$ is the instantaneous value of the current through the switch, and $i_{\rm sw,rms}$ is the rms value of the current through the switch.

The rms current of any one of the primary-side switches in Module 1 and Module 2 is derived as follows:

$$I_{\rm sw,rms,Primary} = \sqrt{\frac{1}{T_{\rm sw}}\left[\int_0^{T_{\rm ON}} (I_{\rm sw})^2 dt + \int_{T_{\rm ON}}^{T_{\rm OFF}} (I_{\rm sw})^2 dt\right]}.$$

Between the time interval $T_{\rm ON}$ to $T_{\rm OFF}$, the switch current is 0. The time interval between 0 and $T_{\rm ON}$ is divided into three intervals. Between the time interval 0 and $T_{\rm I}$, the current through the switch is half the input current to the particular module. The switch current between time interval $T_{\rm I}$ and $T_{\rm II}$ is $((i_{\rm in1}/2) + i_{\rm LS1})$. The switch current between intervals $T_{\rm II}$ and $T_{\rm III}$ is half the input current to the particular module. Furthermore

$$d_{\rm I} = \frac{T_{\rm I}}{T_{\rm sw}}, \quad d_{\rm II} = \frac{T_{\rm II}}{T_{\rm sw}}, \quad d_{\rm III} = \frac{T_{\rm III}}{T_{\rm sw}}.$$

Substituting these, the rms switch current through each primary switch in each module is obtained as follows:

$$i_{\rm sw,rms,Primary1} = \sqrt{\left(\frac{i_{\rm in1}}{2}\right)^2 d_{\rm III} + i_{\rm Ls1}(i_{\rm Ls1} + i_{\rm in1})[d_{\rm II} - d_{\rm I}]}$$
$$i_{\rm sw,rms,Primary2} = \sqrt{\left(\frac{i_{\rm in2}}{2}\right)^2 d_{\rm III} + i_{\rm Ls2}(i_{\rm Ls2} + i_{\rm in2})[d_{\rm II} - d_{\rm I}]}$$

where $i_{\rm sw,rms,Primary1}$ is the rms switch current through each primary-side switch in Module 1, $i_{\rm Ls1}$ is the current through the leakage inductance of the transformer in Module 1, $i_{\rm sw,rms,Primary2}$ is the rms switch current through each primary-side switch in Module 2, and $i_{\rm Ls2}$ is the current through the leakage inductance of the transformer in Module 2. The chosen switch is IPP200N25N3 G, with an ON-state resistance of 20 mΩ, maximum continuous drain current (I_D) of 64 A, and drain–source breakdown voltage ($V_{\rm DS}$) of 250 V. Table II shows the theoretical and simulated conduction loss for the primary switches. Fig. 7 shows the conduction loss in all the primary-side switches for both modules for a single IXTP50N25T switch, single IPP200N25N3 G, and four IPP200N25N3 G switches in parallel. The switch number IXTP50N25T has a 50-mΩ ON-state resistance, while the chosen switch IPP200N25N3 G has a 20-mΩ ON-state resistance.

C. Leakage Inductance

When both the primary-side switches in a module are ON, the current through the transformer (or leakage inductance) is zero. For all other cases, the current through the leakage inductance is given by the following equations:

$$i_{\rm Ls1} = \frac{V_o}{2nL_{s1}}(\Delta t), \quad i_{\rm Ls2} = \frac{V_o}{2nL_{s2}}(\Delta t)$$

TABLE II

THEORETICAL [21] AND SABER SIMULATED VALUES OF THE CONDUCTION LOSSES IN THE PRIMARY-SIDE SWITCHES CALCULATED FOR A 500-W INVERTER WITH A 0.64 CONSTANT DC OFFSET IN DUTY RATIO

R_{DSON} in Ohms	Theoretical projection of conduction loss per primary switch in Watts	Simulated conduction loss per primary switch in Watts
Single 0.02Ω switch	11.493	12.67
Four 0.02 Ω switches in parallel	2.88	3.17

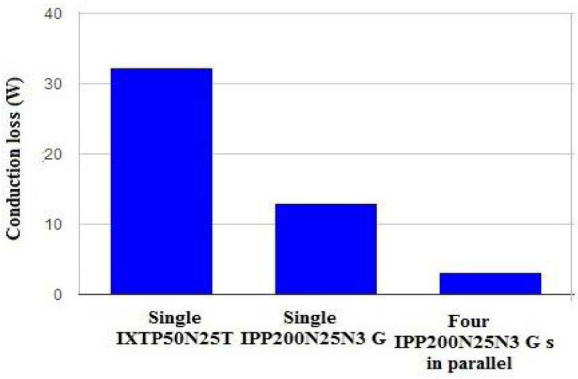


Fig. 7. Conduction loss in the primary-side switches for a 500-W load.

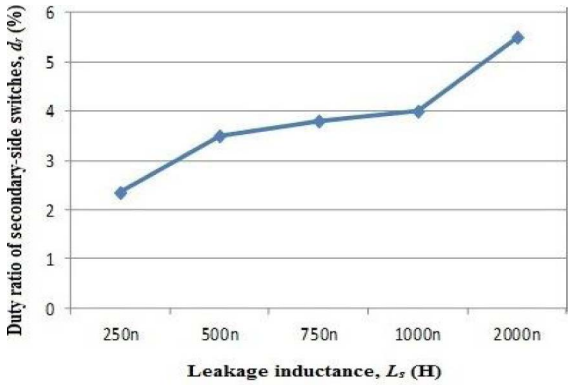


Fig. 8. Duty ratio of secondary-side switches, d_r, in percentage as a function of leakage inductance, L_S (for a 500-W load).

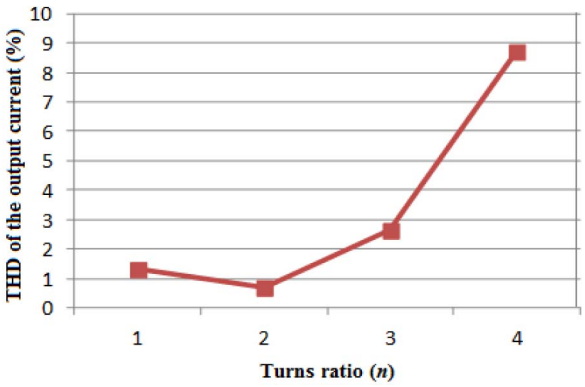


Fig. 9. THD of the output current in percentage versus transformer turns ratio, n (for a 500-W load).

where L_{s1} and L_{s2} are the leakage inductance of Module 1 and Module 2, respectively, and n is the transformers' turns ratio. The leakage inductance of the transformer must be designed to divert the current through one of the primary-side switches within the additional ZCS duty ratio (d_r) of the secondary-side switches. The lower limit of the leakage inductance is primarily influenced by the ZCS duty ratio and the load. The difference in the energies between the input inductors and the leakage inductance restricts the use of a higher value of leakage inductance. The leakage inductance of individual modules is given by the following equation:

$$L_s = \frac{V_o d_r}{n i_{\text{in1}} f_s}$$

where n is the transformer turns ratio, i_{in1} (i_{in2}) is the input current through Module 1 (Module 2), f_s is the switching frequency of the inverter, V_o is the output voltage, and d_r is the soft-switching duty ratio. From the above equation, it can be seen that the leakage inductance affects the soft-switching duty ratio (d_r) and Fig. 8 shows the leakage inductance as a function of the soft-switching range. A leakage inductance of 1 μH is chosen for the analysis of the inverter.

D. Transformer

Apart from providing a galvanic isolation to the source from the load, the transformer also affects two aspects of the inverter. The transformer's turns ratio influences the conduction losses in the switches and the total harmonic distortion (THD) of the output. A higher turns ratio in the transformer reduces the voltage across the switches on the primary side, thereby eliminating the need for higher voltage switches. This reduces the ON-state resistance of the primary-side switches, thereby bringing down the conduction losses on the primary-side, where the switches are turned ON for a longer duration when compared with those at the secondary-side. On the contrary, higher turns ratio results in higher switch current and also increased THD at the load, apart from increasing the size of the magnetics and the transformer losses. One of the major advantages of this topology is that the transformer sees a bipolar voltage and current whose average is zero, thereby reducing the size of the transformer. As the turns ratio increases, the loss in the device also increases. From Figs. 9 and 10, an optimum value of n is found to be 2. Fig. 10 shows the conduction losses in the primary-side switches as a function of transformer turns ratio.

E. Secondary-Side Switches

The secondary-side switches are operated complementarily to the primary-side switches. When the modules are operated

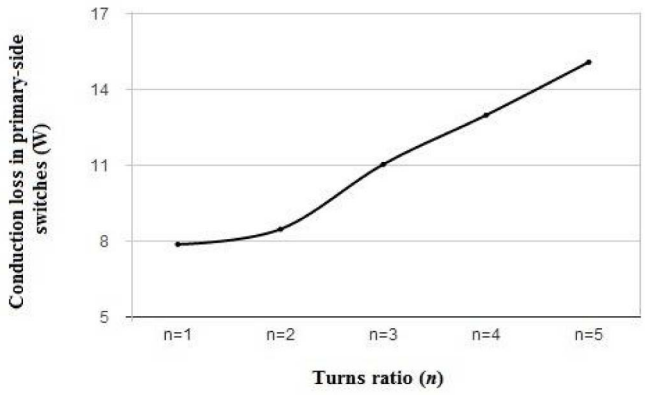


Fig. 10. Conduction losses in a single primary-side switch as a function of the transformer turns ratio for a 500-W load under soft-switching conditions. Each switch is a single chosen switch having an ON-state resistance of 0.02 Ω.

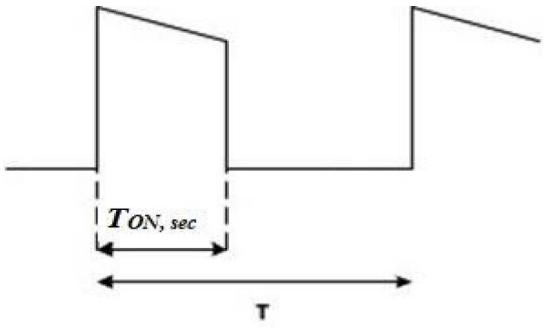


Fig. 11. Current through a secondary-side switch during a switching cycle.

as dc/dc converters, the secondary switches are only turned ON during the turn-OFF of the primary-side switches (to aid the ZCS of the primary-side switches), whereas in the inverter operation, there is considerable conduction loss in the secondary-side switches, since they are turned ON for a longer duration. Maximum voltage across the secondary-side switches is V_o. Fig. 11 shows the current through a secondary-side switch during one switching cycle under hard-switched condition. The rms current of any one of the secondary-side switches in Module 1 and Module 2 is derived as follows:

$$I_{\text{sw,rms,Secondary}} = \sqrt{\frac{1}{T_{\text{sw}}}\left[\int_0^{T_{\text{ON}}} (I_{\text{sw}})^2 dt + \int_{T_{\text{ON}}}^{T_{\text{OFF}}} (I_{\text{sw}})^2 dt\right]}.$$

Between the time interval T_{ON} to T_{OFF}, the switch current is 0. Between the time interval 0 and T_{ON}, the current through the switch is i_{LS}/n. Furthermore, $T_{\text{ON,sec}} = 1 - T_{\text{ON,pri}}$, where $T_{\text{ON,pri}}$ is the time for which any primary-side switch is turned ON and $T_{\text{ON,sec}}$ is the time for which its complimentary switch is turned ON. Solving further, the rms current through any secondary-side switch is obtained

$$i_{\text{rms,Secondary}} = \sqrt{\left(\frac{i_{\text{Ls}}}{n}\right)^2 [1 - d_1]}$$

where i_{Ls} is the current through the leakage inductance of the transformer in any module and d_1 (or d_2) is the duty ratio of the Module 1 (or Module 2). The chosen switch is STY60NM50, with an ON-state resistance of 45 mΩ and a drain–source breakdown voltage (V_{DS}) of 500 V. Table III shows the theoretical and simulated conduction losses for the secondary-side switches. Fig. 12 shows the conduction loss in all the secondary-side switches for both modules for a switch (IXFB100N50P) with an ON-state resistance of 50 mΩ, single STY60NM50 switch, and two STY60NM50 switches in parallel.

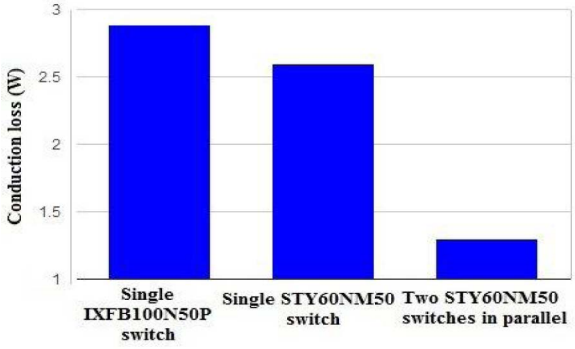


Fig. 12. Conduction loss in the secondary-side switches (for a 500-W load).

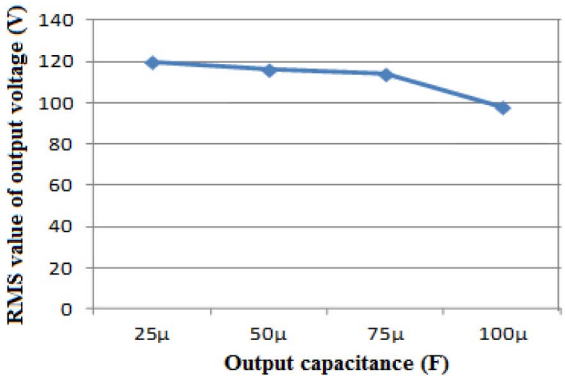


Fig. 13. Output voltage versus output capacitance of the inverter for a 500-W load.

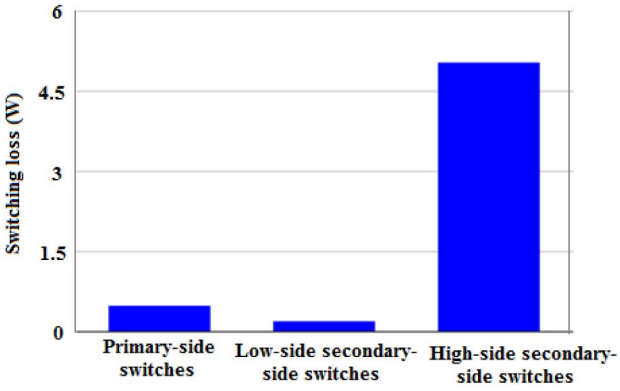


Fig. 14. Estimated switching losses for a switching frequency of 100 kHz (for a 500-W load). The chosen primary-side switch is IPP200N25N3 G and the chosen secondary-side switch is STY60NM50.

F. Output Capacitors

The voltage across the output capacitances is given by the following equations:

$$V_{\text{Co1}} = V_{\text{Co2}} = \frac{V_{o1}}{2}, \quad V_{\text{Co3}} = V_{\text{Co4}} = \frac{V_{o2}}{2}$$

TABLE III
PROJECTED CONDUCTION LOSSES IN THE SECONDARY-SIDE SWITCHES ARE CALCULATED FOR A 500-W INVERTER

R_{DSON} in Ohms	Theoretical projection of conduction loss per secondary-side switch in Watts	Simulated conduction loss per secondary-side switch in Watts
Single 0.045Ω switch	2.12	2.6
Two switches in parallel	1.06	1.3

TABLE IV
IMPEDANCES OFFERED BY DIFFERENT VALUES OF CAPACITORS, FOR VARIOUS ORDERS OF HARMONICS OF THE INVERTER FOR A 500-W LOAD

C_o in μF	X_c at n (Ω)	X_c at $3n$ (Ω)	X_c at $5n$ (Ω)	X_c at $7n$ (Ω)
10	265.2	88.4	53.1	37.9
25	106.1	35.6	21	15.2
50	53	17.7	10.6	7.6
100	26.5	8.8	5.3	3.7

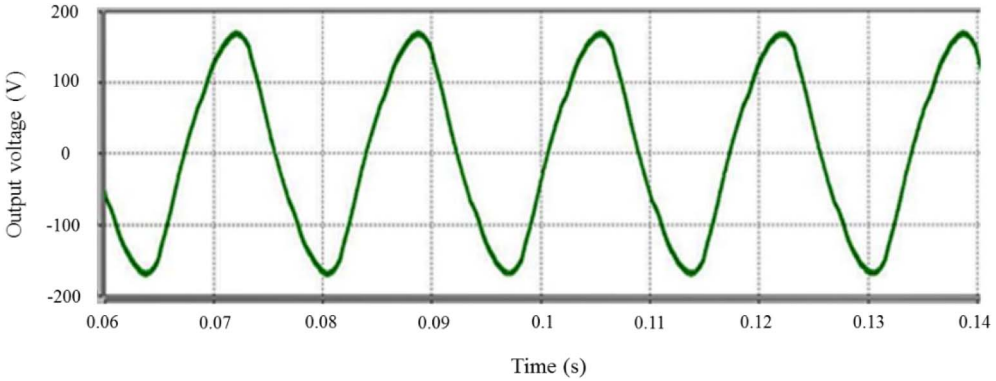


Fig. 15. Output voltage in volts (vertical axis) as a function of time in seconds (horizontal axis) for the inverter operating in open-loop condition. It shows distortion in the output voltage due to nonlinear gain of the open-loop inverter.

where V_{o1} and V_{o2} are the output voltages of the individual modules. Output capacitors are chosen to balance the THD of the load current as well as aid the control strategy by not forming a low impedance path for the high-frequency components. A larger capacitor mitigates higher order harmonics at the output. But, a very large output capacitor provides a low impedance path for the fundamental frequency component. For a 500-W load, Table IV shows the impedances offered by different values of capacitors in an open loop for various orders of harmonics. Symbol X_c represents the impedance offered by the output capacitor and n represents the fundamental frequency, 60 Hz. Fig. 13 shows the rms output voltage of the inverter as a function of the output capacitor.

G. Switching Losses

Switching losses refer to the energy losses that occur during the switching transient as the conducting semiconductor device is changed from ON-state to OFF-state or vice versa. These losses depend on the voltage across the switch during the switching transient, the current through the switch during the transient, and the time taken to move from one state to another (or the switching time). The energy associated with the turning ON of a switch is given by the following equation:

$$E_{\mathrm{ON}} = \int_0^{T_{\mathrm{ri}}+T_{\mathrm{fv}}} V_{\mathrm{DS}}(t) i_D(t) dt$$

where $V_{\mathrm{DS}}(t)$ is the instantaneous value of the drain–source voltage of the switch, $i_D(t)$ is the drain current of the switch, T_{ri} is the time taken for the current to rise from zero to i_D, and T_{fv} is the time taken for the voltage to drop from V_{DS} to zero. The energy associated with the turning OFF of a switch is given by the following equation:

$$E_{\mathrm{OFF}} = \int_0^{T_{\mathrm{rv}}+T_{\mathrm{fi}}} V_{\mathrm{DS}}(t) i_D(t) dt$$

where T_{rv} is the time taken for the voltage to rise from zero to V_{DS} and T_{fi} is the time taken for the current to drop from I_D to zero. The power loss during the switching of the devices is given by the following equation:

$$P_{\mathrm{sw}} = (E_{\mathrm{ON}} + E_{\mathrm{OFF}}) f_s$$

where f_s is the switching frequency of the inverter. Fig. 14 shows the estimated switching losses in all the primary-side switches and the secondary-side devices in both the modules.

IV. INVERTER CONTROL SCHEME

Fig. 15 shows the output voltage of the inverter under open-loop control condition. The clear distortion evident in the output voltage is reflective of the nonlinear gain of the inverter. Therefore, to reduce the THD of the load current

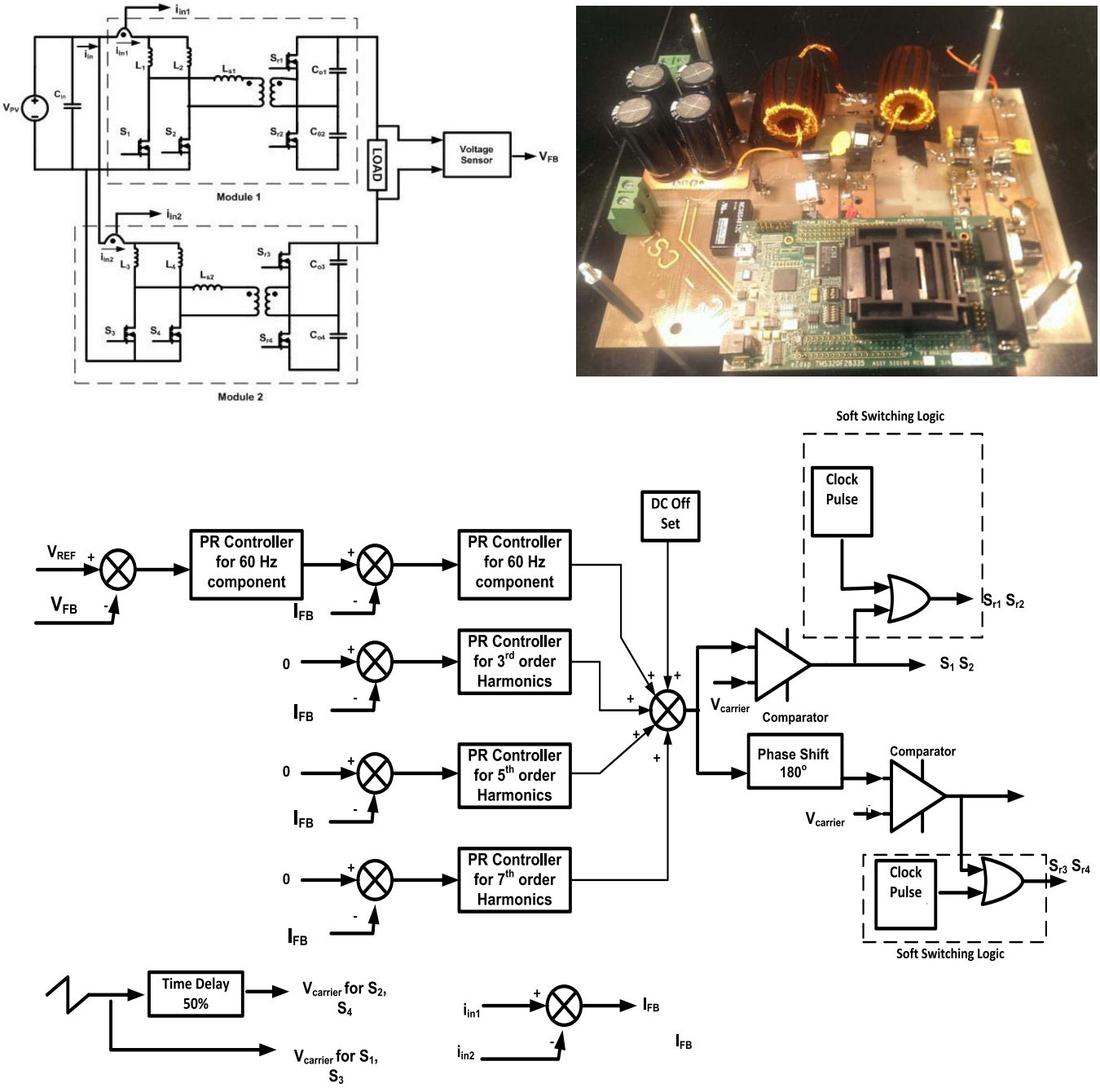


Fig. 16. Closed-loop control scheme of the differential-mode inverter. One module of an experimental inverter operated using a DSP controller, which is currently underway, is shown on the top right.

of the inverter, which has a nonlinear dc gain, a harmonic-compensation control is implemented using a proportional-resonant (PR) controller. Furthermore, the control scheme accounts for the dynamics of the primary-side inductors and the secondary-side capacitors. Essentially, and as implied in Fig. 16, a sinusoidal voltage reference yields additional harmonic components in the actual feedback. Therefore, while the fundamental current reference is extracted from the voltage loop, a zero reference is set for the higher order harmonics that have tangible impact on the output voltage. The PR controller with harmonic compensators achieves high gain at the fundamental and harmonic frequencies, thereby yielding a low steady-state error and nonsinusoidal perturbation in the duty ratio, thereby yielding a low THD output. The PR controller is represented as follows:

$$G(s) = k_p + \frac{k_o s}{[s^2 + (n^2\omega^2)]}$$

where $\omega(= 2\pi n * 60)$ represents the line or fundamental ($n = 1$) frequency and n ($= 3, 5, ..$) represents the higher order harmonics. For $n = 1$, the feedback voltage is compared with a reference 60-Hz sinusoidal voltage and the error is passed

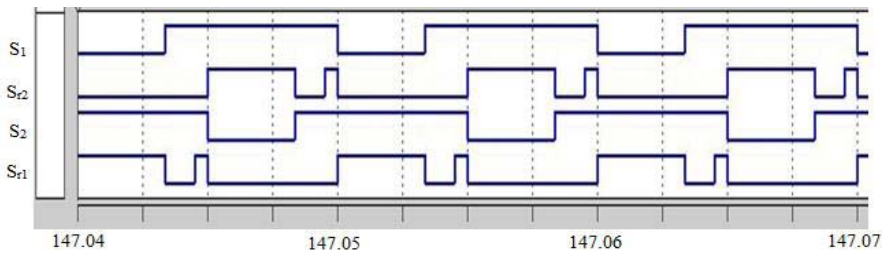


Fig. 17. Gate signals of switches S_1, S_{r2}, S_2, and S_{r1} (starting from the top) as a function of time (in milliseconds) of Module 1 under soft-switched condition.

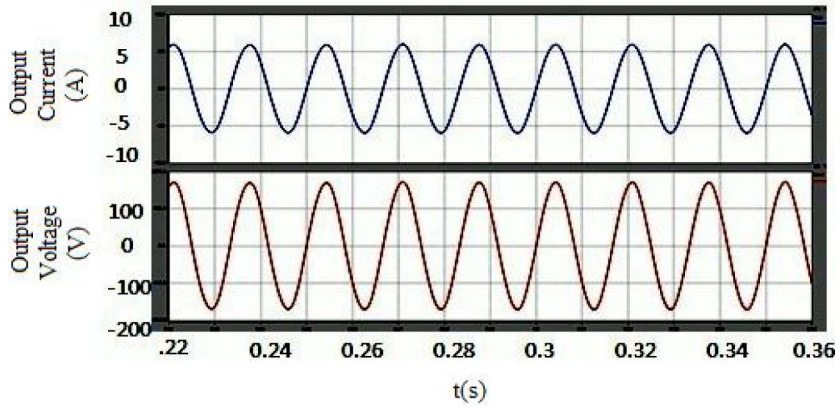


Fig. 18. Load current (top) and output voltage (bottom) of the inverter operating under closed-loop control condition.

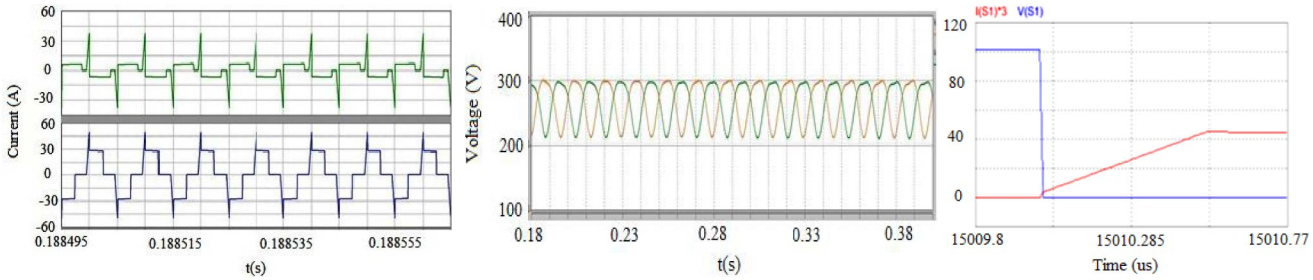


Fig. 19. Left: leakage-inductance currents of Module 1 (top trace) and Module 2 during the negative half cycle of the load voltage. Middle: output-capacitor voltages of the two inverter modules. Right: ZCS of S_1 for (waveforms are scaled for clarity).

through a PR controller, which is tuned at the line frequency. The current command of this voltage loop is compared with a differential-current feedback and passed through a PR controller with harmonic compensators achieves high gain at the fundamental and harmonic frequencies, thereby yielding a low steady-state error and nonsinusoidal perturbation in the duty ratio, thereby yielding a low THD output. The PR controller is represented as follows:

$$G(s) = k_p + \frac{k_o s}{[s^2 + (n^2\omega^2)]}$$

where $\omega(= 2\pi n * 60)$ represents the line or fundamental $(n = 1)$ frequency and n $(= 3, 5, ..)$ represents the higher order harmonics. For $n = 1$, the feedback voltage is compared with a reference 60-Hz sinusoidal voltage and the error is passed through a PR controller, which is tuned at the line frequency. The current command of this voltage loop is compared with a differential-current feedback and passed through a PR controller which is tuned at the fundamental frequency. The differential current is synthesized by taking the difference in the input currents ($i_{\text{in}1}$ and i_{n2}) of Modules 1 and 2. To mitigate the higher order (odd) harmonics (i.e., $n = 3, 5, ..$), separate control loops are implemented that emulate the structure of the fundamental frequency control loop. However, for the harmonics compensation, the current reference is set to 0 and the PR controller is tuned at a frequency that matches the harmonic frequency. The perturbation outputs of the fundamental and high-order harmonic controllers are added to a dc offset, such that the duty ratio of the (primary-side) inverter switches do not fall below 0.5. This duty-cycle signal and a 180° phase-shifted signal of the same are then used to generate the pulse trains for switches S_1 and S_2 and S_3 and S_4, respectively. The signals for secondary-side switches S_{r1} and S_{r2} are generated by

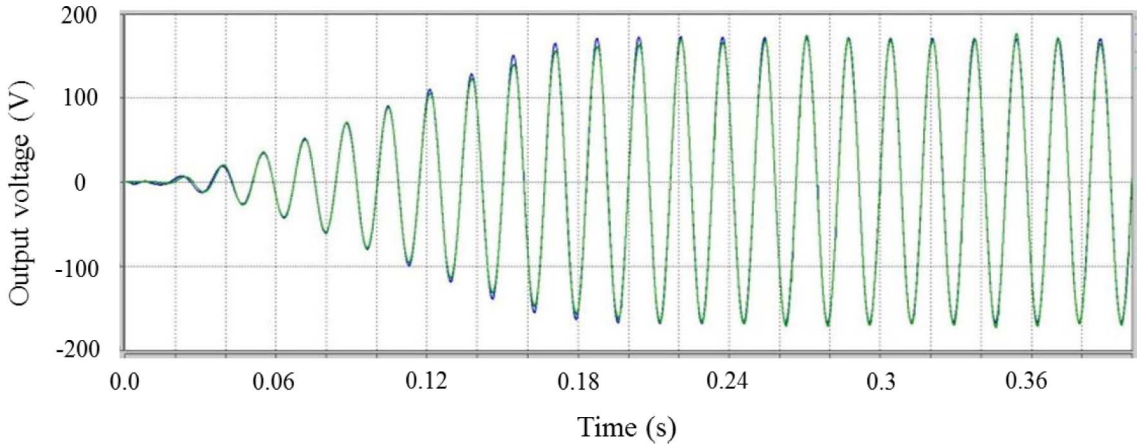


Fig. 20. Comparison of the inverter output voltage during start-up with and without proportional gain for the PR compensator. Blue trace: with proportional gain. Green trace: without proportional gain. The difference in the time to reach the steady state for the controlled inverter with and without proportional gain for the PR compensator is about two 60-Hz line cycles. It is noted that, the voltage reference is ramped up in 150 ms to the desired steady-state magnitude.

complementing the binary switching signals of primary-side switches S_1 and S_2, respectively, and then adding to the pulse train information (d_r) for achieving soft switching. The signals for secondary-side switches S_{r3} and S_{r4} are generated by complementing the binary switching signals of primary-side switches S_3 and S_4, respectively, and then adding to the pulse train information (d_r) for achieving soft switching. Fig. 17 shows the switching signals of Module 1. Fig. 18 shows the inverter output voltage and the output current using the closed-loop control scheme described above. Comparing the results of Figs. 15 and 18, it is evident that the harmonic-compensation-based closed-loop control shown in Fig. 16 addresses the harmonic distortion of the open-loop inverter effectively. For this condition, Fig. 19 shows the leakage-inductance current and output-capacitor voltages of the two modules, and ZVS turn-ON of S_1. Finally, Fig. 20 shows the acceptable dynamic response of the inverter during start-up. The presence of the proportional gain of the PR compensator yields better transient response at the cost of slightly higher distortion.

V. Conclusion

This paper describes a current-source high-frequency-link inverter. It comprises two dc/dc isolated converters that are connected in a differential-mode configuration, thereby yielding an inverter output. The inverter has several key features including the following: 1) single-stage topology; 2) high-frequency instead of bulky line transformer; 3) inherent voltage boost/gain capability; 4) voltage-doubling secondary reduces transformer turns ratio to half; 5) reduced transformer core size due to bipolar flux at the origin; and 6) soft switching of most of the inverter switches. However, the inherent nonlinearity of the inverter yields harmonic distortion under open-loop condition. To mitigate that problem, a harmonic-compensation-based control scheme is outlined. The resultant closed-loop-controlled inverter significantly reduces the harmonic distortion of the inverter output voltage and current and yields acceptable dynamic response. Finally, work in underway currently to synthesize an experimental inverter. A preliminary prototype module is shown in Fig. 16. The following are the projected performance parameters for such an inverter at 500-W output: 1) efficiency of 94% (device conduction and switching losses of 2%, transformer losses: 2%, filter losses: 1.5%, and additional losses: 0.5%); 2) output voltage THD of ∼2%; and 3) dynamic time lag between reference and feedback voltage using proportional-gain-based PR compensator of up to one 60-Hz line cycle. An adaptive tracking controller as outlined in [22] for a differential-mode inverter will also be pursued to reduce the time lag.

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