A Fault-Tolerant Switching Scheme for an Isolated DC/AC Matrix Converter

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***Abstract*—A fault-tolerant scheme is proposed for a multistage isolated three-phase dc/ac matrix inverter (MI-TMI). It comprises a front-end dc/ac converter followed by an ac/pulsating-dc converter and a pulsating-dc/ac converter. The fault-tolerant scheme (FTS) ensures a consistent operation under different fault conditions in any of the three stages of the TMI mentioned previously. A fault-diagnosis scheme is outlined which identifies the source of the converter fault and the impact of when the fault onsets on the inverter is explored. Finally, detailed results on the fault-tolerant switching scheme as well as experimental validation using a fabricated MI-TMI prototype are presented.**

***Index Terms*—Capacitor-less dc link, fault diagnosis, fault tolerant, matrix converter, modulation, renewable/alternative energy, three phase.**

I. Introduction

MULTISTAGE isolated three-phase dc/ac matrix inverter (MI-TMI) topology [1]–[12] features dc-link-capacitor-less solution, higher power density, and modular design yielding a superior solution to several conventional inverter approaches for renewable energy systems. While there have been some recent publications in this area from the standpoints of power-stage and control performances, such analyses are often based on the nominal operation of the MI-TMIs and limited in scope with regard to the alleviation of postfault dynamics and on fault-tolerant operation and continuity of the service [6]–[13]. At high power or for mission-critical or cost-sensitive applications, where the operational continuity of the inverter is vitally important, reliability of the MI-TMI attains significant importance. As such, the need for fault-tolerant operation, which has become almost a mandatory requirement in power converters for military and aeronautical applications, is gaining traction for commercial applications as well.

In [14], a fault-tolerant-converter topology is outlined for grid-connected wind-energy-conversion system, which is based on a redundant fourth leg. [15] also relies on a redundant fourth leg to replace the faulty leg of a voltage-source inverter (VSI) used as a permanent-magnet drive. [16] presents a fault-tolerant powertrain topology for series hybrid electric vehicles (SHEV) by introduction of a redundant phase-leg that is shared between three converters in a standard SHEV powertrain. [17] proposes a fault-tolerant permanent magnet traction module which is based on sharing of a common leg of one of the two VSIs feeding two permanent magnet synchronous machines (PMSMs). However, the reliability of the whole system is still degraded by the bulky electrolytic capacitors used in the dc-link. [18] presents a model-reference adaptive system-based fault diagnosis algorithm for a VSI used as a PMSM drive system. [19] also proposes a fault-detection method for an open-switch fault in the switches of grid-connected neutral-point clamped inverter systems. Both of these only consider open-circuit faults in power switches. Also, in spite of the development of acceptable and promising fault diagnosis algorithms, no solution is offered for the continuity of service in case of a fault. This study provides a mechanism for fault-tolerance of a pulsating-dc-link MI-TMI (i.e., an inverter operating without a dc-link capacitor) without using redundant switches for all of the stages. Instead, depending on the stage in which fault happens, it either takes advantage of the encoded phase information in the resultant pulsating-dc-link waveform of the MI-TMI or incorporates the switches in other stages (leading to less number of redundant switches) to restore the output voltages. The reliability of the proposed method ensures continuity of service under various fault scenarios in different stages of the MI-TMI. Also, a simple fault diagnosis algorithm is proposed based on the signature of the distortion in the output line voltages which enables early detection of faulty switches/legs in less than a few switching cycles. Moreover, the reliability of the system is further increased by removing the need to a bulky electrolytic capacitor in the dc-link [5]. The MI-TMI, as shown in Fig. 1, comprises a front-end dc/ac converter, followed by an ac/pulsating-dc converter and a pulsating-dc/ac converter. Switches S_{xx} are low-frequency and low-cost devices (back-to-back thyristors) for reconfiguration of the topology in case of a fault. The FTS, as outlined in this study, includes the following steps. First, the faulty stage and switching devices are identified using a fault-diagnosis algorithm. Next, depending on the faulty stage, relevant restoration algorithm is employed to sustain the output voltages of the MI-TMI as follows:

1) If the fault happens in the dc/ac converter, faulty circuit is isolated and also based on the type of the lost phase, the pulse-width-modulation (PWM) reference for the remaining phases in the dc/ac converter is changed so as to restore the output line voltages.
2) If the fault happens in the ac/pulsating-dc converter, the faulty leg and the corresponding full bridge in the dc/ac converter are isolated and the PWM reference for the remaining phases in the dc/ac converter and the

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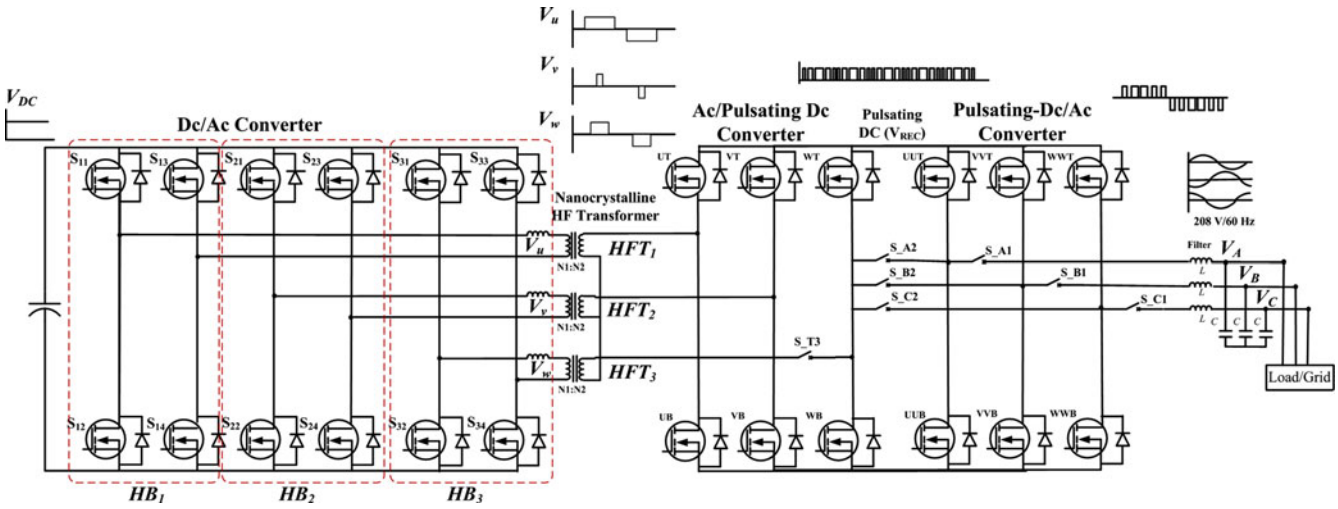


Fig. 1. M I-TMI with fault-tolerant front-end dc/ac converter and low-cost and low-frequency transition switches in the secondary for fault tolerance.

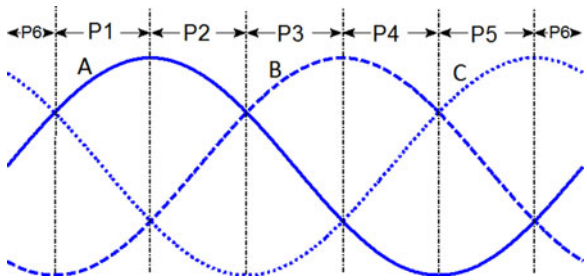


Fig. 2. Illustration of the sectors P1 to P6.

ac/pulsating-dc converter is changed so as to restore the output line voltages.

3) If the fault happens in the pulsating-dc/ac converter, the faulty leg is isolated from load through S_{A1}, S_{B1} or S_{C1}, dc/ac converter and ac/pulsating-dc converters will operate with two full bridges and two legs, respectively, provided that the PWM references for them are changed, and the third leg of ac/pulsating-dc substitutes the faulty leg of pulsating-dc/ac converter.

Section II describes the MI-TMI topology and its fault-free operating principle. Section III provides analysis of different fault scenarios and their effects on the inverter output. Based on the results of this analysis, relevant fault-diagnosis algorithms are then discussed. Subsequently, the restoration from a fault and detailed explanations about the proposed algorithms are provided in Section IV. Effectiveness of the proposed FTS is experimentally verified in Section V using a 1-kW laboratory MI-TMI prototype. Finally, in Section VI, some relevant conclusions are drawn.

II. Fault-Free Operation of the MI-TMI

Fig. 1 demonstrates the topology of the MI-TMI. The front-end dc/ac converter comprises three full-bridge converters generating bipolar and tristate HF voltage pulses, which are fed to the HF transformers. The secondary outputs of these HF transformers are then fed to the ac/pulsating-dc converter, which rectifies the bipolar voltage pulses and creates the resultant pulsating-dc voltage (V_{REC}). Using this pulsating-dc voltage and a specific modulation scheme [5], the pulsating-dc/ac converter generates the desired sinusoidal inverter outputs.

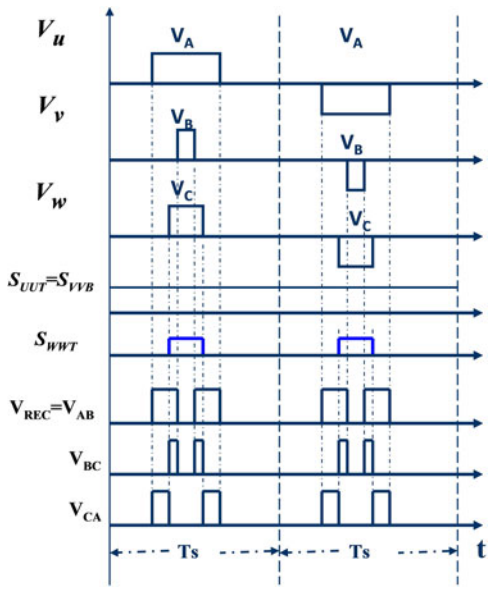


Fig. 3. Illustrating a fault-free operation of the MI-TMI in sector P1.

For the fault-free operation [5], first, the overall 360° period of a line cycle is divided into six sectors marked in Fig. 2 as P1 through P6. In a given switching cycle, three sets of instantaneous bipolar and tristate HF pulses representing three phases are generated using the front-end dc/ac converter (see Fig. 3). These pulse trains are fed to the ac/pulsating-dc converter which generates a unipolar HF pulse-train voltage (V_{REC}). It is noted that the gate pulses for each of the legs in the ac/pulsating-dc converter are synchronized with those of the full-bridge converters in dc/ac converter generating the same phase. Signal VREC contains information of the maximum line voltage at any instant which is encoded in the area under the pulse voltages. As

TABLE I
PWM REFERENCES FOR PULSATING-DC/AC CONVERTER

	Sector					
Signal	P1	P2	P3	p4	P5	P6
UUT	1	1	AC	0	0	AB
VVT	0	BC	1	1	BA	0
WWT	CB	0	0	CA	1	1

Symbols AB, BC, and CA are PWM references for line voltages.

such, there is no need for HF switching of those two legs in the pulsating-dc/ac converter generating the maximum line voltage in each sector P1–P6. We explain the generation of V_{REC} using an illustration. Suppose, the voltage reference vector is in sector P1, then, as per the fault-free switching algorithm, three instantaneous bipolar pulse sequences representing V_{A}, V_{B}, and V_{C} are generated. The ac/pulsating-dc converter output (V_{REC}) is defined by the following equation:

$$V_{\mathrm{REC}} = \max\left(N_2/N_1\left(\left|V_u - V_v\right|, \left|V_v - V_w\right|, \left|V_w - V_u\right|\right)\right). \tag{1}$$

Since in the sector P1, VA and VB are the highest and the lowest phases, respectively, based on (1), V_{REC} contains the information of V_{A}-V_{B} = $\mathrm{V_{AB}}$, which is encoded in the area under the voltage pulses in every switching period. This is illustrated in Fig. 3 with a switching period of T_{s}. Therefore, switch UUT is permanently ON and switch VVT is permanently OFF to pass the rectified pulses representing V_{AB}. The other line voltages are generated by HF switching of the third leg. So, the PWM reference of line CB is used for switching WWT. Therefore, and as shown in Fig. 3, V_{REC} is chopped so as to generate V_{BC} and V_{CA}. Table I shows the PWM references for the pulsating-dc/ac-converter switches for sectors P1 to P6. In Table I, AB, BC, and CA represent PWM references for the respective phase-to-phase voltages. This switching scheme leads to 67% improvement of the efficiency compared with the conventional VSI. The details of this scheme, referred to as hybrid modulation, are provided in [5] and [20].

III. POSSIBLE FAULT TYPES AND FAULT DIAGNOSIS

In the previous section, we considered normal (fault-free) mode of operation of the MI-TMI of Fig. 1. In this section, possible fault scenarios are outlined and it will be shown that since each type of fault generates a specific distortion pattern in the output line voltages, a comprehensive fault diagnosis can be developed.

A. Failure in the DC/AC Converter

The term phase loss in this study is typically used for any kind of failure in full bridge switching devices that disrupts the generation of bipolar HF pulses trains or distorts the output line voltages. Table II illustrates different types of device failure (leading to a short circuit between drain and source of the MOSFETs which is a very common type of failure) and the resultant distorted full-bridge output. Failures listed in the left column lead to a flux imbalance in the HF transformers though encoding the phase information. Failures in the right column, however, interrupt the process of encoding the phase data. No matter what type of fault happens, protection circuits such as $\mathrm{V_{DS,Sat}}$ monitoring (which are industrial standard and not discussed in this study) isolate faulty circuit from the whole converter topology thanks to the modular design of this MI-TMI. Yet, the output voltages of the inverter have to be restored using the remaining full bridges.

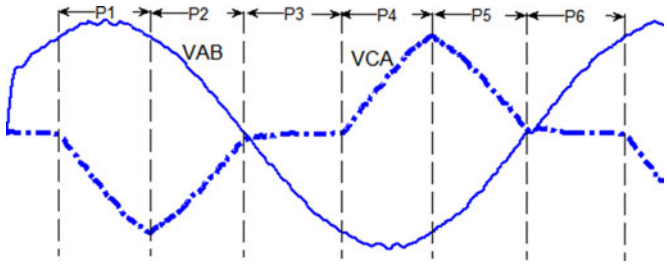
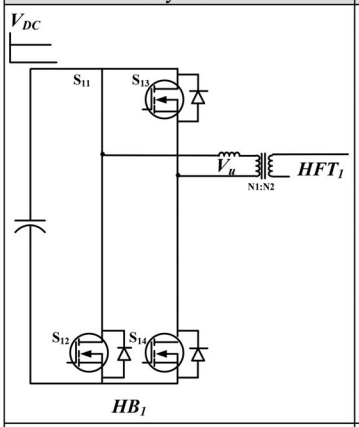
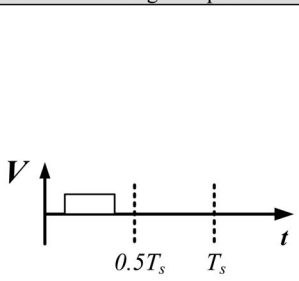
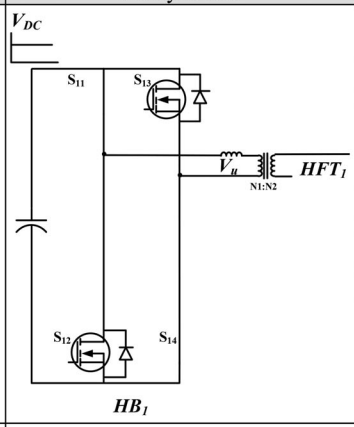
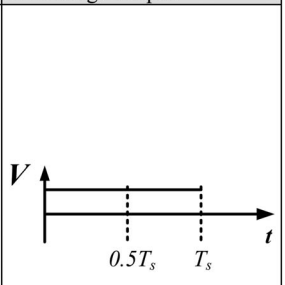
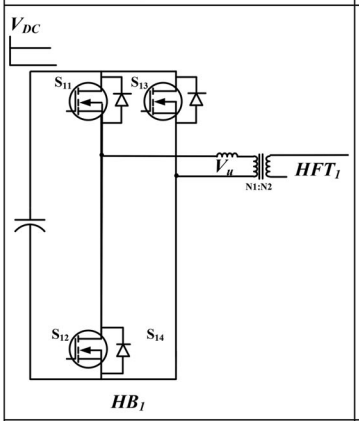
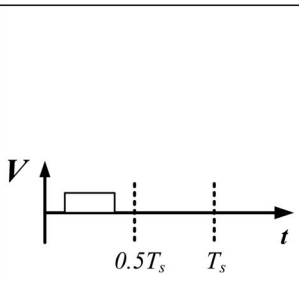
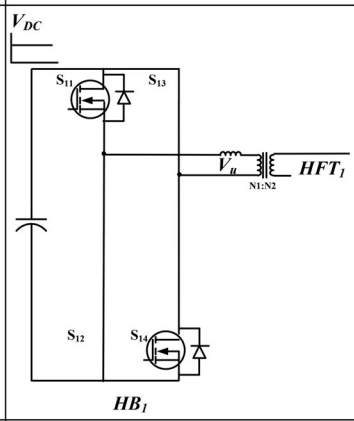
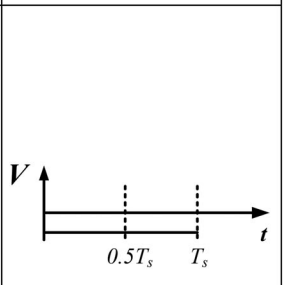
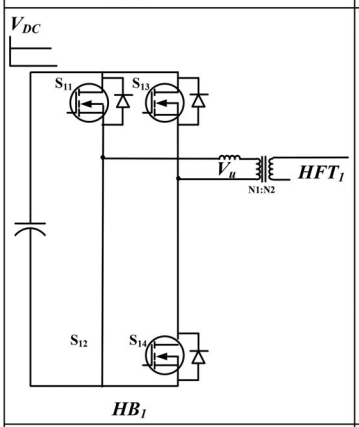
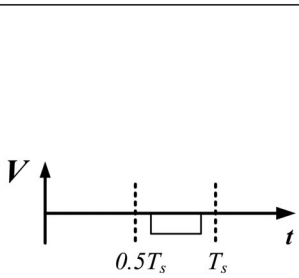
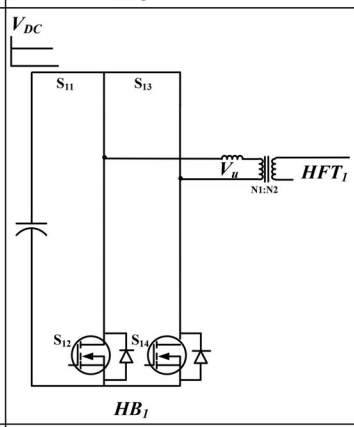
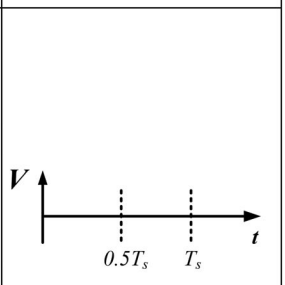
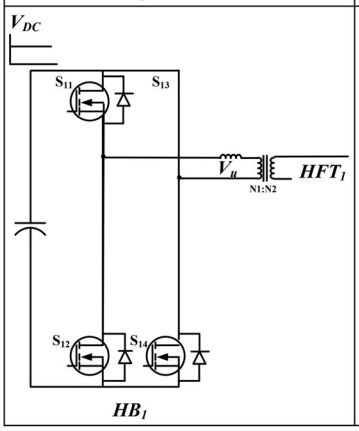
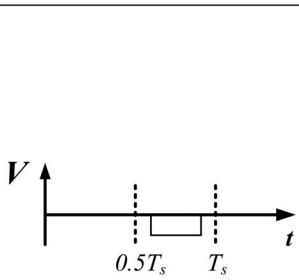
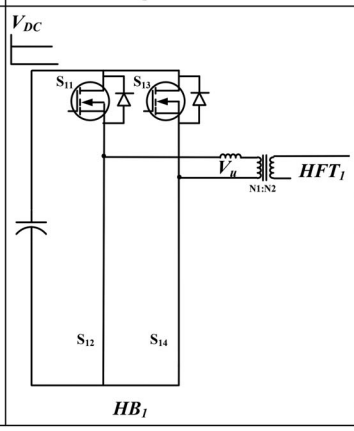
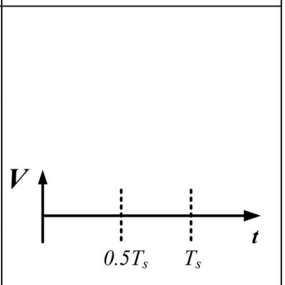


Fig. 4. Effect of a single-phase outage (phase w) on the output line-voltages V_{AB} (top), V_{CA} (middle), and V_{REC} (bottom) of the MI-TMI in Fig. 1 using experimental investigation. Failure of phase w causes a more severe distortion in V_{CA} rather than in V_{AB}. Note that V_{CA} is not distorted in P1 and P4.

1) Loss of One Phase of the DC/AC Converter: Consider the scenario in which one full-bridge converter of the dc/ac converter fails. For instance, if phase w fails and the other two full-bridge converters continue to generate V_u and V_v, the output line voltages of the MI-TMI will be distorted. The obvious reason is that, due to the failure of $\mathrm{HFT_3}$ output and based on (1), the information of phase C is no longer available in V_{REC}. Fig. 4 shows such a distortion in line voltages V_{AB} and V_{CA}. Note that the distortion in V_{CA} is worse than V_{AB}. This is because for generating V_{AB}, the pulsating-dc/ac converter does not require the encoded information of phase C in V_{REC} no matter such information exist (fault-free operation) or not (faulty operation). However, this is not the case for V_{BC} and V_{CA}. Note that the only sectors in which V_{CA} is not distorted despite lack of information of phase C are P1 and P4; in these two sectors, phase C is the intermediate phase. This implies that in P1 and P4 [following (1)] information of phase C is not encoded in V_{REC} by ac/pulsating-dc converter even under fault-free operating conditions (generally, information of the intermediate phase in each sector is not encoded in V_{REC}). Therefore, the effect of failure of V_w does not appear in these sectors and therefore no distortion in V_{CA} is observed in P1 and P4 (see Fig. 4). Under this fault condition, the only way to restore the output line-voltages of the MI-TMI is to change the PWM references of the remaining full-bridge converters so as to encode the information of the lost phase in V_{REC} [6], [20]. In case of a failure of two full-bridge converters in the dc/ac converter, a proper change of the PWM reference for the remaining full-bridge converter can also restore the output voltages though with a lower voltage level.

Based on the case illustration stated, the lost phase in the dc/ac converter can be diagnosed based on the sector in which fault

TABLE II
POSSIBLE TYPES OF FAULT IN FULL BRIDGE OF THE DC/AC CONVERTER

Faulty circuit	Full Bridge Output	Faulty circuit	Full Bridge Output
			
			
			
			

Ts: Switching period.

TABLE III
POSSIBLE TYPES OF FAULT IN FULL BRIDGE OF THE DC/AC CONVERTER

Sector Failed Phase	P1	P2	P3	P4	P5	P6
Phase u $\{S1x \mid x = 1,\ldots,4\}$	Distortion in V_{AB}, V_{CA}	Distortion in V_{AB}, V_{CA}	No Distortion	Distortion in V_{AB}, V_{CA}	Distortion in V_{AB}, V_{CA}	No Distortion
Phase v $\{S2x \mid x = 1,\ldots,4\}$	Distortion in V_{AB}, V_{BC}	No Distortion	Distortion in V_{AB}, V_{BC}	Distortion in V_{AB}, V_{BC}	No Distortion	Distortion in V_{AB}, V_{BC}
Phase w $\{S3x \mid x = 1,\ldots,4\}$	No Distortion	Distortion in V_{CA}, V_{BC}	Distortion in V_{CA}, V_{BC}	No Distortion	Distortion in V_{CA}, V_{BC}	Distortion in V_{CA}, V_{BC}

Ts: Switching period.

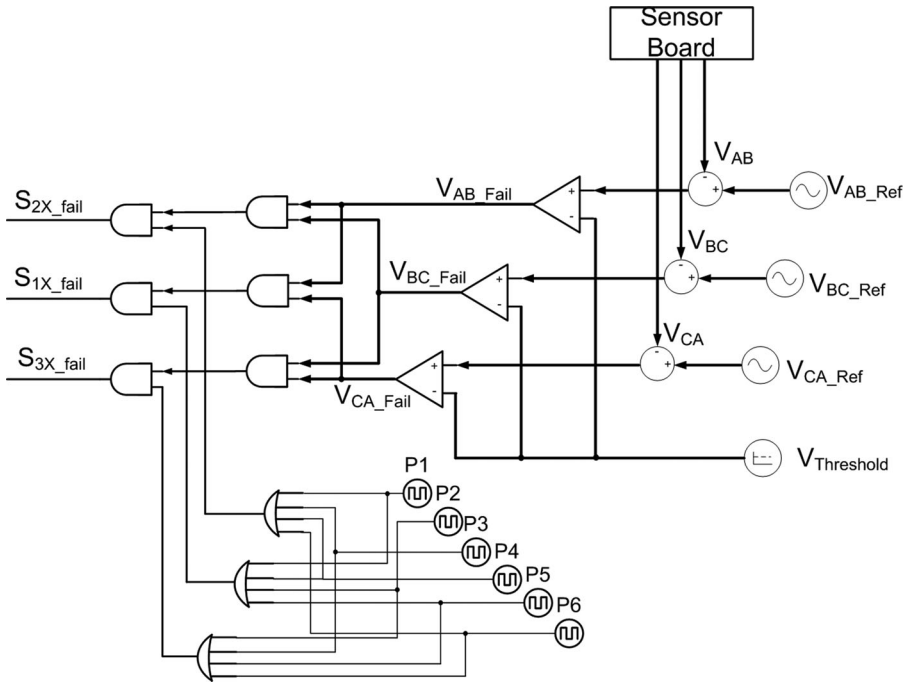


Fig. 5. Proposed fault diagnosis algorithm for transition from three to two active full-bridge converters.

happens and the type of distorted output line voltages ($V_{\rm AB}$, $V_{\rm BC}$, and $V_{\rm CA}$). For instance, if the magnitude of the two line voltages $V_{\rm AB}$ and $V_{\rm CA}$ suddenly fall below the reference values (dictated by load in standalone operation mode and the utility grid in grid connected mode) in any of the two sectors P1 or P2, it is an indication for failure of phase u.

In general, assume that the MI-TMI in Fig. 1 is operating under fault-free condition. Then, after a few cycles, two of the line voltages abruptly get distorted. The phase which is common between the two line voltages is the lost phase in the primary-side dc/ac converter provided that these distortions happen in the sectors in which this common phase has either the maximum or the minimum magnitude. Table III shows distortion patterns associated with failure of each of the three phases. These distortion patterns are used to diagnose the lost phase in dc/ac converter and ac/pulsating-dc converter.

Fig. 5 shows an illustration of the fault diagnosis algorithm in case of a failure of one full-bridge converter in the dc/ac converter based on the aforementioned explanations. Symbols P1 to P6 represent the six sectors as shown in Fig. 2. Symbols $V_{\rm AB\_Ref}$, $V_{\rm BC\_Ref}$, and $V_{\rm CA\_Ref}$ represent the reference values for the three phase line voltages while $V_{\rm AB}$, $V_{\rm BC}$, and $V_{\rm CA}$ are the sensed values for the same. $S_{1X\_\rm fail}$, $S_{2X\_\rm fail}$, and $S_{3X\_\rm fail}$ are flags, each indicating a failure of a full-bridge converter in dc/ac converter. For instance, $S_{1X\_\rm fail}$ indicates the loss of $\rm S_{11}$, $\rm S_{12}$, $\rm S_{13}$, and $\rm S_{14}$. As an illustrative example of this scheme, if in any of the sectors P1, P2, P4, or P5, the differences of $V_{\rm AB}$ and $V_{\rm CA}$ with their references are higher than a threshold, $S_{1X\_\rm fail}$ is set.

2) Loss of Two Phases of the DC/AC Converter: Fig. 5 also captures the fault-diagnosis scheme in case of transition from three to one active full-bridge converter in the dc/ac converter. It is based on the fact that in such a fault (failure of two full-bridge converters in the dc/ac converter), $V_{\rm REC}$ will become almost zero. Consequently, all of the output line voltages cease to zero as soon as the output filter capacitors get discharged. Fig. 6 shows a case illustration in which HB1 fails at 32.7 ms. Fig. 6(a) shows that at $t = 32.7$ ms, $V_{\rm AB\_error} = V_{\rm AB\_Ref} - V_{\rm AB}$

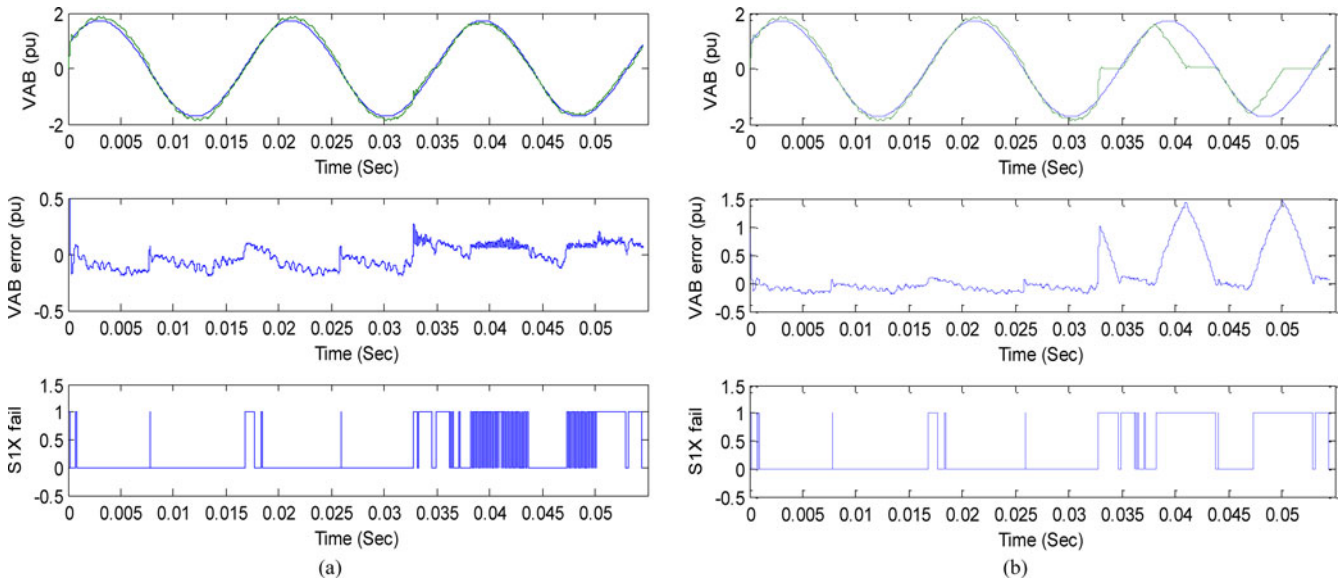


Fig. 6. (a) Top: $V_{\mathrm{AB\_Ref}}$ (in blue) and V_{AB} (in green) both normalized to phase voltage; middle: error signal ($V_{\mathrm{AB\_Ref}} - V_{\mathrm{AB}}$), and bottom: $\mathrm{S_{1x}\_fail}$. At $\mathrm{t} = 32.7$ ms, one of the bridges in the DC/AC converter corresponding to phase u fails and fault diagnosis logic in Fig. 6(a) activates $\mathrm{S}_{1x}\_\mathrm{fail}$. Note that the fault is removed in less than 1 ms. (b) Same scenario is repeated with the exception that the fault is detected (see the jump in the error signal in the middle trace) but the fault is not restored intentionally in order to show the effect of full- bridge-converter loss on V_{AB}.

TABLE IV
INFORMATION ENCODED IN V_{REC} FOR EACH OF THE SIX SECTORS P1–P6

Sector Signal	P1	P2	P3	P4	P5	P6
V_{REC}	Vuv	Vuw	Vvw	Vvu	Vwu	Vwv

exceeds a threshold set in the fault diagnosis program (5%) and S_{1X_fail} is activated. It is shown that in less than 1 ms FTC can restore the output line voltage V_{AB}. Same scenario is repeated in Fig. 6(b) in which FTC is not activated intentionally in order to show the effect of HB1 loss on V_{AB}.

B. Failure in the AC/Pulsating-DC Converter

If a switching device in a leg of ac/pulsating-dc converter fails, the distortion in the output line voltages is exactly similar to what happens if the corresponding full bridge (for the same phase) in the dc/ac converter fails. As such, the fault diagnosis algorithm of Fig. 5 disables gate pulses to the MOSFETs of the leg associated with the diagnosed faulty phase in the ac/pulsating-dc as well. For instance, if the fault diagnosis algorithm tracks a failure in phase u, gate pulses to UT and UB in the ac/pulsating-dc converter will be disabled upon diagnosis and PWM references for HB2 and HB3 will be changed as will be explained in Section IV.

C. Failure in the Pulsating-DC/AC Converter

In order to facilitate our analysis, the content of V_{REC} at different sectors P_1 to P_6 is provided in Table IV at first. For instance, it shows that in sector P1, the pulse area of V_{REC} at every switching period is equivalent to V_{uv}. The effect of a MOSFET failure in dc/ac converter on the output line voltages is analyzed through a case illustration in order to develop the fault diagnosis concept for such failures. Consider that while the MI-TMI of Fig. 1 is in fault-free operation, suddenly UUT fails (a short circuit between two of the three MOSFET terminals [21]). As a typical example, the effect of a short-circuit failure between drain and source terminals of MOSFETs on V_{REC} as well as on the output line voltages of the MI-TMI is shown in Fig. 7. This fault occurs at $t = 2$ ms which falls in sector P_1. It is shown that before sector P_3, no distortion appears in the output line voltages. The reason is as Table IV shows, in sectors P_1 and P_2, the information of line voltages V_{uv} and V_{uw} is encoded in V_{REC} and as shown previously in Table I, UUT is supposed to remain on in these sectors. However, it is observed that in P_3 since VVT turns on (according to hybrid modulation algorithm, Table V), V_{AB} is zero and $V_{\mathrm{BC}} = -V_{\mathrm{CA}}$. Note that in P_6, V_{CA} is zero and $V_{\mathrm{AB}} = -V_{\mathrm{BC}}$. In P_3 and P_6, there are voltage spikes in V_{REC} due to the fact that in these two sectors UUB starts HF switching while UUT is shorted due to the fault.

By generalizing this analysis to other switching devices, a fault-diagnosis algorithm for pulsating-dc/ac converter can be developed as captured in Table V. Having analyzed all types of faults in three stages of the MI-TMI and proposed relevant fault diagnosis algorithms, next section illustrates the fault-tolerant switching scheme (FTSS) for this topology in details.

IV. FTSS FOR THE MI-TMI

Using the backdrop of the fault-free switching scheme, as explained in Section II, and possible fault scenarios and diagnosis algorithms in Section III, we now describe the FTSS for potential switching device failure in all of the three stages. For dc/ac converter, the proposed FTSS restores three phase output line

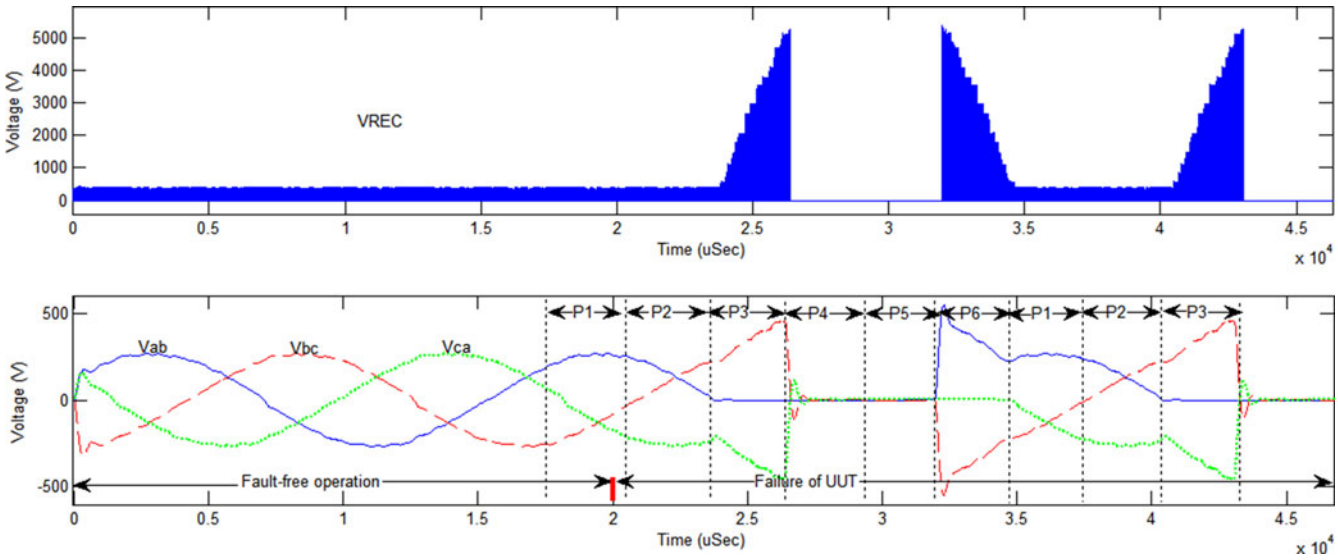


Fig. 7. Effect of UUT failure on V_{REC} and output line voltages of the MI-TMI of Fig. 1.

TABLE V
FAULT AND DISTORTION PATTERNS FOR THE PULSATING-DC/AC CONVERTER

Sector Failed MOSFET	P1	P2	P3	P4	P5	P6
UUT	No Distortion	No Distortion	$V_{AB}=0$ $V_{BC}=-V_{CA}$	No Distortion	No Distortion	$V_{CA}=0$ $V_{AB}=-V_{BC}$
UUB	No Distortion	No Distortion	$V_{CA}=0$ $V_{AB}=-V_{BC}$	No Distortion	No Distortion	$V_{AB}=0$ $V_{BC}=-V_{CA}$
VVT	No Distortion	$V_{AB}=0$ $V_{BC}=-V_{CA}$	No Distortion	No Distortion	$V_{BC}=0$ $V_{AB}=-V_{CA}$	No Distortion
VVB	No Distortion	$V_{BC}=0$ $V_{AB}=-V_{CA}$	No Distortion	No Distortion	$V_{AB}=0$ $V_{BC}=-V_{CA}$	No Distortion
WWT	$V_{CA}=0$ $V_{AB}=-V_{BC}$	No Distortion	No Distortion	$V_{BC}=0$ $V_{AB}=-V_{CA}$	No Distortion	No Distortion
WWB	$V_{BC}=0$ $V_{AB}=-V_{CA}$	No Distortion	No Distortion	$V_{CA}=0$ $V_{AB}=-V_{BC}$	No Distortion	No Distortion

voltages when one or even two phases of the dc/ac converter are lost. In essence, the fault-tolerant operation of the dc/ac converter ensures the synthesis of the same encoded pulsating-dc voltage (obtained during the fault-free operation) when one or even two phases of the dc/ac converter are lost. In order to give an analytical insight into the FTSS, at first we consider the equations for the output line-voltages of the MI-TMI under fault-free operation condition. For the MI-TMI of Fig. 1, the following sets of equations are valid for the output line voltages:

$$V_{\mathrm{AB}} = (S_{\mathrm{UUT}} - S_{\mathrm{VVT}}) \times V_{\mathrm{REC}} \tag{2}$$

$$V_{\mathrm{BC}} = (S_{\mathrm{VVT}} - S_{\mathrm{WWT}}) \times V_{\mathrm{REC}} \tag{3}$$

$$V_{\mathrm{CA}} = (S_{\mathrm{WWT}} - S_{\mathrm{UUT}}) \times V_{\mathrm{REC}} \tag{4}$$

in which S_{UUT}, S_{VVT}, and S_{WWT} are the switching functions of the pulsating-dc/ac converter. However, we know that

$$V_{\mathrm{REC}} = \frac{N_2}{N_1} \times V_{\mathrm{DC}} \times \begin{pmatrix} \mathrm{MAX}\left\{|\mathrm{S}_{11}-\mathrm{S}_{21}|, |\mathrm{S}_{11}-\mathrm{S}_{31}|, |\mathrm{S}_{21}-\mathrm{S}_{31}|\right\} \\ +\ \mathrm{MAX}\left\{|\mathrm{S}_{13}-\mathrm{S}_{23}|, |\mathrm{S}_{13}-\mathrm{S}_{33}|, |\mathrm{S}_{23}-\mathrm{S}_{33}|\right\} \end{pmatrix} \tag{5}$$

where S_{ij} $(i,j=1,2,3)$ is the switching functions of the dc/ac converter, V_{DC} is the input dc voltage, and N_1 and N_2 are the primary and the secondary turns ratio of the HF transformers, respectively. As mentioned earlier, if any one of the three full-bridge converters of dc/ac converter fails, the encoded information of the relevant phase in V_{REC} is lost. For instance, if the full-bridge converter consisting of S_{31}, S_{32}, S_{33}, and S_{34} fails, the information of phase C will no longer be encoded in V_{REC} in sectors P2, P3, P5, and P6. Consequently, V_{REC} will be expressed as follows:

$$V_{\mathrm{REC}} = \frac{N_2}{N_1} \times V_{\mathrm{DC}} \times \left(|S_{11}-S_{21}| + |S_{13}-S_{23}|\right). \tag{6}$$

This in turn leads to a severe distortion in V_{BC} and V_{CA} and a slightly more moderate distortion in V_{AB}. Fig. 4 shows the effect of loss of the full-bridge converter generating the information

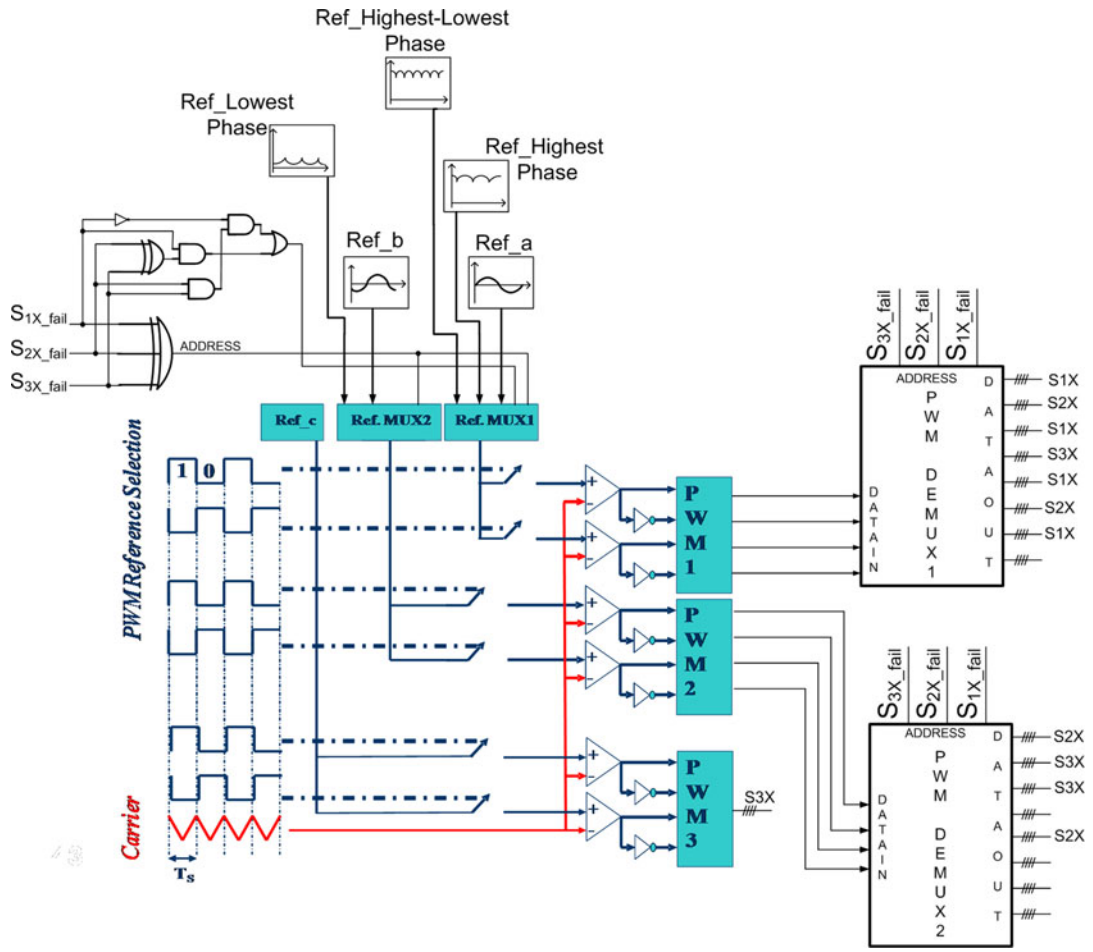


Fig. 8. PWM technique to retain the nominal operation in case of a single phase or a double-phase outage. If, for instance, phase w is lost, one of the remained full-bridge converters of the dc/ac converter generates a bipolar pulse train containing the information of the highest phase in every sector from P1–P6 while the other one does the same for the lowest phase.

of phase C on $V_{\rm AB}$ and $V_{\rm CA}$ (Note that a generalized analysis of loss of phases u, v, and w are given in Table III in context of the fault diagnosis). So, in order to restore the information of the lost phase, PWM references for the remaining full-bridge converters should be modified. In the subsequent sections, it will be shown that this PWM reference modification is required for output line voltage restoration no matter in which stage a failure is occurred. The following sections discuss these modifications under different fault scenarios.

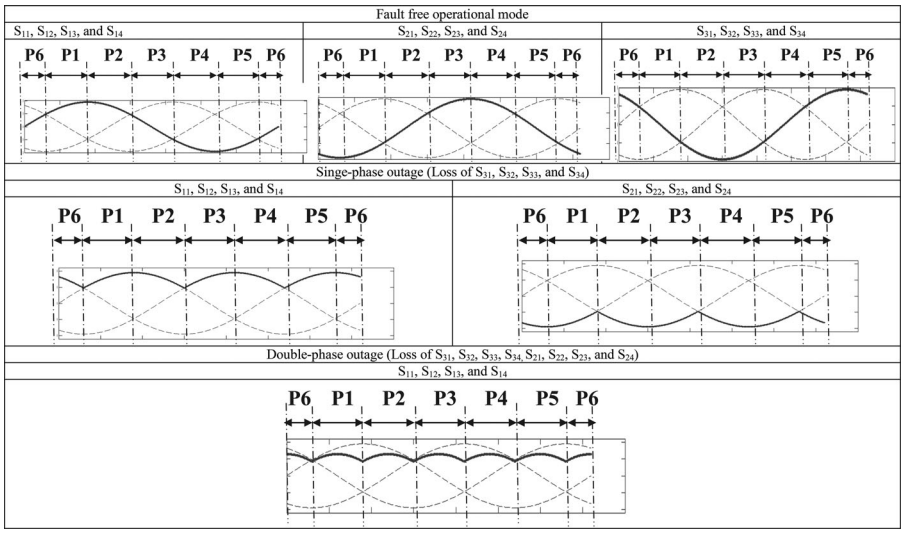
A. Case 1: FTSS Under Single-Phase Outage of the DC/AC Converter

If one of the phase outputs of the dc/ac converter is lost, the signature of the $V_{\rm REC}$ changes, which in turn affects the output phase voltages. To generate the pulsating-dc voltage that has the same characteristic (or information content) as that obtained under fault-free operation, one of the remaining dc/ac converter full-bridge converters has to generate a bipolar pulse train for the highest phase while the other full-bridge converter has to generate a bipolar pulse train for the lowest phase. "PWM1" and "PWM2" are two sets of four PWM signals which contain the information of the highest and the lowest phases in each sector if any one of $S_{1X\_\rm fail}$, $S_{2X\_\rm fail}$, or $S_{3X\_\rm fail}$ signals is 1 (see Fig. 8). Based on the diagnosed faulty phase in the dc/ac converter, they are applied to the remaining full-bridge converters via a set of two demultiplexers "PWM DEMUX1" and "PWM DEMUX2." For instance, if in any of the four sectors P1, P2, P4, or P5 the differences of $V_{\rm AB}$ and $V_{\rm CA}$ with their references are higher than a threshold, $S_{1X\_\rm fail}$ is set (see Fig. 5). Hence, PWM1 is connected to the second full-bridge converter (S2X switches) via PWM DEMUX1 and PWM2 is connected to the third one (S3X switches) via PWM DEMUX2. The result will be generation of the information of the highest phase by the second full-bridge converter and of the lowest phase by the third one in every sector.

B. Case 2: FTSS Under Double-Phase Outage of the DC/AC Converter

If two phases of the dc/ac converter are lost, the modulating reference of the remaining full-bridge converter has to be modified so as to encode the same information in the pulsating-dc voltage ($V_{\rm REC}$) as in fault-free operation. This information is nothing but the highest line voltage at each time. The mechanism to realize this FTSS is shown in Fig. 8. It shows that the required PWM reference in each of the time sectors P1 to P6

TABLE VI
PWM REFERENCES FOR THE DC/AC CONVERTER UNDER FAULT-FREE AND FAULT CONDITIONS FOR SECTORS P1–P6



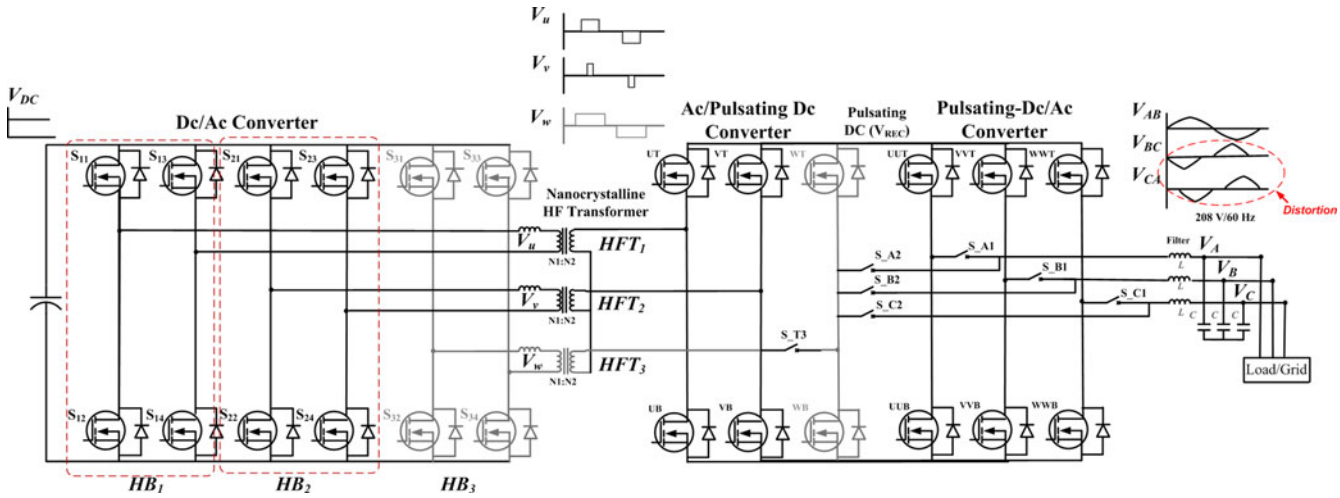


Fig. 9. Failure in a phase of ac/pulsating-dc converter causes the same distortion in the output line voltages as if the same fault is lost in the dc/ac converter. Failure of phase c in the ac/pulsating converter causes a distortion pattern from which the fault diagnosis algorithm considers a fault in phase c of both converters.

is generated using the PWM reference for the highest line voltage in that sector. Based on the diagnosed faulty phases in the dc/ac converter, the modified PWM is applied to the remaining full-bridge converter via demultiplexer PWM DEMUX1. For instance, consider that both of the S_{1X_fail} and S_{3X_fail} signals are set indicating that the only remained full-bridge converter in the dc/ac converter is the one consisting S_{21}, S_{22}, S_{23}, and S_{24}. Hence, the modified PWM is connected to the second full-bridge converter via PWM DEMUX1. The result will be generation of the information of the highest line voltage by the second full-bridge converter in every sector. Table VI summarizes the PWM references for nominal operation, single- phase outage, and double phase outage.

C. Case 3: FTSS for Fault in the AC/Pulsating-DC Converter

As explained in Section III, if a leg of the ac/pulsating-dc converter suddenly fails, it causes the same distortion pattern in the output line voltages as resulted from a failure of the same phase in the dc/ac converter. It was also shown that for the same reason, the fault diagnosis algorithm for these two converters are equivalent and upon detection of a certain distortion pattern in the output line voltages, a certain phase in both dc/ac converter and ac/pulsating-dc converter would be considered faulty. As an example, assume that during fault-free operation, suddenly a MOSFET in the phase C fails. Since the protection circuits of the module prevents firing of WT and WB (upon detection of a short circuit in the leg consisting these switching devices), V_{REC} will include only the information of phase A and phase B. As a result, output line voltages of the MI-TMI will be distorted according to the last row of Table III. This fault scenario is shown in Fig. 9. This specific distortion pattern in the output line voltages is interpreted using the fault diagnosis algorithm of Fig. 5 as a failure of phase C in either dc/ac converter or ac/pulsating-dc converter. The restoration steps are listed as follows:

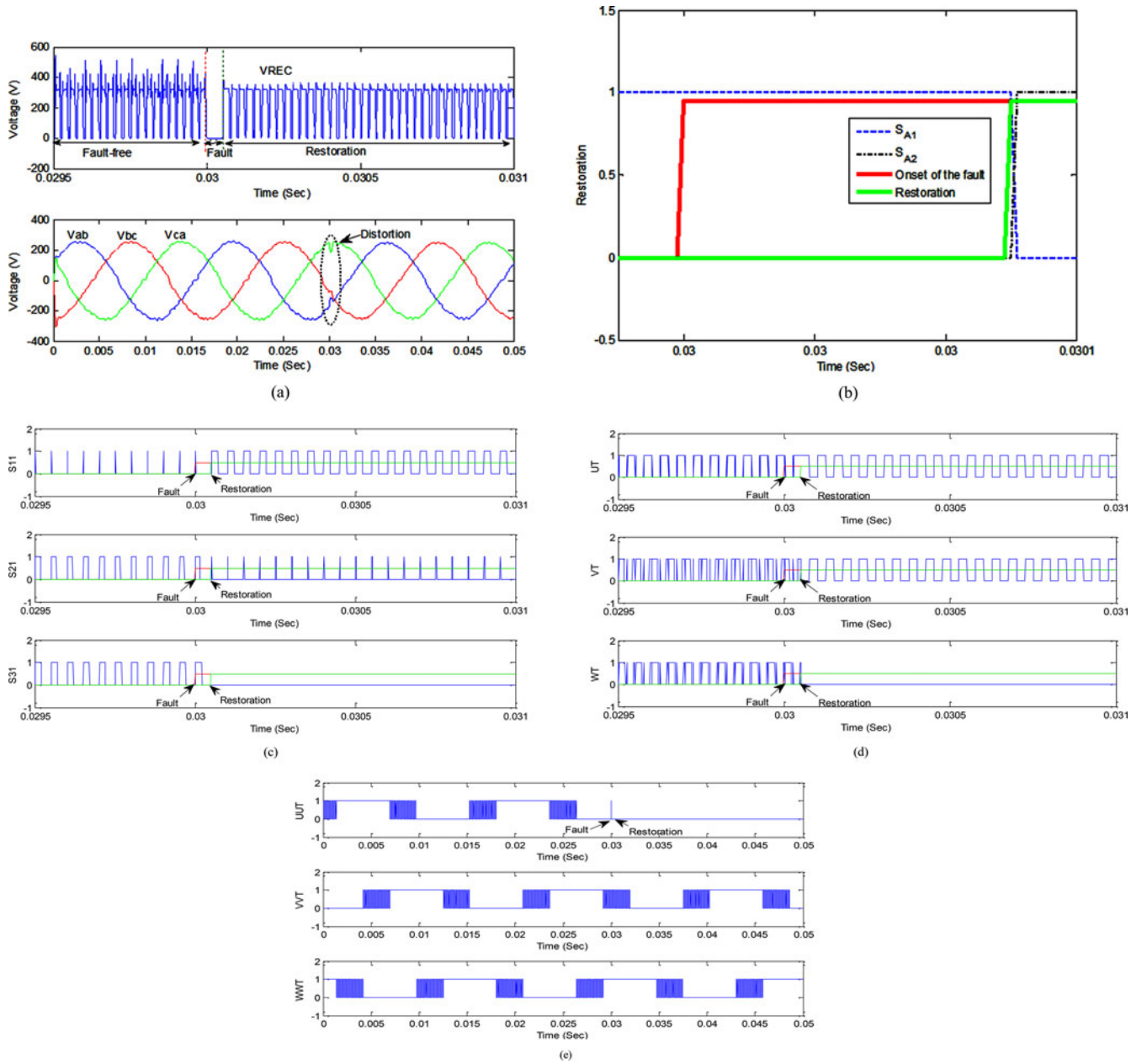


Fig. 10. FTSS for fault in the pulsating-dc/ac converter (failure of UUT at $t = 30$ ms). (a) Distortion in V_{REC} (top) and three-phase output voltages (bottom). (b) Signals showing the onset of the fault, restoration, and the state of isolating switches. (c),(d), and (e) Gate commands for MOSFETs in fault-free, and restoration mods of operation in dc/ac converter, ac/pulsating-dc converter, and pulsating-dc/ac converter.

1) deactivation of the gate pulses for S31, S32, S33, and S34 in dc/ac converter and WT and WB in ac/pulsating-dc converter;
2) modifying the PWM references for S11, S12, S13, S14 and S21, S22, S23, S24 switches according to restoration methodology of Fig. 8 and waveforms of Table VI.

In case of a failure in other phases, the above steps will be adjusted accordingly (see Fig. 8).

D. Case 4: FTSS for Fault in the Pulsating-DC/AC Converter

In Table V, a fault-diagnosis mechanism was developed for failure in switching devices of the pulsating-dc/ac converter. Irrespective of the type of failure (short circuit between any of the MOSFET terminals), the faulty circuit will be isolated upon detection of excess current or $V_{\mathrm{DS\_Sat}}$ depending on the protection circuits included in the power modules. But as mentioned previously, this only prevents extra damage to other devices and load. Yet, the output line voltages of the MI-TMI should be restored. Hence, upon detection of a failure in pulsating-dc/ac converter, the fault diagnosis algorithm identifies the failed converter arm and restoration action starts immediately based on the type of lost phase. For instance, if the fault occurs in phase a, upon being identified by fault diagnosis algorithm, the following actions are taken in order to restore the output line voltages:

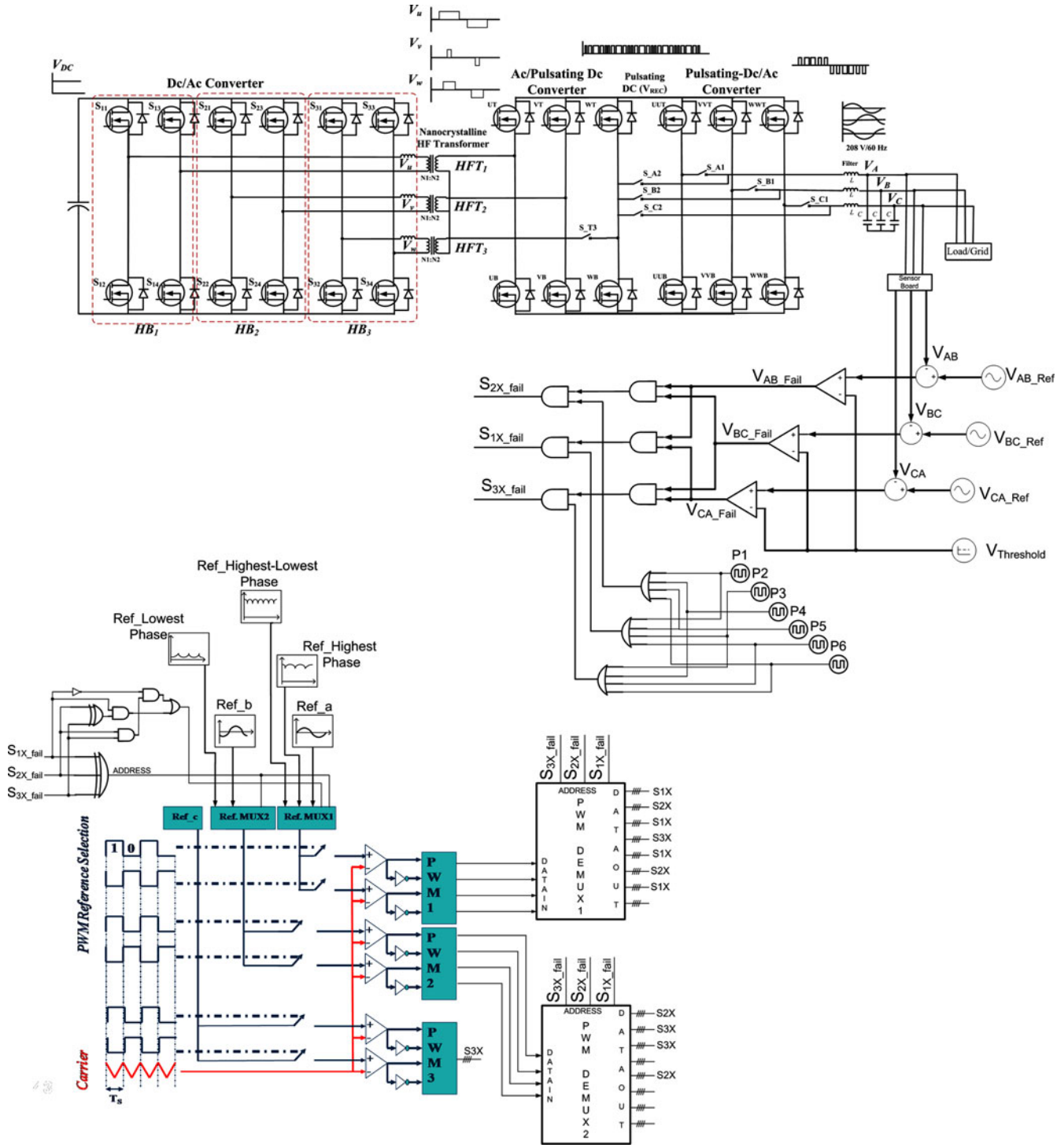


Fig. 11. Illustration of the overall fault diagnosis algorithm and FTSS for an isolated and multistage MI-TMI.

1) S_A1 and S_T3 will be opened;
2) S_A2 is closed;
3) PWM commands for UUT and UUB are applied to WT and WB, respectively;
4) PWM signals for $\{S_{1X}, x = 1,\ldots,4\}$ and $\{S_{2X}, x = 1,\ldots,4\}$ are changed as in the case if phase w is lost in the dc/ac converter (see Table VI). Also, PWM signals for $\{S_{3X}, x = 1,\ldots,4\}$ are disabled;
5) PWM commands for UT, UB, VT, and VB are changed as in the case if phase w is lost in the ac/pulsating-dc converter (see Table VI).

Fig. 10 demonstrates the simulation results of a failure in UUT. At $t = 30$ ms, due to a fault, a short circuit happens between drain and source of UUT. Protection logic disables gate commands for this leg (consisting of UUT and UUB) and the above steps are initiated. Restoration algorithm changes the gate

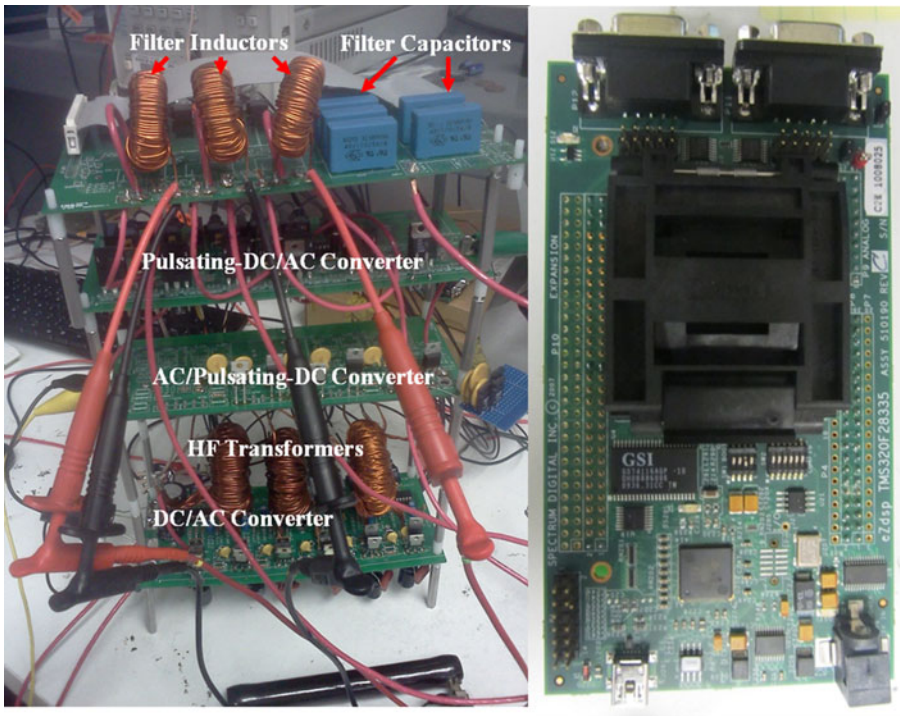


Fig. 12. (Left) 1-kW isolated and multistage MI-TMI prototype developed for validation of the proposed FTSS scheme. (Right) TMS320F28335 DSK board that generates the switching signals.

TABLE VII
PHYSICAL SPECIFICATIONS OF THE INVERTER PROTOTYPE

Input voltage	40 V
Output voltage	208 V
Switching frequency (DC/AC Converter)	20 kHz
Switching frequency (AC/Pulsating-DC, Pulsating-DC/AC Converter)	40 kHz
Rated power	1000 W
Controller board	TMS320F28335 (Texas Instrument)
Transformers: Nanocrystalline core (MK Magnetics # STX1060M1), Primary: 12T 6 x AWG14, Secondary: 52T AWG14	

pulses for the dc/ac bridge MOSFETs as well as ac/pulsating-dc bridge. Fig. 10(a) presents V_{REC} and three phase output voltages during the fault-free, fault, and restoration modes of operation. Fig. 10(b) shows the isolation of the faulty leg (UUT and UUB) using S_A1 and S_A2 commanded by the restoration algorithm. Fig. 10(c), (d), and (e) demonstrates the gate commands applied to the MOSFETs in the dc/ac converter, ac/pulsating-dc converter, and pulsating-dc/ac converter, respectively. Note that the gate commands of S_{13}, S_{23}, and S_{33} have the same pulse width as of those of S_{11}, S_{21}, and S_{31} and not shown for simplicity. It can be seen that after the onset of the restoration algorithm, the gate commands of the MOSFETs in the dc/ac converter are changed to modulate the new PWM references in Table VI (PWM references given for single-phase outage) as shown in Fig. 10(c). Note that because WT and WB no longer operate as an active rectifier leg (and are used as a substitute leg for the faulty leg of UUT and UUB), gate commands of UUT and UUB are applied to them in restoration. Accordingly, the gate commands of the MOSFETs of the ac/pulsating-dc converter are changed to be synchronous with the dc/ac converter [see Fig. 10(d)].

Now that fault diagnosis algorithm and FTSS for all of the possible faults in all of the stages in the MI-TMI of Fig. 1 are covered, the overall scheme is presented in Fig. 11.

V. EXPERIMENTAL RESULTS

In the previous sections, it was shown that in all of the possible fault scenarios, no matter in which stage a failure occurs, output line voltage restoration is based on an operation transition from three to two full bridges in the primary-side dc/ac converter. Specifically, if the fault diagnosis algorithm detects loss of phase A in dc/ac converter or ac/pulsating-dc converter, HB2 and HB3 will keep on operating with modified PWM references. If the failure of phase A is detected in pulsating-dc/ac converter, restoration process replaces (UUT, UUB) with (WT, WB) MOSFETs feeding phase A of the load. However, since there are only two legs remained in the ac/pulsating-dc converter (i.e., UT,

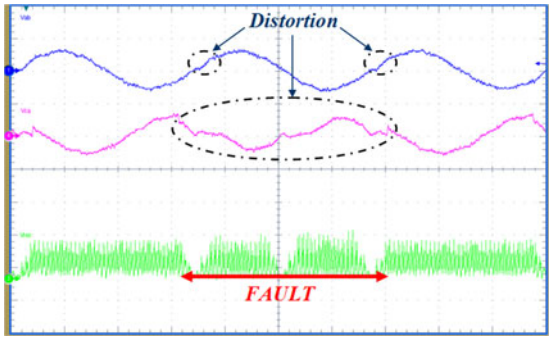


Fig. 13. Effect of a single phase outage (phase w) on the output line-voltages V_{AB} (top-500 V/div), V_{CA} (middle-500 V/div), and V_{REC} (bottom-500 V/div) of the MI-TMI in Fig. 1 versus time (5 ms/div). It is shown that failure of phase w causes a more severe distortion in V_{CA} rather than in V_{AB}.

UB, VT, and VB), dc/ac converter should operate with only two full bridges HB1 and HB2 (with modified PWM references). As such, the restoring operation of dc/ac converter which is the key part of the proposed FTSS is verified through experimental results in this section. Experimental results for the proposed FTSS are obtained using a MI-TMI prototype with the following specifications: nominal input voltage of 40 V, nominal output voltage of 208-V line-to-line (RMS), switching frequencies of 20 and 40 kHz for the dc/ac and the pulsating-dc/ac converters, respectively. The output power is 1 kW and the output *LC* filter has an inductance of 1 mH and a capacitance of 1 μF per phase. Fig. 12 shows the developed prototype and the DSP controller board. Table VII summarizes some technical specifications of the developed prototype. To verify the FTSS, three different scenarios are tested using a TMS320F28335-DSP-based controller and the relevant power-stage results are provided to ascertain the effectiveness of the FTSS under different fault conditions.

A. Scenario 1: Single-Phase Outage (i.e., Transition From Three Full-Bridge Converters to Two Full-Bridge Converters in the DC/AC Converter)

In this scenario, prior to the onset of the fault, three full-bridge converters of the dc/ac converter are generating three bipolar pulse trains containing the information of all of the three phases. At the onset of the fault, the full-bridge converter corresponding to phase w fails. Consequently, the information of phase c is no longer available to the pulsating-dc/ac converter. Fig. 13 shows the pattern of distortion in the output line voltages V_{AB} and V_{CA}. Restoration onsets by changing the PWM references for the remaining two full-bridge converters so as to provide the information of the highest and the lowest phases to the ac/pulsating-dc converter. PWM references (according to Table VI) for the dc/ac converter MOSFETs before and after loss of one full-bridge converter in the first fault scenario are shown in Fig. 14.

Fig. 15 shows that amplitude of V_{CA} and I_C fall to almost zero in the fault interval since the lost full-bridge converter is the one generating information of phase c. V_{REC} amplitude also falls to zero in the fault interval. Fig. 16 illustrates the distortions incurred in V_{AB} and I_A due to the loss of the full-

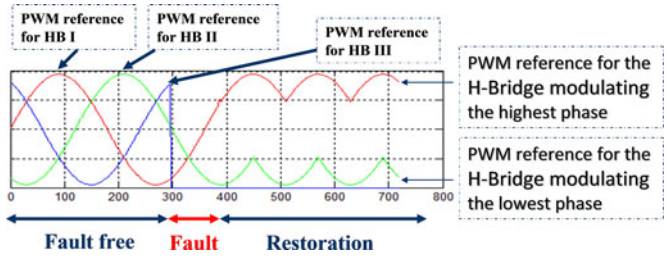


Fig. 14. PWM references for the dc/ac-converter switches before and after loss of one full-bridge converter in the first fault scenario.

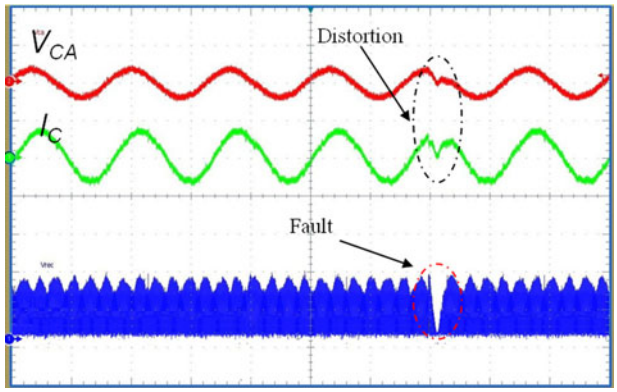


Fig. 15. V_{CA} (top-1 kV/div), I_C (middle-5 A/div), and V_{REC} (bottom-500 V/div) for scenario 1(10 ms/div): Loss of one full-bridge converter in dc/ac converter.

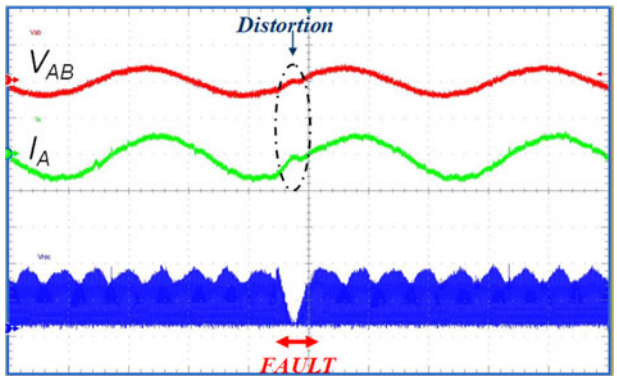


Fig. 16. V_{AB} (top-1 kV/div), I_A (middle-10A/div), and V_{REC} (bottom-500 V/div) in scenario 1(5 ms/div): Loss of one full-bridge converter in dc/ac converter.

bridge converter generating information of phase A. Note that as explained earlier, since the lost phase is w, it does not make a huge distortion on V_{AB} and I_A. However, since at the onset of the fault V_C is the highest phase and has reached the peak value, it causes a voltage collapse of V_{CA}.

Fig. 17 demonstrates V_{CA}, V_u, V_v, and V_w and a larger view of these waveforms in the fault-free, fault, and restoration operation. V_u, V_v, and V_w represent output voltages of three HF Transformers in Fig. 1. Fig. 17(b) is the larger view of these waveforms at 75° (fault-free operation mode). Note that, V_u and V_v have the highest and the lowest pulse widths, respectively.

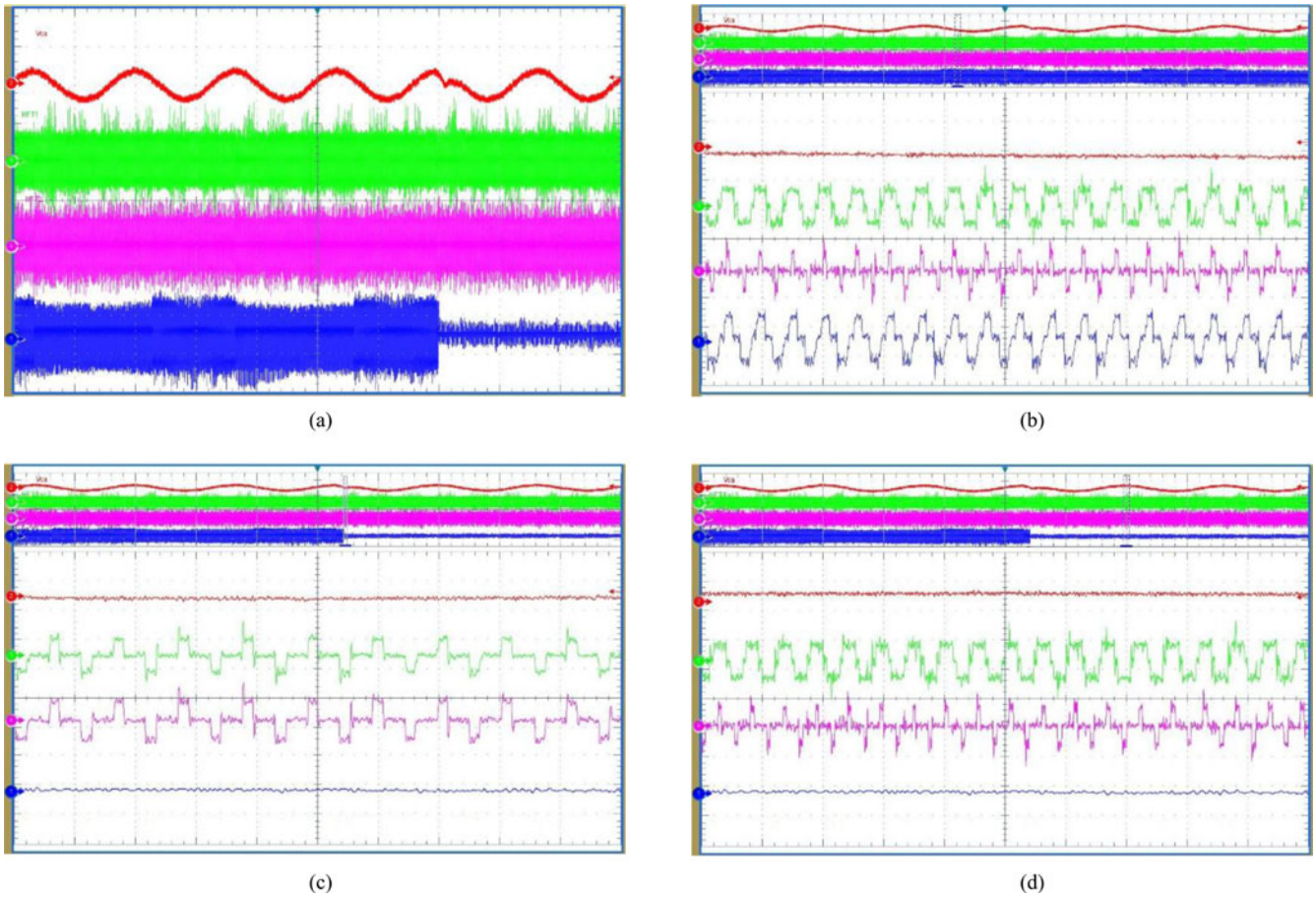


Fig. 17. (a) From top to bottom: VCA (1 kV/div), Vu, Vv, and Vw, (100 V/div–10 ms/div). (b) Fault-free operation interval (100 us/div). (c) Interval of the first fault scenario (100 us/div). (d) Restoration interval (100 us/div).

Fig. 17(d) shows the same at 690° when V_{CA} is reaches the peak. Note that since FTSS has changed the PWM references according to Table VI, V_u and V_v have the highest and the lowest pulse-widths, respectively. Assuming that the MI-TMI is operating under fault-free conditions and conditions based on Table VI, at 690°, V_u, V_v, and V_w are supposed to have the lowest, intermediate, and the highest pulse-width, respectively.

B. Scenario 2: Single-Phase Outage Followed by a Double-Phase Outage (in the DC/AC Converter)

This case demonstrates the impact of FTSS when one of the two remaining dc/ac converter phases fails while restoration is ongoing to recover the inverter from the earlier loss of another dc/ac converter phase. In particular, the full- bridge converter generating the highest phase is lost due to a second fault at 210°. Restoration onsets at 300° when the PWM reference for the only active full-bridge converter of the dc/ac converter is changed as demonstrated in Fig. 18. The new PWM references are obtained by subtracting the two references applied prior to the onset of this fault.

Fig. 19 demonstrates the adverse effect of this fault on the output line voltages of the MI-TMI. Following the second fault, V_{AB} and V_{BC} have a magnitude of zero before restoration initiates. Fig. 19(c) and (d) show a larger view of the output of the two

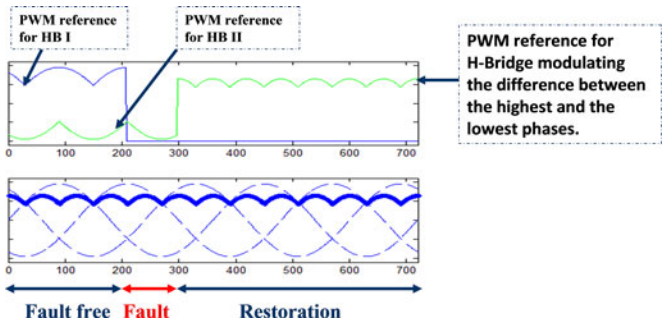


Fig. 18. PWM references for the dc/ac-converter switches before and after loss of another full-bridge converter in the second fault scenario of double-phase outage.

HF Transformers in Fig. 1 as well as V_{BC} under fault-free and restoration modes of operation. Subsequent to the adjustment of the PWM reference for the remaining active phase following FTSS, V_{AB} and V_{BC} are restored and operation is sustained.

C. Scenario 3: Failure in the Pulsating-DC/AC Converter Feeding a Single-Phase Load

In this scenario, it is assumed that the dc/ac converter is operating with two full-bridges ($\{S_{1X}, x = 1, \ldots, 4\}$ and $\{S_{2X},$

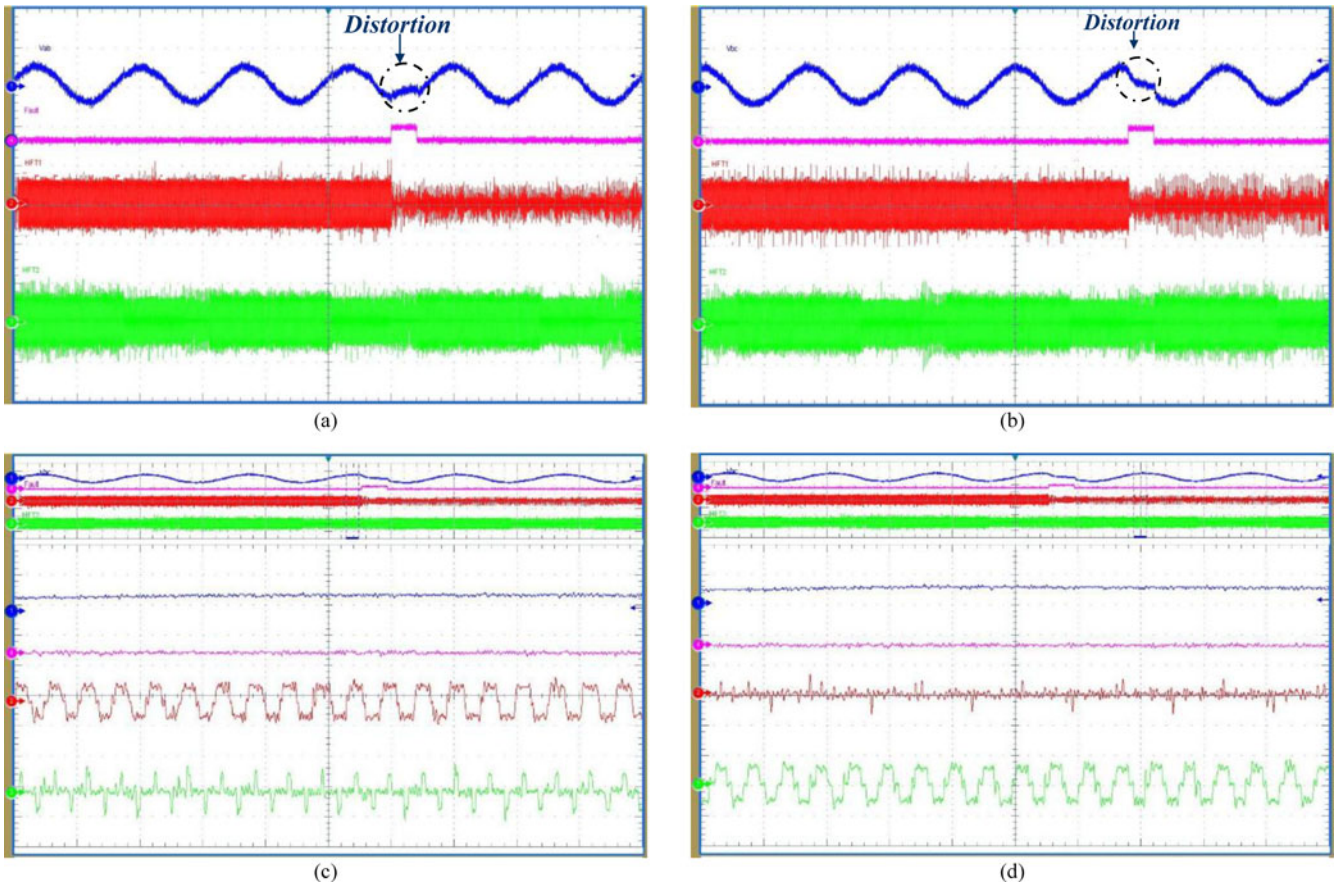


Fig. 19. Fault scenario 2: double-phase outage. (a) V_{AB} (1 kV/div–10 ms/div). (b) From top to bottom: V_{BC} (1kV/div—10 ms/div), signal indicating the onset of failure of one of the dc/ac converter phases at rising edge, and the onset of fault-tolerant control action at the trailing edge. Larger view of V_u , and V_v (100 V/div–100 us/div) are shown in (c) fault-free operation and (d) restoration interval.

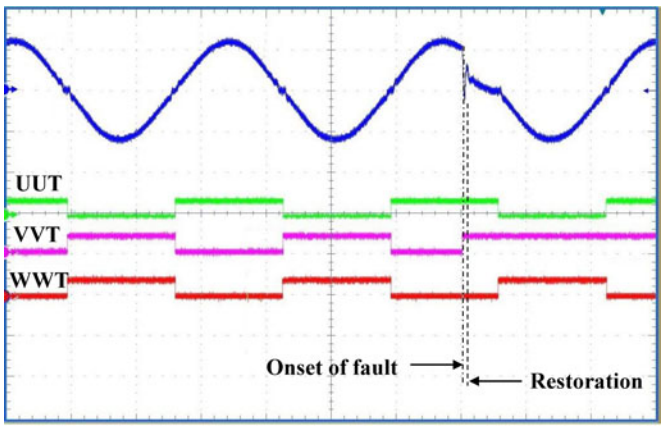


Fig. 20. Fault scenario 3: FTSS for the pulsating-dc/ac converter operating under single phase load. From top to bottom: output phase voltage (144 V/div–5 ms/div), PWM signals for pulsating-dc/ac converter switching devices.

$x = 1, \ldots, 4\}$) and consequently (WT, WB) are not switching. Pulsating-dc/ac Converter is feeding a single-phase load connected to the legs containing UUT, UUB, VVT, and VVB. Suddenly, a failure in the leg of VVT, VVB leads to isolation of this leg and interruption of the service. The fault is generated by deliberately turning on the high-side MOSFET (VVT) while UUT is on leading to a sag in the output voltage. Restoration algorithm opens S_B1 and closes S_B2 and also applies the PWM pulses of VVT and VVB to WT and WB so that the output phase voltage is restored. Fig. 20 shows the result of this scenario. The top trace, shows the output phase voltage and the rest of the traces from top to bottom are PWM pulses for UUT, VVT, and WT. Note that since V_{REC} encodes the information of the output phase voltage, Pulsating-dc/ac converter only needs to fold it with respect to positive and negative half cycles using low frequency PWM signals. It is shown that at the onset of the fault, both UUT and VVT are turned on and the output voltage falls to zero but FTSS replaces the lost leg of VVT and VVB with the redundant leg consisting of WT and WB in the active rectifier and restores the output phase voltage.

VI. Conclusion

A novel FTSS is proposed for all of the three stages in a MI-TMI. The proposed FTSS is designed based on the inherent redundancy of one phase in the primary side dc/ac converter and ac/pulsating-dc converter and is based on changing the PWM references for the remaining full-bridge converters upon

detection of the fault using a proposed fault diagnosis system. The new switching scheme provides the continuity of service of the inverter while maintaining acceptable dc-link and output voltages when one or even two phases of the dc/ac converter ceases to generate any output, or when one phase in ac/pulsating-dc converter or pulsating-dc/ac converter fails. Effect of the time (or phase angle) at which a fault happens was discussed and based on a comprehensive analysis of the latter a fault diagnosis algorithm is proposed. In the diagnosis step, the distortion pattern of the three line voltages V_{AB}, V_{BC}, and V_{CA} are diagnosed. As explained in Section III of this paper, by analyzing the pattern of distortion in each of the three line voltages with six sectors, we can determine the lost phase and the faulty stage. In the next step, based on the type of lost phase(s) and faulty stage, the PWM reference for the remaining phase(s) is changed so as to restore the output line voltages of the inverter. The effectiveness of the FTSS under various fault scenarios was investigated through experimental results on a 1-kW prototype and found to be satisfactory.

REFERENCES

[1] L. Empringham, J. W. Kolar, J. Rodriguez, P. W. Wheeler, and J. C. Clare, "Technological issues and industrial application of matrix converters: A review," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4260–4271, Oct. 2013.

[2] K. Basu, R. K. Gupta, S. Nath, and G. F. Castelino, "Research in matrix-converter based three-phase power-electronic transformers," in *Proc. Int. Power Electron. Conf.*, 2010, pp. 299–2803.

[3] S. Manias, P. D. Ziogas, and G. Olivier, "Bilateral dc to ac convertor using a high frequency link," *Proc. IEE*, vol. 134, no. 1, pp. 15–23, Feb. 1987.

[4] M. Koyama, K. Sanada, N. Sashida, and T. Kawabata, "High frequency link dc/ac converter with PWM cycloconverter for UPS," in *Proc. Int. Power Electron. Conf.*, 1990, pp. 748–754.

[5] S. K. Mazumder, "A novel hybrid modulation scheme for an isolated high-frequency-link fuel cell inverter," in *Proc. IEEE Power Energy Soc. Gen. Meeting*, 2008, pp. 1–7.

[6] P. Barriuso, J. Dixon, P. Flores, and L. Morán, "Fault tolerant reconfiguration system for asymmetric multilevel converters using bi-directional power switches," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1300–1306, Apr. 2009.

[7] A. Tajfar and S. K. Mazumder, "A fault-tolerant switching scheme for a photovoltaic high-frequency-link inverter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 2087–2094.

[8] A. Tajfar and S. K. Mazumder, "A transformer-flux-balance controller for a high-frequency-link inverter," in *Proc. IEEE Elect. Ship Technol. Symp.*, 2011, pp. 121–126.

[9] A. Rahnamaee and S. K. Mazumder, "A soft-switching modulation scheme for a three-phase capacitor-less pulsating-dc link transformer-isolated inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3893–3906, 2014.

[10] A. Tajfar and S. K. Mazumder, "Control of high-frequency-link inverter using optimal switching sequence," in *Proc. IEEE Energy Convers. Conf. Expo.*, 2012, pp. 4703–4710.

[11] A. Tajfar and S. K. Mazumder, "An optimal sequence-based-controller (OSBC) for a grid-connected three-phase photovoltaic high-frequency-link inverter," in *Proc. IEEE Appl. Power Electron. Conf.*, 2013, pp. 905–911.

[12] S. K. Mazumder and K. Acharya, "Multiple Lyapunov function based reaching criteria for orbital existence of switching power converters," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1449–1471, 2008.

[13] Z. Sang, C. Mao, J. Lu, and D. Wang, "Analysis and simulation of fault characteristics of power switch failures in distribution electronic power transformers," *Energies*, vol. 6, pp. 4246–4268, 2013.

[14] A. Gaillard, S. Karimi, P. Poure, S. Saadate, and E. Gholipour, "A fault tolerant converter topology for wind energy conversion system with doubly fed induction generator," in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 2007, pp. 1–6.

[15] R. R. Errabelli and P. Mutschler, "Fault-tolerant voltage source inverter for permanent magnet drives," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 500–508, Feb. 2012.

[16] Y. Song and B. Wang, "Analysis and experimental verification of a fault-tolerant HEV powertrain," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5854–5864, Dec. 2013.

[17] W. Wang, M. Cheng, B. Zhang, Y. Zhu, and S. Ding, "A fault-tolerant permanent-magnet traction module for subway applications," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1646–1658, Apr. 2014.

[18] S.-M. Jung, J.-S. Park, H.-W. Kim, K.-Y. Cho, and M.-J. Youn, "A MRAS-based diagnosis of open-circuit fault in PWM voltage-source inverters for PM synchronous motor drive systems," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2514–2526, May 2013.

[19] U.-M. Choi, H.-G. Jeong, K.-B. Lee, and F. Blaabjerg, "Method for detecting an open-switch fault in a grid-connected NPC inverter system," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2726–2739, Jun. 2012.

[20] S. K. Mazumder and R. Huang, "Multiphase converter apparatus and method," U.S. Patent 7 ,768 ,800 B2, Aug. 3, 2010.

[21] NXP Semiconductors, "Application note AN11243: Failure signature of electrical overstress on power MOSFETs," Rev. 01, Oct. 29, 2012.

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