Hybrid Modulation Scheme for a High-Frequency AC-Link Inverter

Sudip K. Mazumder, *Senior Member, IEEE*

***Abstract*—This paper describes a hybrid modulation scheme for a high-frequency ac-link (HFACL) multistage inverter comprising a front-end dc/ac converter, followed by isolation transformers, an ac/pulsating-dc converter, and a pulsating-dc/ac converter. The hybrid modulation scheme enables 1) removal of the dc-link filter evident in conventional fixed dc-link (FDCL) inverters placed after the ac/pulsating-dc converter stage and before an end stage voltage source inverter and 2) significant reduction in switching loss of the inverter by reducing the high-frequency switching requirement of the pulsating-dc/ac converter by two-third yielding higher efficiency, improved voltage utilization, and reduced current stress. Unlike the FDCL approach, in the HFACL approach, hybrid modulation enables the retention of the sine-wave-modulated switching information at the output of the ac/pulsating-dc converter rather than filtering it to yield a fixed dc thereby reducing the high-frequency switching requirement for the pulsating-dc/ac converter. Overall, the following is outlined: 1) hybrid modulation scheme and its uniqueness, 2) operation of the HFACL inverter using the hybrid modulation scheme, 3) comparison of the efficiency and losses, current stress, and harmonic distortion between the hybrid-modulation-based HFACL inverter and the FDCL inverter, and 4) scaled experimental validation. It is noted that the term hybrid modulation has no similarity with the modulation scheme for a hybrid converter (which are conjugation of two types of converters based on a slow and fast device) reported in the literature. The term hybrid modulation scheme is simply chosen because at any given time only one leg of the inverter output stage (i.e., pulsating-dc/ac converter) switch under high frequency, while the other two legs do not switch. The outlined hybrid modulation scheme is unlike all reported discontinuous modulation schemes where the input is a dc and not a pulsating modulated dc, and at most only one leg stays on or off permanently in a 60° or 120° cycle.**

***Index Terms*—AC link, high frequency, hybrid modulation, inverter, isolation, loss, reachability.**

I. Introduction

SI-DEVICE-BASED high-power inverters usually operate at low switching frequencies owing to higher switching loss and thermal limitations of Si. Low switching frequency yields bulky and expensive magnetic and capacitive filter elements or complex topological structure (for a given device breakdown voltage) to attain higher commutation frequency for the same device switching frequency. If isolation is required, conventional transformer core materials also yield heavier, costlier, and high-footprint space device. Recently, developed SiC MOSFETs (with 100–400X lower on resistance) and SiC Schottky diodes (with superior reverse recovery) [1], [2] with high thermal conductivity and thermal sustenance, and high permeability and efficient nanocrystalline-core-based transformers [3], [4] overcome some of these limitations. Clearly, they pave way for compact isolated high-power and high-frequency systems and have attained significant attention with regard to applications including renewable and alternative energy-based systems, fuel cell and energy storage applications, active filters, traction drives, and solid-state transformers because of potential for substantial reduction in materials and labor cost without significant compromise in efficiency.

Towards that goal, two high-frequency topologies have received attention [5]–[13]. The first topology, as shown in Fig. 1, will be referred refer to as the high-frequency ac-link (HFACL) topology. The second topology, which is referred in this paper as the fixed dc-link (FDCL) topology is obtained from Fig. 1 by simply placing a dc-link capacitor at the output of the ac/pulsating-dc converter. Both the topologies have a front-end high-frequency dc/ac converter followed by an ac/pulsating-dc converter and support galvanic isolation. However, the two topologies differ at the output stage. The output stage of the FDCL topology is a dc/ac voltage source inverter (VSI) that is preceded by a decoupling link capacitor. While the last stage of the HFACL topology is a pulsating-dc/ac converter, which is not preceded by any decoupling link capacitor. Furthermore, for the HFACL topology, the dc/ac converter is operated with sine wave modulation, while the pulsating-dc/ac converter is operated with hybrid modulation. For the FDCL topology, the dc/ac converter operates with square wave modulation and the final stage dc/ac converter (i.e., VSI) is sinusoidally modulated.

In the context of the HFACL inverter topology, a new innovation in the form of a hybrid modulation [5], [6] has been put forward by the author that significantly reduces the switching loss of the HFACL topologies (e.g., Fig. 1). This modulation scheme is unlike all reported discontinuous modulation schemes [14] where the input is a dc and not a pulsating modulated dc, and at most only one leg stays on or off permanently in a 60° or 120° cycle. The present three-phase hybrid modulation scheme is also different from earlier reported modulation schemes for single-phase direct power conversion systems [15]. The primary role of the modulation scheme for the single-phase pulsating-dc/ac converter is to demodulate the ac/pulsating-dc converter output on a half-line cycle basis to generate the output sine wave modulation pattern. This is different than the hybrid modulation scheme for the HFACL topology (see Fig. 1), where not all the legs modulate uniformly since the output of the ac/pulsating-dc

Manuscript received October 5, 2014; revised December 13, 2014; accepted March 5, 2015. Date of publication March 10, 2015; date of current version September 21, 2015. This work was supported in part by the U.S. National Science Foundation under Awards 0725887, 1002369, and 1239118. Recommended for publication by Associate Editor A. M. Trzynadlowski.

S. K. Mazumder is with the Laboratory for Energy and Switching-Electronics Systems, Department of Electrical and Computer Engineering, University of Illinois, Chicago, IL 60607, USA (e-mail: mazumder@uic.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2015.2411714

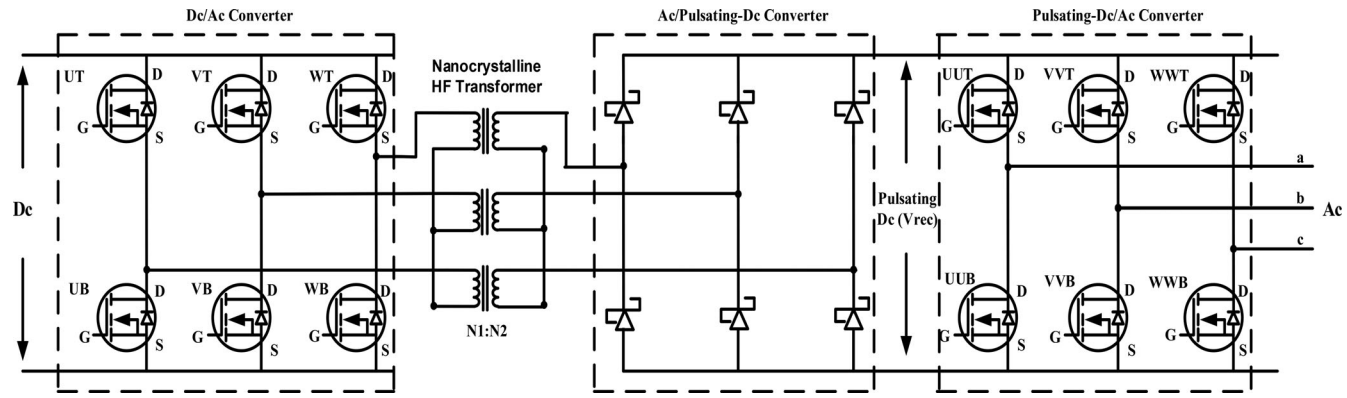

Fig. 1. Topology of an HFACL inverter. An FDCL topology has the same architecture except that it has a dc-link filter capacitor after the ac/pulsating-dc converter, and hence, the output stage (which operates as a VSI instead of as a pulsating-dc/ac converter) is fed with a dc voltage rather than a pulsating dc voltage ($V_{\rm rec}$) for the HFACL scheme. The hybrid modulation scheme evaluated in this paper for the HFACL topology is implemented for the pulsating-dc/ac converter stage. For the FDCL topology, the output stage dc/ac converter (VSI) is operated using other modulation scheme. To ascertain the effectiveness of the hybrid modulation scheme, the dc/ac converter is operated with the same sinusoidal PWM technique for both HFACL and FDCL inverter topologies. The ac/pulsating-dc converter simply rectifies the bipolar transformer secondary voltages.

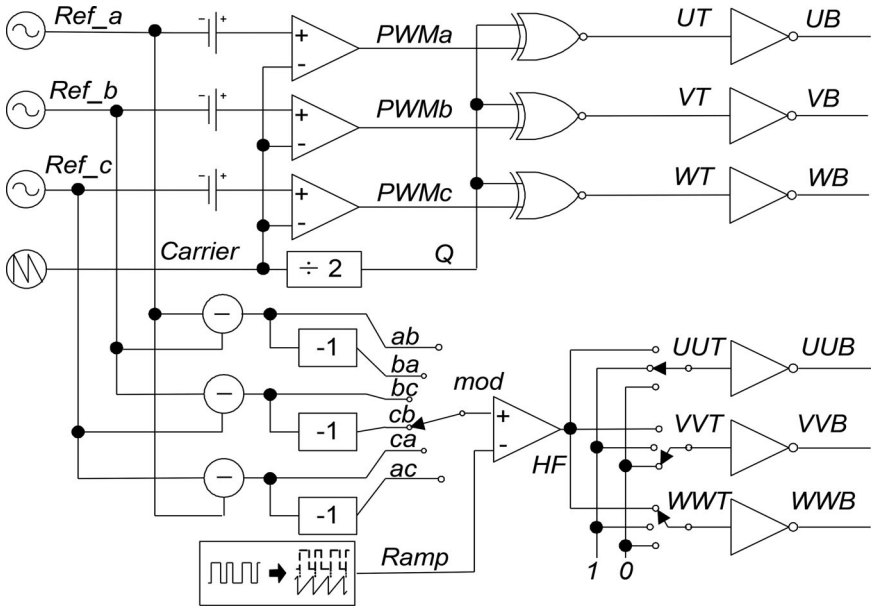

Fig. 2. Diagram of gate drive signal generation for the HFACL inverter.

converter contains encoded information of only one phase-to-phase voltage output of the primary-side high-frequency dc/ac converter.

Finally, the term hybrid modulation has no similarity with the modulation scheme for hybrid converter as reported in [16]. Hybrid converters are conjugation of two types of converters that are based on two different types of devices: one that supports higher power and switches at slow frequency and the other that operates at high frequency and supports lower harmonic power. The pulsating-dc/ac converter in Fig. 1 is a single converter. The term hybrid modulation scheme simply is chosen because at any given time (and as demonstrated in Section II), only one leg of the pulsating-dc/ac converter carries out forced switching while the switches in the other two legs do not change their switching states. This effectively yields a two-third reduction in the switching loss of the pulsating-dc/ac converter simply by modulation and without requiring any complex circuitry.

II. Overview of the Hybrid Modulation Scheme and HFACL Inverter Operation

The key concept regarding the operation of the hybrid modulation scheme relates to the evolution of the switching sequences of the output stage pulsating-dc/ac converter given the pulsating dc-link voltage waveform at the output of the ac/pulsating-dc rectifier. This pulsating dc-link voltage, in turn, evolves from the bipolar, high-frequency, and sinusoidally modulated output voltage waveforms of the front-end high-frequency dc/ac converter. Given that the dc/ac converter is modulated sinusoidally, the pulsating dc link voltage retains the sinusoidally encoded

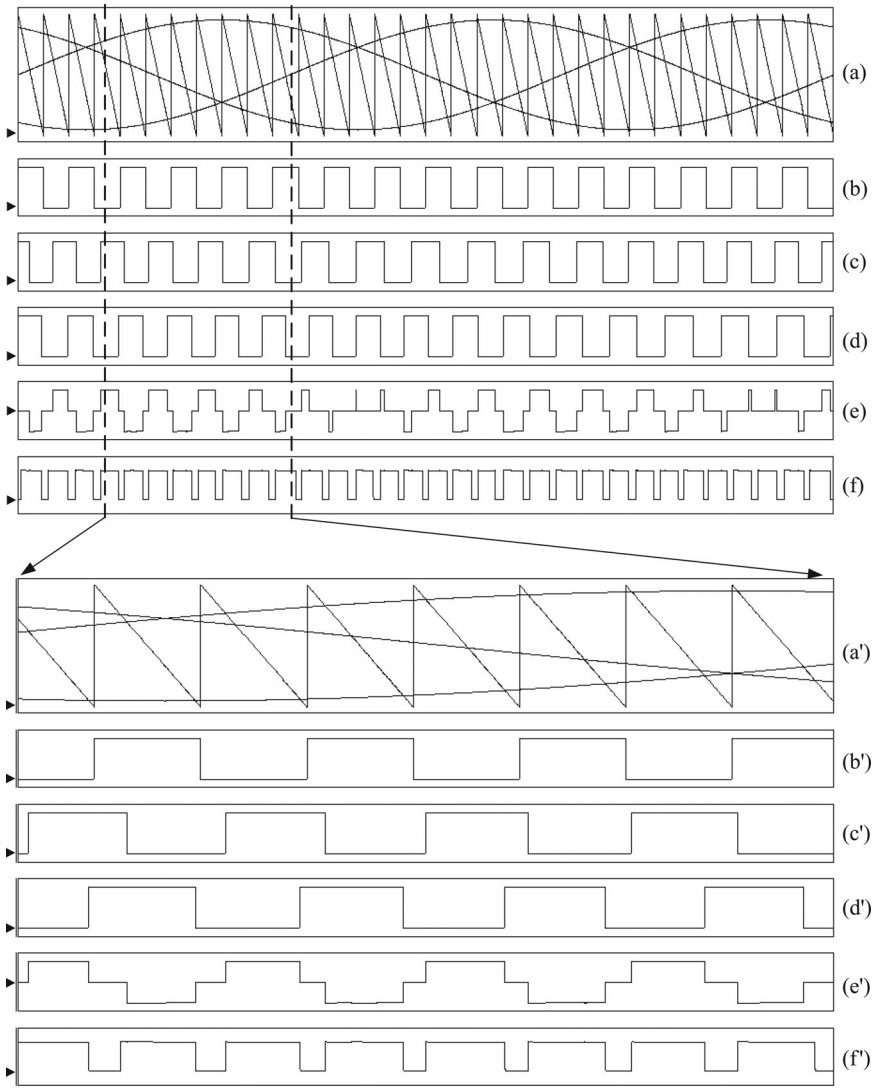

Fig. 3. Key waveforms of the primary dc/ac converter in one cycle and enlarged view of the interval between two dot lines: (a) three-phase sine wave references (Ref_a, Ref_b, and Ref_c) and carrier signal; (b) Q: square ware with half frequency of the carrier; (c) UT: gate signal for the upper switch of phase U; (d) VT: gate signal for the upper switch of phase V; (e) $V_{\rm uv}$: output of phase U and V; and (f) $V_{\rm rec}$: output waveform of the rectifier.

information of two active phases of the dc/ac converter because only the maximum phase-to-phase voltage of the dc/ac converter feeds the ac/pulsating-dc converter. As such, to create a balanced three-phase output using this pulsating dc-link voltage at the output of the pulsating-dc/ac converter, while two legs of the latter do not change switching states at all, the third leg has to be switched to reconstruct the remaining output phases. The choice of the two legs that do not change switching states changes every 60° of the 60-Hz line cycle. This is because every 60°, a new dc/ac converter phase-to-phase voltage attains the peak voltage. In addition to that, two additional issues need to be resolved: for the two legs of the pulsating-dc/ac converter that do not change switching states, what should be the switching state of each leg during the 60° period; and how should one switch the third leg of the pulsating-dc/ac converter that operates at high frequency. All of these have been outlined below in this section.

Fig. 2 illustrates the generation of switch gate signals for the HFACL inverter. The bottom switches are controlled complimentarily to the upper ones hence they are not described further. Three gate drive signals UT, VT, and WT for primary-side devices are obtained by phase shifting a square wave with respect to a 20-kHz square wave signal Q [shown in Fig. 3(b)]. Signal Q is synchronous with a 40-kHz sawtooth carrier signal, as shown in Fig. 3(a). The phase differences are modulated sinusoidally using three 60-Hz references for phases a, b, and c. Two gate signals (for switches UT and VT) corresponding to phases U and V are illustrated in Fig. 3(c) and (d), respectively. Because the carrier frequency is much higher than the reference frequency, UT, VT, and WT will be square wave with the frequency of 20 kHz and their phases are modulated. The resulting output phase-to-phase voltages at the primary side of the transformers are bipolar waveforms. Waveform $V_{\rm uv}$ is plotted in Fig. 3(e) as an illustration. It is noted that the

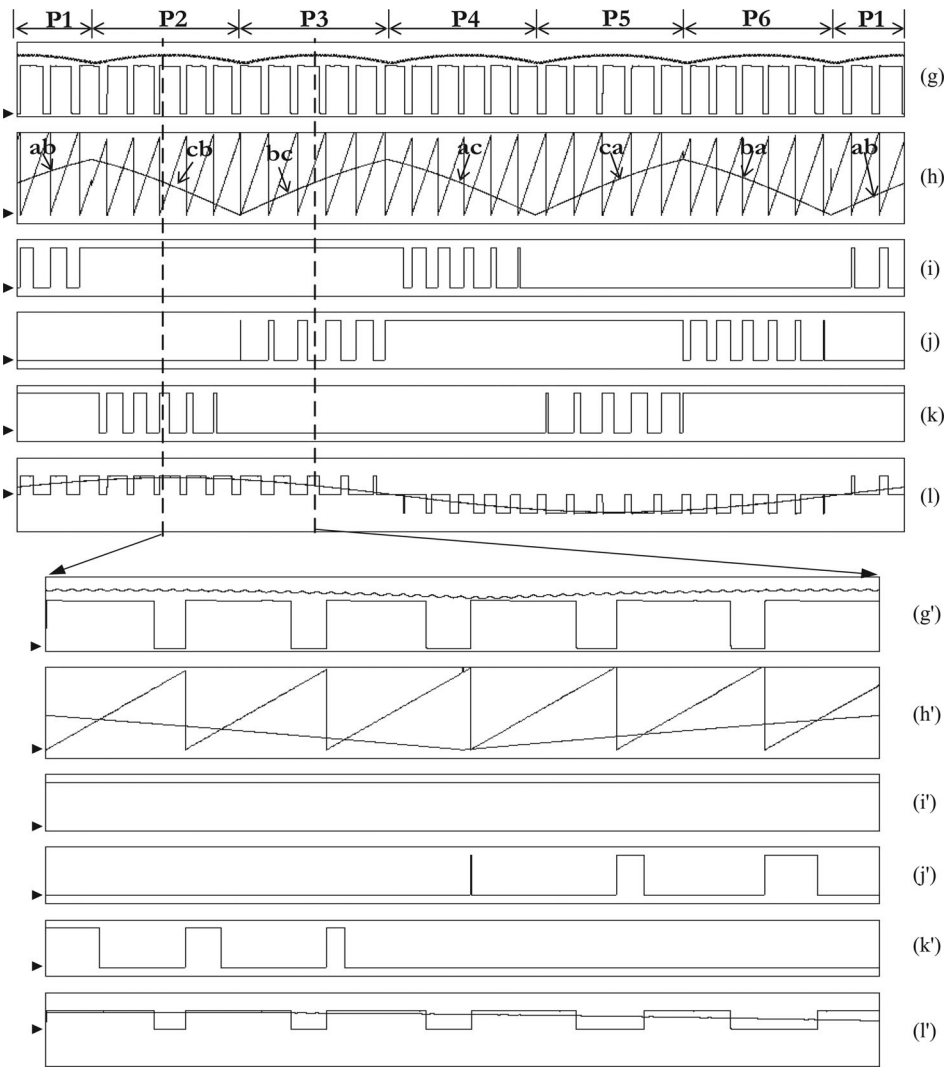

Fig. 4. Key waveforms of the hybrid-modulation-based pulsating-dc/ac converter in one cycle and an enlarged view of the interval between two dotted lines: (g) $V_{\rm rec}$: output PWM waveform of the ac/pulsating-dc converter with six pulse envelop; (h) mod: modulated signal and ramp: the carrier which is synchronous with (g); (i) UUT: gate signal for the top switch of phase a; (j) VVT: gate signal for the top switch of phase b; (k) WWT: gate signal for the top switch of phase c; and (l) PWM output of the line to line voltage $V_{\rm ab}$ and its envelop.

transformer is a high-frequency transformer since the flux balance is achieved at 20 kHz by using a volt–second balanced bipolar signal that ensures resetting every 50 μs. After passing through high-frequency transformers, the phase-to-phase voltage signals are rectified by the ac/pulsating-dc converter to obtain a unipolar PWM waveform, which has a six pulse as envelop. This waveform is shown in Fig. 3(f) and the mathematic expressions are as follows:

$$\mathrm{V_{rec}} = \mathrm{N.V_{dc}.MAX}\left(|\mathrm{UT}-\mathrm{VT}|, |\mathrm{VT}-\mathrm{WT}|, |\mathrm{WT}-\mathrm{UT}|\right) \quad (1)$$

$$\mathrm{UT} = \overline{\mathrm{Q}\otimes\mathrm{PWM_a}} \quad (2)$$

$$\mathrm{VT} = \overline{\mathrm{Q}\otimes\mathrm{PWM_b}} \quad (3)$$

$$\mathrm{WT} = \overline{\mathrm{Q}\otimes\mathrm{PWM_c}} \quad (4)$$

where $\mathrm{PWM_x}$ $(x = a, b, \text{or } c)$ denotes the binary comparator output between reference and carrier for phase x. Symbol $\otimes$ stands for XNOR operation, while N represents the transformer turns ratio. The six-pulse rectified waveform is partitioned into six segments named P1–P6 and is shown in Fig 4(g). The rising and falling edges of $V_{\rm rec}$ are different for different segment. Fig. 3(a)'–(f)' shows a particular time interval within segment 2, where the rising and falling edges of $V_{\rm rec}$ (marked as $\uparrow V_{\rm rec}$ and $\downarrow V_{\rm rec}$) are determined by the edges of UT and VT, respectively. Other cases are summarized in Table I.

TABLE I
EDGE DEPENDENCE OF THE RECTIFIER OUTPUT ON GATE SIGNALS

	P1	P2	P3	P4	P5	P6
$\uparrow \mathrm{V_{rec}}$	WT	UT	UT	VT	VT	WT
$\downarrow \mathrm{V_{rec}}$	VT	VT	WT	WT	UT	UT

TABLE II
SWITCHING PATTERN FOR UPPER SWITCHES OF THE PULSATING-DC/AC CONVERTER BASED ON HYBRID MODULATION

	P1	P2	P3	P4	P5	P6
$V_{\rm rec}$ (g)	$V_{\rm wv}$	$V_{\rm uv}$	$V_{\rm uw}$	$V_{\rm vw}$	$V_{\rm vu}$	$V_{\rm wu}$
UUT (i)	HF	ON	ON	HF	OFF	OFF
VVT (j)	OFF	OFF	HF	ON	ON	HF
WWT (k)	ON	HF	OFF	OFF	HF	ON
mod (h)	Ab	cb	bc	ac	ca	ba
$i_{\rm rec}$	(i_a+i_c, i_c) or $(-i_b, i_c)$	(i_a+i_c, i_a) or $(-i_b, i_a)$	(i_a+i_b, i_a) or $(-i_c, i_a)$	(i_b+i_a, i_b) or $(-i_c, i_b)$	(i_b+i_c, i_b) or $(-i_a, i_b)$	(i_c+i_b, i_c) or $(-i_a, i_c)$
$i_{\rm rec} > 0$	$i_b < 0 < 30°$ lagging $i_c > 0 < 30°$ leading	$i_a > 0 < 30°$ lagging $i_b < 0 < 30°$ leading	$i_c < 0 < 30°$ lagging $i_a > 0 < 30°$ leading	$i_b > 0 < 30°$ lagging $i_c < 0 < 30°$ leading	$i_a < 0 < 30°$ lagging $i_b > 0 < 30°$ leading	$i_c > 0 < 30°$ lagging $i_a < 0 < 30°$ leading

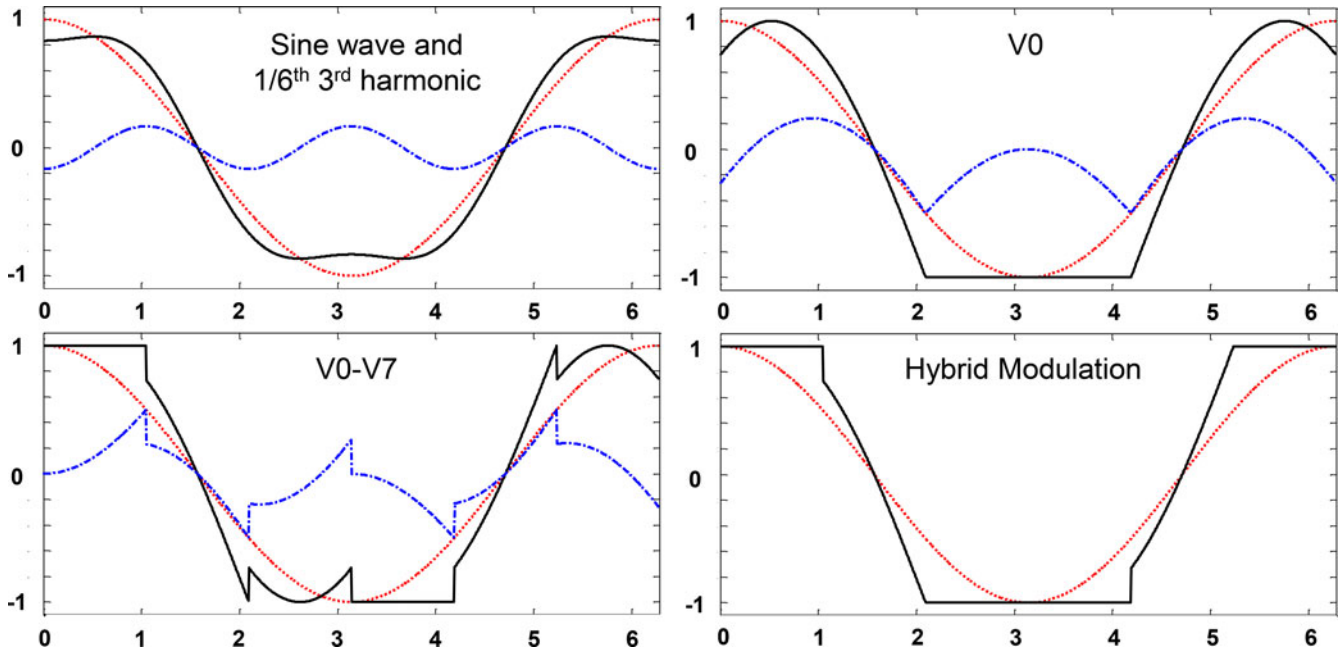

Fig. 5. Modulation functions corresponding to sine wave (with one-sixth third harmonic), V0, V0-V7, and hybrid modulation schemes. Blue and red traces represent zero sequence and sinusoidal signals, respectively. Black trace is the modulating signal.

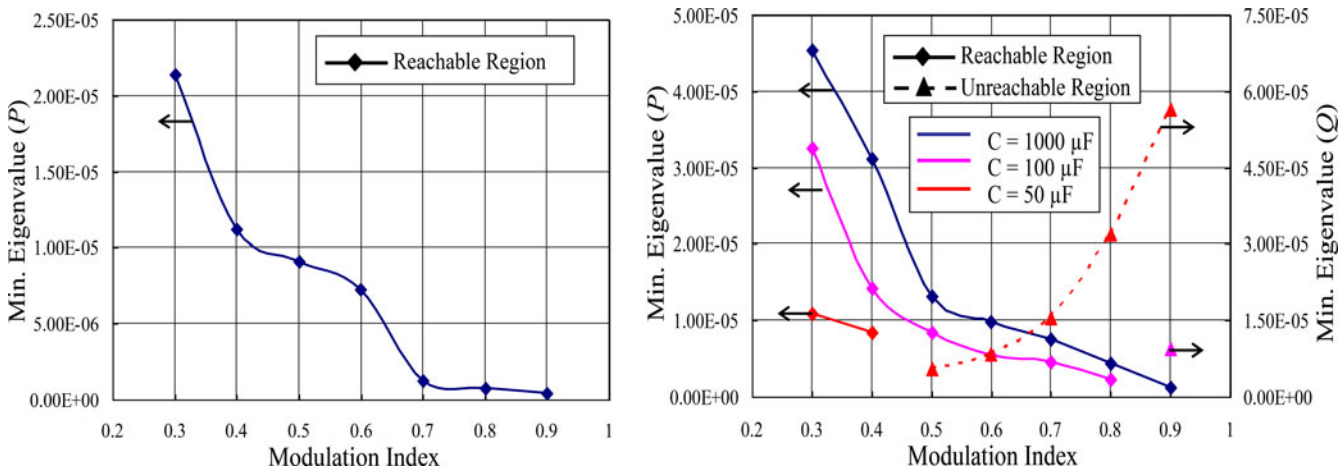

Fig. 6. Reachability analysis for (a) hybrid-modulated HFACL and (b) V0-V7 SVM-based FDCL inverter topologies. Clearly, the hybrid-modulation-based inverter provides a different underlying dynamics.

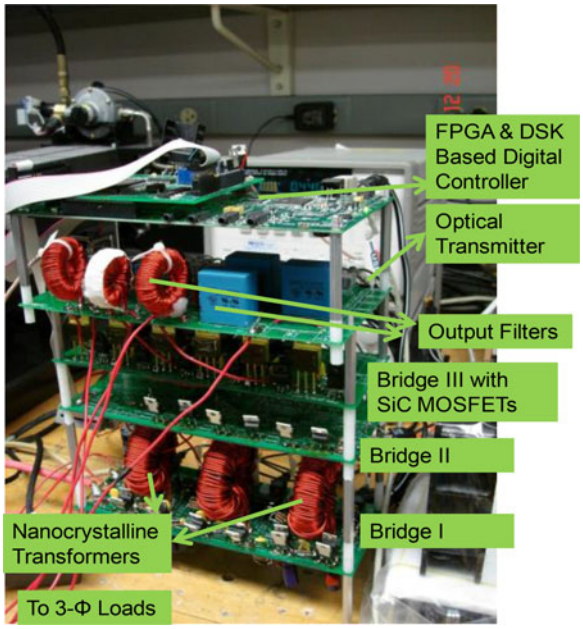

Fig. 7. Picture of the experimental inverter prototype.

TABLE III
MAIN COMPONENTS USED IN THE EXPERIMENTAL PROTOTYPE (SYMBOL X REPRESENTS PHASES U, V, AND W)

Name	Part Number and Descriptions
X1T, X2T, X1B, X2B	IPP070N06L; MOSFET, 60V/80A/6.7 mΩ
XT, XB	SiC MOSFET, 600V/20A, $R_{\mathrm{ds}}(on) = 0.125\ \Omega$
DXT, DXB	IDT016S60C, SiC Schottky Diode, 600V/16A/1.5 $\mathrm{V_F}$
Transformers	Nanocrystalline core; Primary: 12T 6 x AWG14; Secondary: 52T, AWG14

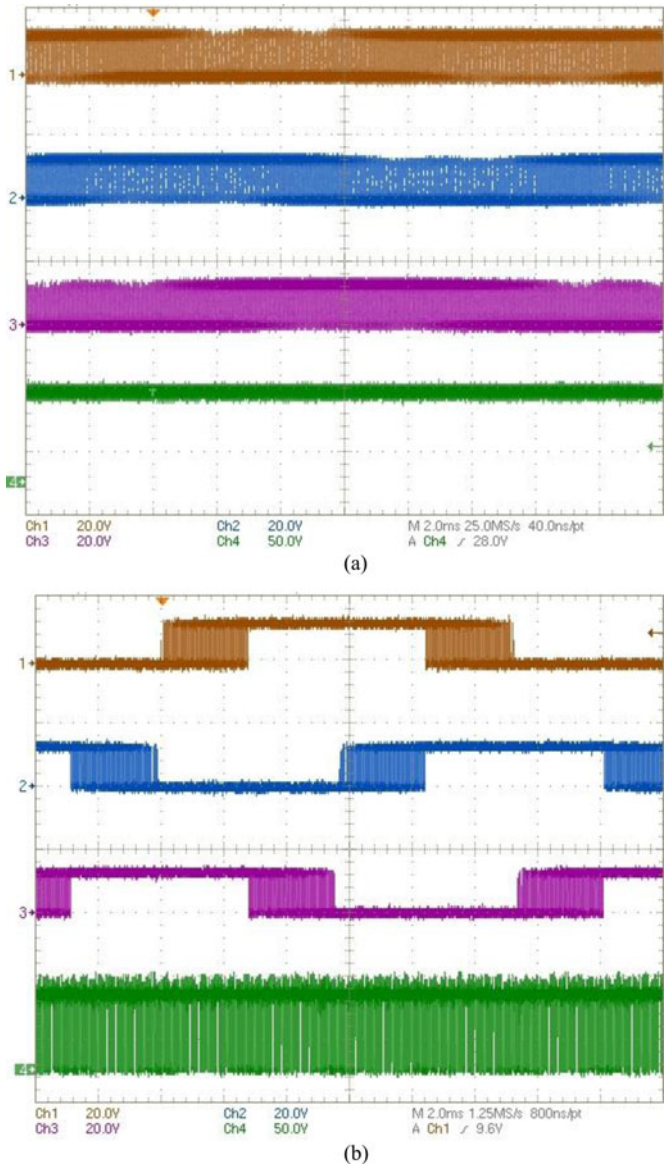

Fig. 8. Experimental signals of the Bridge III using (a): V0-V7 modulation and (b) hybrid modulation. Waveforms from top to bottom are: gate signals for UT, VT, WT and scaled V_{rec}. For (b), it is evident that at any given instant only one switch of the pulsating-dc converter switches at high frequency.

As alluded to before, the PWM output of the ac/pulsating-dc converter is contributed, respectively, by V_{wv}, V_{uv}, V_{uw}, V_{vw}, V_{vu}, and $\mathrm{V_{wu}}$ at each segment ranging from P1 to P6. The bottom part of the Fig. 2 shows the diagram of generating switching signals for three upper switches of the secondary-side pulsating-dc/ac converter. During each segment, every switch will be either: permanently ON ("1"), permanently OFF ("0"), or toggling with 40 kHz ("HF"). The switching pattern for the upper three switches in each segment for one-cycle period is summarized in Table II. In Table II, symbols (g), (h), (i), (j), and (k) are in reference to Fig. 4.

The switch positions illustrated in Fig. 2 are for the case of segment P2. Since the rectifier output has the same shape as V_{uv} within this interval, the phase-to-phase voltage V_{ab} at the output side of the pulsating-dc/ac converter is directly obtained by keeping switches UUT and VVT in ON and OFF status, respectively. Another phase-to-phase voltage V_{cb}, however, needs to be synthesized by operating switches WWT and WWB of the third leg at high frequency, where the modulated signal ("mod") is the difference between references c and b, and the carrier signal ("ramp") is a 40-kHz sawtooth waveform synchronized to the pulsewidth-modulated output of the ac/pulsating-dc converter. The key waveforms are shown in Fig. 4. The mathematic expressions for three phase-to-phase voltages are as follows:

$$\mathrm{V_{ab}} = \mathrm{V_{rec}} \cdot (\mathrm{UUT} - \mathrm{VVT}) \tag{5}$$

$$\mathrm{V_{cb}} = \mathrm{V_{rec}} \cdot (\mathrm{WWT} - \mathrm{VVT}) \tag{6}$$

$$\mathrm{V_{ca}} = \mathrm{V_{cb}} - \mathrm{V_{ab}}. \tag{7}$$

Because the high-frequency pulsating dc voltage at the output of the ac/pulsating-dc converter is encoded with sinusoidal information, only one of the pulsating-dc/ac converter legs needs to be force switched under unity power factor condition at any given moment. Devices of the other two legs do not change switching state. This considerably reduces switching losses.

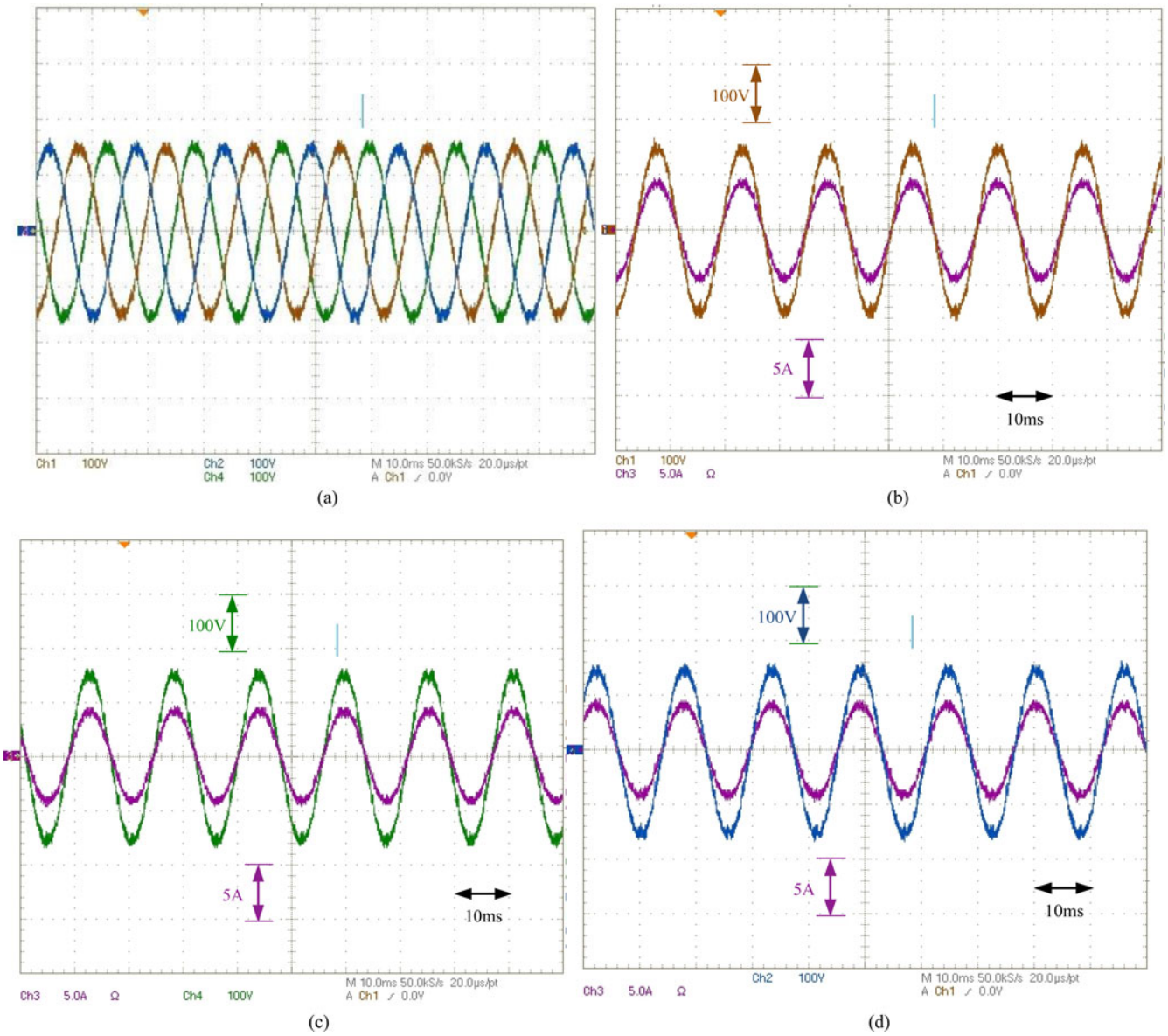

Fig. 9. (a) Output voltage of the HFACL-based inverter. (b)–(d) Output voltage and current of phases a through c.

Fig. 5 illustrates the modulation functions of the hybrid modulation scheme with four well-known SVM schemes (namely sinusoidal PWM with one-sixth third harmonic injection [14] and two discontinuous SVM schemes [17], [18]: V0 and V0-V7) to illustrate that there is an underlying difference between the new modulation scheme and existing ones. It is noted that V0-V7 SVM is the minimum switching loss scheme.

Finally, by using a newly developed technique (outlined by the author in [18]) for reachability analysis of switching power converters using composite Lyapunov function based on a hybrid model, we demonstrate in Fig. 6 that the hybrid-modulation-based HFACL inverter topology is not a limiting case of an FDCL topology for progressively reducing the dc-link capacitance. Basically, the procedure involves modeling the HFACL and FDCL topologies using the state-space hybrid model $\dot{\mathrm{x}} = \mathrm{A_i x} + \mathrm{B_i}$ (where the matrices are functions of the power stage parameters in the *i*th switching state which can be easily derived following [19] and [20]), and subsequently determining (to ascertain stability) if a matrix inequality $\sum_{\mathrm{i}=1}^{\mathrm{h}} \alpha_{\mathrm{ki}} \begin{pmatrix} \mathrm{A_i^T P_{ki}} + \mathrm{P_{ki} A_i} & \mathrm{P_{ki}} \bar{\mathrm{B}}_{\mathrm{i}} \\ \bar{\mathrm{B}}_{\mathrm{i}}^{\mathrm{T}} \mathrm{P_{ki}} & 0 \end{pmatrix} < 0$ is satisfied. This condition, where h represents the switching states in the *k*th switching sequence and $0 \leq \alpha_{\mathrm{ki}} \leq 1$, is satisfied if matrix P_{ki} is positive definite (i.e., if the minimum eigenvalue of P_{ki} is positive). In case this condition is not satisfied, determination of a dual matrix Q_{ki} to be positive confirms instability. Fig. 6 clearly shows the difference in reachability of the FDCL inverter with voltage-sourced final stage and varying dc-link capacitance, and the reachability of the HFACL inverter operating without the dc-link capacitance.

III. Results of the Performance of Hybrid Modulation

Fig. 7 shows an experimental unit of the hybrid-modulation-based three-phase HFACL inverter. The same setup has been used for obtaining experimental data using V0-V7 modulation for the FDCL inverter by simply inserting a 2.2-mF dc-link capacitor between ac/pulsating-dc rectifier and the output bridge. The three converter stages in Fig. 7 are identified as follows: Bridge I: (primary side) dc/ac converter; Bridge II: (secondary side) ac/pulsating-dc converter (diode rectifier); and Bridge III: used as a pulsating-dc/ac converter for the HFACL approach or as a VSI for the FDCL approach. The basic parameter details are provided in Table III. The designed input voltage of the inverter is 40-V dc. Transformer turns ratio is around 1:4.2. The inverter is controlled using an advanced TMS320C6713 DSP and EPF10K50VRC240–2-based Xcalibur FPGA digital controller boards.

Using this setup, several key experiments were conducted to analyze the performance of the hybrid modulation. To do an accurate assessment, we carry out the experiments as follows. First, the dc/ac converter (Bridge I) is operated using high-frequency sine wave modulation for both HFACL and FDCL approaches at 20-kHz switching frequency. Second, the ac/pulsating-dc rectifier (Bridge II) is chosen to be unidirectional (i.e., diode based) for both the cases. Thus, up to the output of the Bridge II (ac/pulsating-dc converter), there is no difference between the operation of the HFACL and FDCL inverters. The main difference is in the final stage or Bridge III. For the HFACL approach, Bridge III, fed by the pulsating dc-link voltage, is operated as a pulsating-dc/ac converter using hybrid modulation, while for the FDCL approach, Bridge III is operated as a VSI using V0-V7 modulation. This is demonstrated in Fig. 8. The switching frequency of Bridge III for the FDCL approach is set at 40 kHz. For the HFACL approach, the switching frequency is naturally set at 40 kHz because the ac/pulsating-dc converter rectifies the Bridge I bipolar 20 kHz output, thereby creating 40-kHz pulsating dc-link signal. The output voltage of the HFACL-based inverter is shown in Fig. 9(a), while the output voltage and current of each of the three phases are demonstrated in Fig. 9(b)–(d).

Fig. 10 shows the experimental efficiency of the Bridge III using hybrid modulation and V0-V7 modulation, respectively, for the HFACL and the FDCL approaches. Clearly, hybrid modulation provides higher efficiency. Simulation results in Fig. 11 give an insight into the cause. As evident, compared to V0-V7 modulation, hybrid modulation of Bridge III yields lower switching loss as well as conduction loss. Reduction in the conduction loss is attributed to the reduced RMS diode and the switch current of Bridge III, as evident in Fig. 12.

Finally, in Fig. 13, we demonstrate the experimental total harmonic distortion (THD) of the output voltage of the hybrid modulation and V0-V7 modulation-based inverter. We observe that, although the THD using hybrid modulation is higher, it is well within typical standard requirement of 5%. Most importantly, hybrid modulation achieves such low level of THD without a dc-link filter that it is used for the V0-V7 FDCL scheme. It is noted further that, by operating the HFACL inverter using

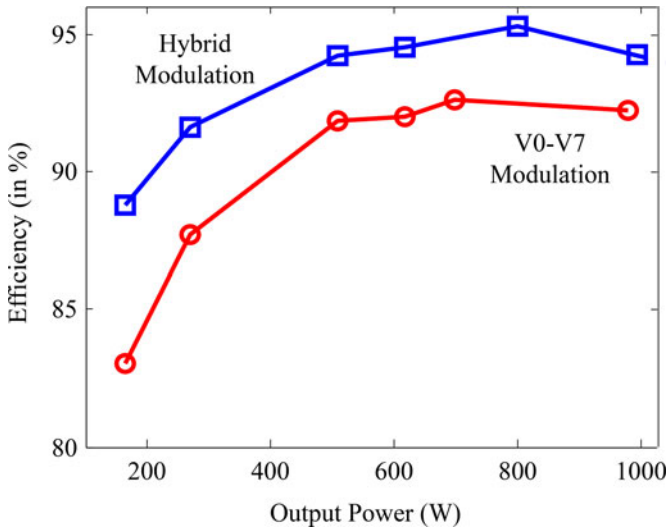

Fig. 10. Experimental efficiencies of the hybrid modulation and V0-V7 modulation-based Bridge III.

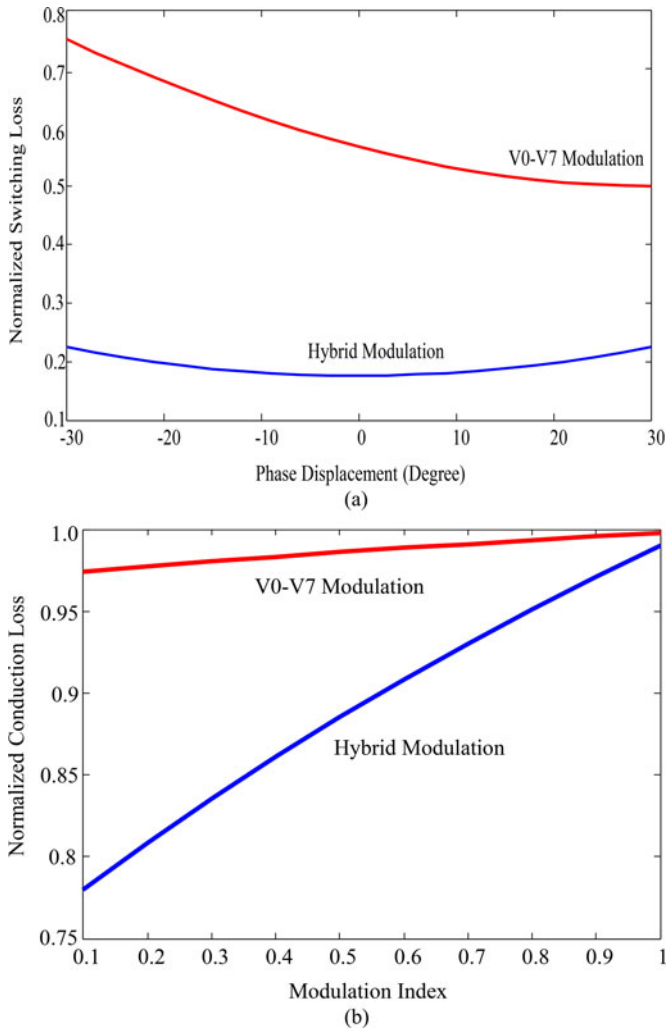

Fig. 11. Comparison of normalized (a) switching and (b) conduction losses of Bridge III using hybrid modulation and V0-V7 modulation.

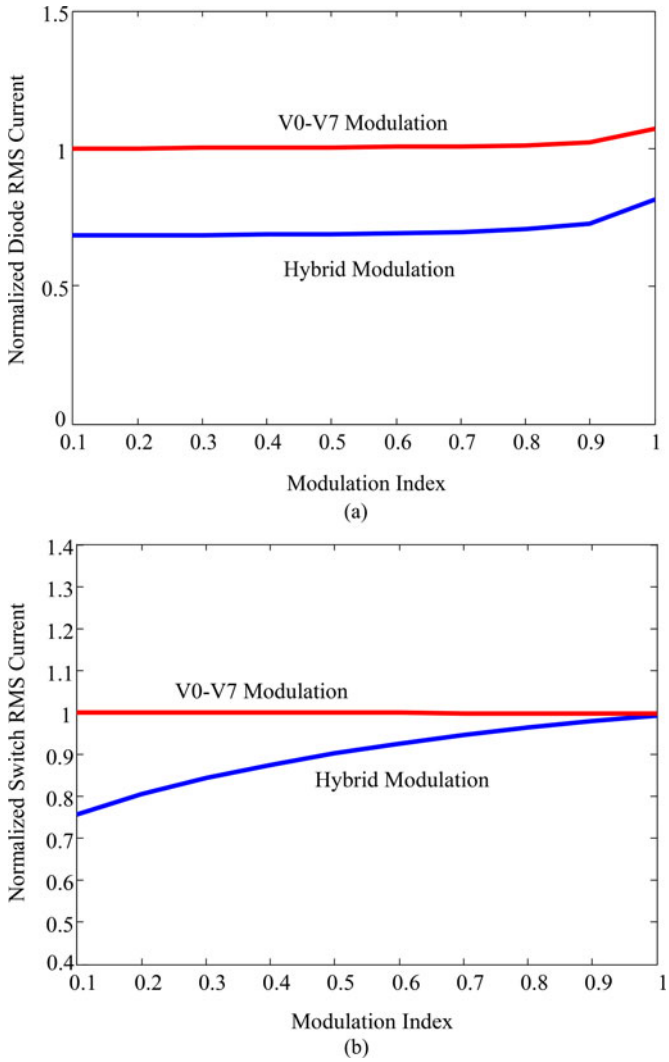

Fig. 12. Comparison of normalized (a) diode and (b) switch currents of Bridge III using hybrid modulation and V0-V7 modulation.

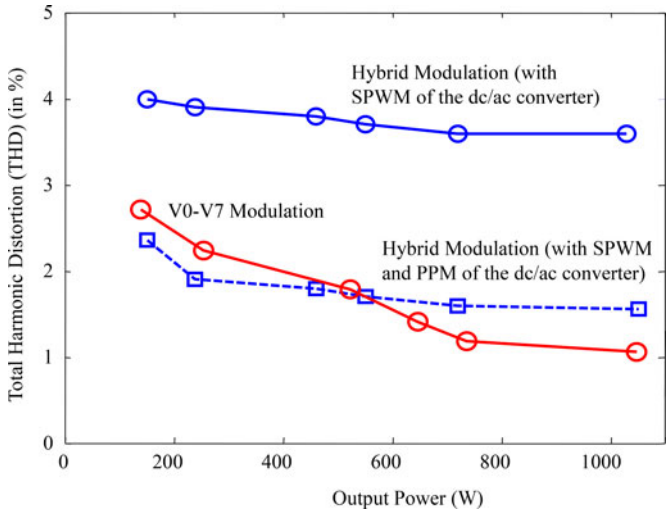

Fig. 13. Experimental THD of the output voltage of the hybrid modulation and V0-V7 modulation-based inverter. Symbols SPWM and PPM represent, respectively, sinusoidal pulse width modulation and pulse placement modulation.

a combination of pulse width and pulse placement modulation of the dc/ac converter along with the hybrid modulation of the pulsating-dc converter, one can reduce the THD of the output voltage to a value that is comparable to that obtained using the V0-V7 modulation [7].

IV. Conclusion

This paper demonstrates the performance of a hybrid-modulation-based HFACL inverter for high-power renewable and alternative-energy-based standalone, and distributed generation systems. It achieves high efficiency in spite of operating at high frequency owing to a significant reduction in switching loss of the output stage pulsating-dc converter and also due to a reduction in the conduction loss due to a net reduction in switch and diode RMS currents. This also leads to better dc-bus voltage utilization and lesser variation in the output voltage for the increasing load. Although the output THD is slightly higher for the hybrid-modulation-based inverter, it is well within the acceptable level and is achieved without any bulky dc-link filter, which is used for the FDCL inverter. It is noted that, by modulating the dc/ac converter based on pulse position and pulse width principles, the output THD of the HFACL inverter using the hybrid modulation is further reduced. It is also shown that the reachability of the hybrid-modulation-based HFACL system is not a limiting case for the FDCL system for the progressively reduced dc-link capacitance.

References

[1] H. Niwa, G. Feng, J. Suda, and T. Kimoto, "Breakdown characteristics of 12–20 kV-class 4H-SiC PiN diodes with improved junction termination structures," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2012, pp. 381–384.

[2] M. K. Das, C. Capell, D. E. Grider, R. Raju, M. Schutten, J. Nasadoski, S. Leslie, J. Ostop, and A. Hefner, 10 kV, 120 A SiC half H-bridge power MOSFET modules suitable for high frequency, medium voltage applications," in *Proc. IEEE Energy Convers. Congress Expo.*, 2011, pp. 2689–2692.

[3] W. A. Reass, D. M. Baca, and R. F. Gribble, "Multi-megawatt high frequency polyphase nanocrystalline transformers," presented at the High Megawatt Converter Workshop, Nat. Inst. Standards Technol., Gaithersburg, MD, USA, Jan. 24, 2007.

[4] G. Ortiz, M. Leibl, J. W. Kolar, and O. Apeldoorn, "Medium frequency transformers for solid-state-transformer applications—Design and experimental verification," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst.*, 2013, pp. 1285–1290.

[5] S. K. Mazumder and R. Huang, "Multiphase converter apparatus and method," US Patent 7 768 800 B2, Aug. 3, 2010.

[6] S. K. Mazumder, "A novel hybrid modulation scheme for an isolated high-frequency-link fuel cell inverter," in *Proc. IEEE Power Energy Soc. Gen. Meeting*, 2008, pp. 1–7.

[7] S. K. Mazumder and A. Rathore, "Impact of dc link pulse coding on the harmonic distortion of the high-frequency-link inverter," in *Proc. IEEE Ind. Electron. Conf.*, 2010, pp. 4499–504.

[8] J. Itoh, R. Oshima, and H. Takahashi, "Experimental verification of high frequency link dc-ac converter using pulse density modulation at secondary matrix converter," in *Proc. Int. Power Electron. Conf.*, 2014, pp. 1021–1027.

[9] S. Xu, Y. Xunwei, W. Fei, and A. Q. Huang, "Design and demonstration of a 3.6-kV–120-V/10-kVA solid-state transformer smart grid application," vol. 29, no. 8, pp. 3982–3996, Dec. 2013.

[10] K. Basu and N. Mohan, "A high-frequency link single-stage PWM inverter with common-mode voltage suppression and source-based commutation of leakage energy," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3907–3918, Sep. 2013.

[11] P. Jain, M. Pahlevaninezhad, S. Pan, and J. Drobnik, "A review of high-frequency power distribution systems: for space, telecommunication, and computer applications," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3852–3863, Nov. 2013.
[12] L. Chen, A. Amirahmadi, Q. Zhang, N. Kutkut, and I. Batarseh, "Design and implementation of three-phase two-stage grid-connected module integrated converter," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3881–3892, Dec. 2013.
[13] H. Keyhani and H. A. Toliyat, "Single-stage multistring PV inverter with an isolated high-frequency link and soft-switching operation," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3919–3929, Nov. 2013.
[14] D. G. Holmes and T. A. Lipo, *Pulse-Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ, USA: Wiley, 2003.
[15] B. K. Bose, P. M. Szczesny, and R. Steigerwald, "Microcomputer control of a residential photovoltaic power conditioning system," *IEEE Trans. Ind.. Appl.*, vol. IA-21, no. 5, pp. 1182–1191, Sep. 1985.
[16] M. Manjrekar and T. Lipo, "Hybrid multilevel power conversion system: A competitive solution for high power applications," *IEEE Trans. Ind. Appl.*, vol. 36, no. 3, pp. 834–841, May/Jun. 2000.
[17] H. Van der Broeck, "Analysis of the harmonics in voltage fed inverter drives caused by PWM schemes with discontinuous switching operation," in *Proc. Eur. Power Electron. Conf.*, 1991, pp. 31261–31266.
[18] A. M. Trzynadlowski and S. Legowski, "Minimum-loss vector PWM strategy for three-phase inverters," *IEEE Trans. Power Electron.*, vol. 9, no. 1, pp. 26–34, Jan. 1994.
[19] S. K. Mazumder and K. Acharya, "Multiple Lyapunov function based reaching criteria for orbital existence of switching power converters," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1449–1471, May 2008.
[20] A. Tajfar. (2014). A unified controller for a high-frequency-link (HFL) inverter. Ph.D. Dissertation, Department of Electrical and Computer Engineering, Univ. of Illinois, Chicago, IL, USA. [Online]. Available: (http://indigo.uic.edu/bitstream/handle/10027/19100/TAJFAR_ALIREZA.pdf?sequence=1

Sudip K. Mazumder (SM'03) received the M.S. degree from the Department of Electrical Power Engineering, Rensselaer Polytechnic Institute, Troy, NY, USA, in 1993, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA, USA, in 2001.

He is currently the Director of the Laboratory for Energy and Switching-Electronics Systems and a Professor in the Department of Electrical and Computer Engineering, University of Illinois at Chicago (UIC), Chicago, IL, USA. He has more than 23 years of professional experience and has held R&D and design positions in leading industrial organizations and has served as the Technical Consultant for several industries. He also serves as the President of NextWatt LLC, a small business organization that he setup in 2008. Since joining UIC, he has been awarded more than 40 sponsored projects by National Science Foundation, Department of Energy, Office of Naval Research, Environmental Protection Agency, CEC, AFRL, NASA, ARPA-E, NAVSEA, and multiple leading industries in above-referenced areas. He has published about 185 refereed papers in prestigious journals and conferences and has published one book and nine book chapters. He has presented 65 invited/plenary/keynote presentations at leading international conferences, organizations, and institutions, and currently, he also holds eight-issued patents. In 2014 and 2015, he was/has been invited by Applied Power Electronics Conference and Exposition, CDC, ACC, EPE, IEEE International Conference on Power Electronics, Drives and Energy Systems, IECON, ST Microelectronics, CBIP (Govt. of India), Texas A&M University to present his work on switching-sequence and switching-transition control for power-electronics-based energy systems. He delivered the first Plenary Lecture at the U.S. National Science Foundation hosted workshop on Energy Cyber Physical Systems in 2013. In 2006, he delivered a Plenary Lecture at the IEEE Power Electronics Specialists Conference; while in 2013, he delivered a Plenary Lecture at the International Symposium on Physics of Semiconductor Devices.

Dr. Mazumder received the Inventor of the Year Award at UIC in 2014, the University Scholar Award from the University of Illinois in 2013, and the Teaching Recognition Program Award at UIC in 2011. In 2008 and 2006, he received the prestigious Faculty Research Award at UIC for outstanding research performance and excellent scholarly activities. He also received the Office of Naval Research (ONR) Young Investigator Award and the National Science Foundation (NSF) CAREER Awards in 2005 and 2003, respectively, and prestigious IEEE Prize Paper Awards in 2002, 2007, and 2013, respectively. In 2005, he led a UIC student team to third place ranking as a part of the IEEE sponsored International Future Energy Challenge competition. He served as the first Editor-in-Chief for the *International Journal of Power Management Electronics* (currently known as Advances in Power Electronics) between 2006 and 2009. He has also served or is serving as the Guest Editor/Guest Coeditor for the following transaction special issues: IEEE TRANSACTIONS ON POWER ELECTRONICS Special Issue on high-frequency-link power-conversion systems (2013–2014); IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS special issue on control strategies for spatially distributed interactive power networks (2013–2014); Guest Associate Editor, IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS special issue on green power supplies (2015–2016); Guest Associate Editor, IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS special issue on sustainable energy systems integration (2014–2015); IEEE TRANSACTIONS ON POWER ELECTRONICS special issue on Power Electronics in dc distribution systems (2011–2013); *Advances in Power Electronics* special issue on advances in power electronics for renewable energy (2010–2011); and *Advances in Power Electronics* special issue on all electric ship technology (2012–2013). He serves as an Associate Editor for the following transactions: IEEE TRANSACTIONS ON POWER ELECTRONICS (since 2009), the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS (since 2003), and IEEE TRANSACTIONS ON AEROSPACE AND ELECTRONICS SYSTEMS (since 2008). He is also an Editorial Board Member for *Advances in Power Electronics*. Previously, he has also served as an Associate Editor for IEEE POWER ELECTRONICS LETTER. He is serving, respectively, as a Plenary Chair and as a Tutorial Chair for the 2015 and 2016 IEEE Energy Conversion Congress and Exposition. He is also serving as the Technical Awards Committee Chair for IEEE Power Electronics Society (PELS) Technical Committee on Sustainable Energy Systems (SES) since 2013 and chaired the Prize-Paper Awards Committee for the IEEE TRANSACTIONS ON POWER ELECTRONICS in 2014. He is also leading the effort to create the PELS Sustainable Energy Systems' Technical Achievement Award. Earlier his efforts led to the creation of the Sustainable Energy Systems' Best Paper Award. He also served as the Cochair for the IEEE PELS Technical Committee on Sustainable Energy Systems. He is also serving as the Co-Chair for IEEE PELS Subcommittee on Distributed Generation and Microgrid and for IEEE PELS Subcommittee on Power Semiconductors, and Committee Member for IEEE PELS Standards Subcommittee. In 2010, he served as the Chair, Student/Industry Coordination Activities for IEEE Energy Conversion Congress and Exposition, which is the largest conference in power electronics today in North America. He served as the Advisory Committee Member for 2012 IEEE India International Conference on Power Electronics and for 2010 IEEE International Symposium on Power Electronics for Distributed Generation Systems. In addition, he is serving/has served as the Technical Program Committee Member for numerous IEEE sponsored and other reputed conferences including IEEE Energy Conversion Congress and Exposition, IEEE Applied Power Electronics Conference and Exposition, IEEE Industrial Electronics Conference, and IEEE International Symposium on Power Electronics for Distributed Generation Systems.