A DirectFET-Based High-Frequency Fuel-Cell Inverter

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Abstract—In this paper, the design guideline for a highpower-density inverter for fuel-cell (FC) applications is presented. Such an inverter can lead to savings in volume and weight due to high-frequency operation. In addition, we present a guideline to determine the optimal size of the input filter. It is also illustrated that, for such a topology, an optimal choice of transformer leakage inductance is necessary to achieve low power loss and to establish a balance between efficiency and reliability. Transient load condition, which may degrade FC-stack reliability, is handled through a battery-sourced energy-buffering unit. Experimental results demonstrating the nominal operations of inverter and energy buffering unit are presented.

Index Terms—Cycloconverter, energy buffering, fuel cell (FC), GaAs Schottky diode, high frequency (HF), inverter, planar transformer, power density.

I. INTRODUCTION

S. DEPARTMENT of Energy (DOE) has recently emphasized the need for near-zero-emissions and ultrahigh-efficiency technologies for electric power generation. These environmental characteristics are inherent in fuelcell (FC) systems [1]. Electric power generation is emerging as the first large-scale commercial application for FCs and will account for more than half of related global product and service demand by 2014, according to U.S. FC Council. This application area is also one of the centerpiece emerging energy technologies to address the mounting crisis resulting from total dependence on existing fossil-fuel-energy systems. In [2], an outline of the market share of the promising FC technology applications poised for rapid growth is outlined. The framework for integrating these advanced power generation sources with the existing stationary energy infrastructure has been provided by the concept of a microgrid [3], [4], which is intrinsically linked to the burgeoning concept of distributed generation (DG). Apart from DG, the compact FC energy systems are also very attractive solutions for automotive applications and this market is expected to grow significantly in the next few years [5].

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Technology development in power electronics plays a crucial role in improving various stationary and automotive system performances, which will further drive their penetration into the electricity and vehicular markets [2]. However, viable application of FC energy sources for these wide-ranging applications requires the development of power-electronic systems to convert FC's variable dc output voltage to commercial ac output that meet the following requirements [6]: 1) low cost; 2) high energy efficiency; 3) high reliability; and 4) high power density. During recent times, several power-electronicsystem topologies, which address one or more of the above factors, have been proposed [7]-[20]. For instance, in [13], a hybrid FC system comprising an auxiliary battery buffer is outlined. However, it interfaces to a monolithic stack, and the nonmodular inverter, apart from being a three-level system, requires a dc-link capacitor. The latter is also a requirement for a FC inverter system outlined in [14]. In [15], an interesting FC and battery-based isolated inverter system is proposed. However, it needs a dc-link capacitor and it will be fed by a monolithic stack because of the nonmodular topology of the inverter. In [16], a modular full-bridge (FB)-based inverter, similar to that proposed in [17] (which forms the basis of this paper), is proposed. However, integration of the battery buffer is not outlined. Similar primary-side FB converter modularity is demonstrated in [18]; however, this paper limits to an isolated dc/dc converter only and does not include the energy buffer. Mazumdar et al. [19] outline a two-stage inverter with the second-stage cycloconverter demonstrating line-frequency switching but subject to diode reverse recovery. However, the primary-side converter is nonmodular and the operating frequency is much lower than that pursued in this paper. In addition, the integration of energy buffering has not been considered. In this paper, we present the design of a high-energy density FC power-electronic system (Fig. 1) with a modular converter architecture consisting of a highfrequency (HF) inverter followed by a forced cycloconverter.

Another important issue for FC power-conversion systems is the selection of the rating of the FC stack. At present, no widely accepted output voltage rating for the FC stack has been established as an industry standard. High input voltage designs require a large number of cells. The failure or poor performance of any one cell can result in the failure of the entire stack. As stack height (cell count) increases, there is an increasing probability of least one cell causing the entire stack to fail. This effect is shown in Fig. 1 [21] for Solid oxide fuel cell (SOFC). In general, the rated output voltage of a stack decreases over time through various cell degradation mechanisms [22], [23]. FC system developers, recognizing

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Fig. 1. Binomial distribution effect of SOFC cell count on stack yield.



Fig. 2. Left: joined stack array designs for tall FC stacks [24]. Right: modular stacks of a planar SOFC.

that this dilemma (tall stacks needed for high voltage versus increasing failure probability with stack height) impacts both cost (yield) and reliability, have attempted to mitigate this effect by creating designs which attempt to provide parallel connection of multiple cells within the stacks and multiple parallel stacks for power scaling, as shown in Fig. 2.

Such a low-voltage and high-current energy source creates several challenges for power-electronics design: 1) mitigate conduction loss due to high source current for a given load demand and 2) boost low input voltage without encountering instability (e.g., for a front-end dc/dc boost converter) or reliability (e.g., for an isolated FB converter that has to deal with large turns ratio and possibly transformer leakage inductance leading to higher voltage spikes and losses in the power devices). This paper, therefore, discusses power-electronics-design strategies particularly for a low-voltage, high current FC-stack output.

A final design issue is related to handling the reflected inverter low-frequency ripple current, which can degrade the efficiency and life of the FC stack [22]. For single-phase inverter applications, the peak current drawn from the stack is double for unity-power-factor passive loads and even larger for passive reactive loads compared with the average dc current [8]. For harmonic loads, the ripple depends on the load power factor and the harmonic content of the load current [22]. Overall, to handle such current ripples, the stack has to be significantly oversized, which increases the installation and operating costs. Typically, capacitive filter solutions are used to limit the low-frequency current drawn from the stack. In this paper, we present a design guideline to choose the optimum size of a capacitive input filter from the standpoints of the overall system energy density and cost.

II. SYSTEM DESCRIPTION AND OPERATION

The overall dc-link capacitor-less power-electronic system [Fig. 3(a)] consists of four HF phase-shifted zero-voltageswitched (ZVS) FB converters (connected in parallel at the input) and a single line-frequency ac/ac cycloconverter [8] followed by an *LC* filter [Fig. 3(a)]. Because of lowinput voltage, current handled by the primary-side devices is significantly high leading to higher conduction and switching losses. To reduce loss, this topology consists of parallel modules on the primary side. Such an arrangement also results in individual transformers with lower turns-ratio, thereby reducing the leakage inductance for each of them. To provide the desired bus voltage for generating a 110 V/60-Hz output, the secondaries of the transformers are connected in series.

The switches of the HF converter are sinusoidally modulated based on the output of a voltage-mode controller. For high-energy density, we operate the converter at high switching frequencies (reducing the size and weight of the magnetic components). While being advantageous from the energy density point of view, HF operation also leads to the increased switching losses. To address this issue, we use surface-mount power MOSFETs (i.e., DirectFET [25]) for the HF converter, which have significantly low conduction and switching losses compared with the conventional power MOSFETs. Because the switches for ac/ac cycloconverter operate at line frequency, their switching losses are minimal.

An energy-buffering unit is used to provide the additional energy requirements during load transients, as shown in Fig. 3(c). This unit provides the additional energy to the load during the short period of high energy demand, and then automatically shuts off when the air and fuel flow rates for the FC stack readjusts to new load demand. A four-module basic dc/dc boost converter is used to step up the battery output voltage (12 V) to the rated bus (i.e., stack output) voltage level (24 V). This converter senses the output voltage of the FC stack and activates only when a sudden dip in the stack voltage occurs due to load transient.

A. Operating Modes of the HF Converter and the AC/AC Cycloconverter

Fig. 4 shows the operating modes and schematic waveforms for the HF converter and the ac/ac cycloconverter for a positive



Fig. 3. (a) System schematic, (b) key waveforms, and (c) energy-flow diagrams for the FC power-conversion system.

transformer primary current. For a positive primary current, the converter operation can be divided into five different modes, as described below. A similar five-mode set exists for a negative primary current. It is noted that, and as shown in Fig. 3(b), the ac/ac cycloconverter essentially unfolds the transformer output generated by the HF converter. For unity power factor operation, this essentially translates to only flipping the negative signals of the sinusoidally encoded bipolar



Fig. 4. (a)-(e) Topologies and (f) waveforms corresponding to the five operating modes of the dc/ac converter for positive primary current.

signals generated by the HF converter in the positive half of a output cycle; while in the negative half of a output cycle flipping the positive signals thereby creating an overall sinuoidally modulated inverter output that is positive or zero in the positive line cycle and negative or zero in the negative line cycle. *Mode 1 [Fig. 4(a)]:* During this mode switches Q_{11} and Q_{21} of the FB converter are ON and the transformer primary current I_{p1} is positive. The output current I_{out} is positive and flows through the bidirectional switch pair S1–S1' and S2–S2' and the output filter. Switches Q_{31} , Q_{41} , S3–S3', and S4–S4' are OFF during this interval.

Mode 2 [Fig. 4(b)]: At the beginning of this interval the gate voltage of switch Q_{11} undergoes a high-to-low transition. As a result, the output capacitance of Q_{11} begins to accumulate charge and at the same time the output capacitance of switch Q_{41} begins to discharge through the external fly capacitor. Once the voltage across Q_{41} goes to zero, it is turned ON under ZVS. The transformer primary current I_{p1} and the output current I_{out} continue to flow in the same direction. Switch Q_{21} and the bidirectional switch pair S1–S1' and S2–S2' are ON, while the switches Q_{31} , Q_{41} , S3–S3', and S4–S4' are OFF. This mode ends when the switch Q_{11} is completely turned OFF and its output capacitance is charged to the FC stack voltage.

Mode 3 [Fig. 4(c)]: This mode starts with the complete turn-OFF of switch Q_{11} . The transformer primary current I_{p1} is still positive, and free wheels through the diode Q_{41} and Q_{21} . In addition, the output current continues to flow in the same direction as before. This mode ends at the commencement of turn-OFF of switch Q_{21} .

Mode 4 [Fig. 4(d)]: At the beginning of this interval the gate voltage of switch Q_{21} undergoes a high-to-low transition. As a result, the output capacitance of Q_{21} begins to accumulate charge and at the same time the output capacitance of switch Q_{31} begins to discharge. The charging current of Q_{21} and discharging current of Q_{31} together add up to the primary current I_{p1} . The transformer current makes a transition from positive-to-negative. Once the voltage across Q_{31} goes to zero, it is turned ON under ZVS. The output current flows in the same direction as before, but makes a rapid transition from the bidirectional switches S1-S1' and S2-S2' to S3-S3' and S4-S4', and during this process, Iout splits between both the transformer secondaries and flows through both the bidirectional switches. This mode ends when the switch Q_{21} is completely turned OFF and its output capacitance is charged to the FC stack voltage.

Mode 5 [Fig. 4(e)]: This mode starts with the complete turn-OFF of switch Q_{21} . The primary current I_{p1} is negative, while the output current is positive.

A low-cost phase-shift pulsewidth modulation controller UCC3895 (which implements control of the HF converter by phase shifting the switching of one of the legs with respect to the other leg of the FB) is employed [Fig. 5(a)]. A single master control signal drives all the HF-converter modules for synchronization. By allowing controllable dead times between the switching of the top and bottom devices of each leg, it allows resonant ZVS capabilities [26]. Mazumder et al. [26] also outline analytically the issues related to transformer leakage inductance including duty-cycle loss, ZVS range, and device stress that are not repeated in this paper. The line-frequency-modulating signals for the ac/ac cycloconverter switches are generated by a zero-crossing detector circuit (which compares the bipolar sine wave with



Fig. 5. Schematic of the controllers for (a) inverter and (b) energy-buffering boost converter unit.



Fig. 6. Comparison of gate charge and ON-resistance among different power devices of similar ratings (80-100 V, $\sim40-50$ A) demonstrates the rationale for selecting DirectFET.

the ground level and generates square wave output depending on the polarity of the sine wave). Current-mode controller is used for the boost converter in the energy buffering unit and is shown in Fig. 5(b).

III. DESIGN METHODOLOGY

A. Selection of Power Devices

DirectFET was chosen as the switching devices because of their extremely low gate charge and low ON-state resistance (see Fig. 6). Although DirectFET has a low ON-state resistance of ~15 m Ω , the conduction loss for a single device while conducting rated current (~30-A rms) is significant. Therefore, each switch of the FB converter was designed as a parallel combination of multiple such devices. The choice of the switching devices for the ac/ac cycloconverter is critically important because of the large voltage and current stresses handled by the circuit. For instance, to generate 110 V output rms, the minimum nominal voltage stress would be >200 V across each device. However, due to the presence of voltage spike at the secondary of the transformer (due to resonance between the leakage inductance of the transformer and the device output capacitance of the HF converter), the peak voltage stress was estimated to be >500 V. Devices with higher breakdown voltage, therefore, must be used. However, high voltage rated devices, especially power MOSFETs, generally exhibit large ON-state resistance, thereby leading to high conduction loss. However, because the line-frequency operation of the ac/ac cycloconverter switches does not pose any significant requirement on the switching speed, device with low conduction loss has been selected along with external antiparallel diode which switches at twice the frequency of the HF converter. For the diode, a combination of factors such as forward conduction drop, reverse-recovery charge and time, and breakdown voltage needs to be considered. We explored the possibility of using Schottky diodes, which has almost zero reverse-recovery charge to reduce the switching loss at HF. Because there exists no commercial Si Schottky diode with such high blocking voltage rating, GaAs Schottky diode (part# DGSS-20-06CC) has been used.

B. Transformer Design

Proper choice of transformer leakage inductance is critical for an efficient inverter design. The effects of the leakage inductance on the losses of the FC inverter are summarized as follows.

- 1) Conduction losses of the power devices and the transformer increase with an increase in the leakage inductance because of the corresponding increase in duty-ratio loss [8].
- Switching losses of the HF converter decrease with increasing in the leakage inductance due to an increase in ZVS range [8].
- 3) Switching losses of the ac/ac cycloconverter diodes (connected antiparallel to the controlled device) decrease with an increase in the leakage inductance as the peak reverse current of the diodes decreases [8].

Therefore, to achieve higher efficiency, the leakage inductance of the transformer has to be properly optimized. In addition, an interaction between the leakage inductance and the parasitic capacitances of DirectFET devices results in voltage spike across the device during turn-OFF. Lowering the overall parasitic inductance (including trace inductance and leakage) reduces the device stress. Moreover, to ensure that the secondary voltage is not distorted, the duty-ratio losses of all the modules (and hence, the leakage inductances of the transformers) need to be closely matched. Choice of planar transformer serves the dual purpose of low and uniform leakage and compact and lightweight sizing. Following [26], Fig. 7 shows the total estimated power loss of the overall inverter as a function of the transformer primary leakage inductance for different load power factors. Power loss increases with the increasing reactive power given higher circulating/reactive current. With regard to leakage inductance, power loss increases at lower inductances, since



Fig. 7. Total power loss as a function of transformer primary leakage inductance for various load power factors.



Fig. 8. Experimentally emulated FC characteristics.

ZVS effectiveness reduces; while power loss also increases at higher inductances due to a reduction in effective duty cycle [26] that needs to be compensated leading to higher switch ON state time and conduction loss.

C. Input Filter Design

An FC stack can be modeled as a current-dependent voltage source and the equivalent area-specific-resistance (ASR) can be calculated from experimentally measured characteristics. Using a resistor in series with a constant voltage source, we can emulate the behavior of the stack. The experimentally measured characteristics are shown in Fig. 8.

When no active/passive input filter is used, we obtain the following equation describing instantaneous FC current:

$$I_{\rm FC} = \frac{V_{\rm OC}}{2R_{\rm ASR}} \\ \pm \frac{\sqrt{V_{\rm OC}^2 - 4R_{\rm ASR} \left(\frac{V_m I_m}{2\eta} [\cos(\phi) - \cos(2\omega t + \phi)]\right)}}{2R_{\rm ASR}}$$
(1)

where R_{ASR} is ASR of FC stack, V_{OC} is stack open-circuit voltage, V_m and I_m are inverter output peak voltage and current, φ is power factor angle, and η is inverter efficiency.



Fig. 9. Estimated monetary gains and total area savings of the FC energy system with variation of the input capacitor and the optimal range.



(c)

Fig. 10. (a) Experimental prototype of the FC power-electronics system with energy buffering unit. (b) DirectFET-based compact HF converter board layout and a compact planar HF transformer (compared with a conventional transformer). (c) Test setup of the inverter with a planar SOFC stack.

From (1), we observe that for nonunity power factor, the current drawn from the FC could be negative. Because the FC cannot support such a current, an input filter is required to support nonunity power factors. If a capacitor (C) is used



Fig. 11. Operating signals of the FB converter and the cycloconverter.

as the input filter, the output voltage of the FC (V_{FC}) is given by the following nonlinear differential equation:

$$-V_{\rm FC}\frac{dV_{\rm FC}}{dt} - \frac{V_{\rm FC}^2}{CR_{\rm ASR}} + \frac{V_{\rm FC}V_{\rm OC}}{CR_{\rm ASR}} - \frac{V_m I_m}{2C\eta} \times [\cos(\phi) - \cos(2\omega t + \phi)] = 0.$$
(2)

We numerically solve (2) to calculate the FC current ripple and relate it to the FC-stack efficiency. Even for unity power factor, the power-electronic system draws a low-frequency current ripple from the FC in addition to the dc current. To provide this current, the FC stack has to be significantly oversized. The stack size can be substantially reduced by allowing the low-frequency current to flow through the input filter capacitor. This leads to higher stack efficiency by reducing ripple percentage, which effectively translates into cost saving on stack [8]. However, this comes at the cost of increasing the component cost and foot-print area of the power electronics. Based on the DOE specification of SOFC stack cost (\$400/kW) [27], we calculate the monetary gain achievable by increasing filter capacitor size and the total foot-print area (sum of stack and converter area) to determine the optimum range of input filter size (Fig. 9).

IV. EXPERIMENTAL RESULTS

The experimental prototype of the proposed HF inverter and the energy buffering unit is shown in Fig. 10 with the following parameters: 1) output power of 3 kW; 2) output voltage of 110 V (rms); 3) 35 A (rms) rated load current;



Fig. 12. Experimental results illustrating (a) output voltage and current of the inverter operating at an output power of 2 kW and input voltage of 28 V and (b) variation of THD with power levels.



Fig. 13. Efficiency of the HF inverter.

4) line frequency of 60 Hz; 5) switching frequency of 0.2 MHz; and 6) filter inductance and capacitance of 500 μ H and 5 μ F, respectively. As shown in Fig. 10(b), the HF operation yields a compact planar transformer (with low leakage inductance), which due to modular HF converter, has a multiplicative reduction in size and a compact output filter.

Fig. 11 shows the gate signals of the FB converter and the cycloconverter. The small dead-time between the switching of the switches in each leg ensures that there is no shoot-through problem due to a short across the FB input. In addition, the dead-time is necessary to ensure ZVS turn-ON of the FB switches. Cycloconverter switches operate at line frequency, thereby minimizing switching losses. Fig. 12(a) shows the output voltage and current waveforms of the inverter



Fig. 14. Experimental results illustrating the performance of the energy buffering unit during load transients.

operating with a resistive load. The variation of the totalharmonic distortion (THD) of the output voltage with output power is shown in Fig. 12(b). The proposed inverter operates within desired THD bounds (<5%) as per the IEEE standards.

The efficiency of the HF inverter, as a function of the output power, is shown in Fig. 13. Design 1 is based on DirectFET-based inverter. Changes made in the Design 2 are the introduction of low-leakage HF transformer and GaAs Schottky diode and they improved the overall efficiency of the inverter as can be seen from Fig. 13. The breakdown of the component losses of the inverter as a function of the total loss at rated power is approximately as follows: 1) HF-converter's MOSFET conduction and switching losses (14% and 7.6%, respectively); 2) ac/ac converter's MOSFET conduction loss (22%); 3) diode conduction and switching losses (22% and 6.3%, respectively); 4) transformer's copper and core losses (9% and 6.8%, respectively); 5) loss in snubbers placed across the drain and source of the MOSFETs (7.6%); and 6) output filter loss (4.7%).

Fig. 14 shows the performance of the energy buffering unit during a load transient from 1.5 to 2 kW and vice versa with the boost converter providing or absorbing the 500 W. The energy buffering unit takes a finite amount of time to respond to the load transient. This results in a sharp drop in the inverter input voltage when the load transient is initiated before it recovers back to the operating voltage level, as shown

in Fig. 14. The reason the FC stack voltage does not normalize after the transient is because of the lack of availability of a balance of power systems for the FC stack.

V. CONCLUSION

In this paper, the design guideline for a high-power density modular inverter for low-voltage and high-current FC stack applications is presented. Such a direct-powerconversion inverter can lead to savings in volume and weight due to HF operation. A guideline to determine the optimal size of the input filter is outlined from the standpoint of FC-energy-system cost. It is also illustrated that, for such a topology, an optimal choice of transformer leakage inductance is necessary to achieve low power loss and establish a balance between efficiency and reliability. This is achieved using a planar transformer design. Further, to reduce the device losses for the isolated two-stage inverter, DirectFET devices (with low-ON resistance and gate charge) are used for the primary-side HF inverter; while line-frequency-switched devices (with low forward drop) along with high-voltage reduced-recovery GaAs Schottky diodes are used for the secondary-side ac/ac cycloconverter. Transient in load demands, which may jeopardize the FC stack reliability, is handled through a (low-voltage and low-cost) batterysourced energy-buffering unit. Because of the voltage-level mismatch between the commercially available battery source and the FC stack rating, boost converter is used for the energy buffering. Experimental results demonstrating the nominal operations of inverter and energy buffering unit are presented.

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A DirectFET-Based High-Frequency Fuel-Cell Inverter

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Abstract—In this paper, the design guideline for a highpower-density inverter for fuel-cell (FC) applications is presented. Such an inverter can lead to savings in volume and weight due to high-frequency operation. In addition, we present a guideline to determine the optimal size of the input filter. It is also illustrated that, for such a topology, an optimal choice of transformer leakage inductance is necessary to achieve low power loss and to establish a balance between efficiency and reliability. Transient load condition, which may degrade FC-stack reliability, is handled through a battery-sourced energy-buffering unit. Experimental results demonstrating the nominal operations of inverter and energy buffering unit are presented.

Index Terms—Cycloconverter, energy buffering, fuel cell (FC), GaAs Schottky diode, high frequency (HF), inverter, planar transformer, power density.

I. INTRODUCTION

S. DEPARTMENT of Energy (DOE) has recently emphasized the need for near-zero-emissions and ultrahigh-efficiency technologies for electric power generation. These environmental characteristics are inherent in fuelcell (FC) systems [1]. Electric power generation is emerging as the first large-scale commercial application for FCs and will account for more than half of related global product and service demand by 2014, according to U.S. FC Council. This application area is also one of the centerpiece emerging energy technologies to address the mounting crisis resulting from total dependence on existing fossil-fuel-energy systems. In [2], an outline of the market share of the promising FC technology applications poised for rapid growth is outlined. The framework for integrating these advanced power generation sources with the existing stationary energy infrastructure has been provided by the concept of a microgrid [3], [4], which is intrinsically linked to the burgeoning concept of distributed generation (DG). Apart from DG, the compact FC energy systems are also very attractive solutions for automotive applications and this market is expected to grow significantly in the next few years [5].

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Technology development in power electronics plays a crucial role in improving various stationary and automotive system performances, which will further drive their penetration into the electricity and vehicular markets [2]. However, viable application of FC energy sources for these wide-ranging applications requires the development of power-electronic systems to convert FC's variable dc output voltage to commercial ac output that meet the following requirements [6]: 1) low cost; 2) high energy efficiency; 3) high reliability; and 4) high power density. During recent times, several power-electronicsystem topologies, which address one or more of the above factors, have been proposed [7]-[20]. For instance, in [13], a hybrid FC system comprising an auxiliary battery buffer is outlined. However, it interfaces to a monolithic stack, and the nonmodular inverter, apart from being a three-level system, requires a dc-link capacitor. The latter is also a requirement for a FC inverter system outlined in [14]. In [15], an interesting FC and battery-based isolated inverter system is proposed. However, it needs a dc-link capacitor and it will be fed by a monolithic stack because of the nonmodular topology of the inverter. In [16], a modular full-bridge (FB)-based inverter, similar to that proposed in [17] (which forms the basis of this paper), is proposed. However, integration of the battery buffer is not outlined. Similar primary-side FB converter modularity is demonstrated in [18]; however, this paper limits to an isolated dc/dc converter only and does not include the energy buffer. Mazumdar et al. [19] outline a two-stage inverter with the second-stage cycloconverter demonstrating line-frequency switching but subject to diode reverse recovery. However, the primary-side converter is nonmodular and the operating frequency is much lower than that pursued in this paper. In addition, the integration of energy buffering has not been considered. In this paper, we present the design of a high-energy density FC power-electronic system (Fig. 1) with a modular converter architecture consisting of a highfrequency (HF) inverter followed by a forced cycloconverter.

Another important issue for FC power-conversion systems is the selection of the rating of the FC stack. At present, no widely accepted output voltage rating for the FC stack has been established as an industry standard. High input voltage designs require a large number of cells. The failure or poor performance of any one cell can result in the failure of the entire stack. As stack height (cell count) increases, there is an increasing probability of least one cell causing the entire stack to fail. This effect is shown in Fig. 1 [21] for Solid oxide fuel cell (SOFC). In general, the rated output voltage of a stack decreases over time through various cell degradation mechanisms [22], [23]. FC system developers, recognizing

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Fig. 1. Binomial distribution effect of SOFC cell count on stack yield.



Fig. 2. Left: joined stack array designs for tall FC stacks [24]. Right: modular stacks of a planar SOFC.

that this dilemma (tall stacks needed for high voltage versus increasing failure probability with stack height) impacts both cost (yield) and reliability, have attempted to mitigate this effect by creating designs which attempt to provide parallel connection of multiple cells within the stacks and multiple parallel stacks for power scaling, as shown in Fig. 2.

Such a low-voltage and high-current energy source creates several challenges for power-electronics design: 1) mitigate conduction loss due to high source current for a given load demand and 2) boost low input voltage without encountering instability (e.g., for a front-end dc/dc boost converter) or reliability (e.g., for an isolated FB converter that has to deal with large turns ratio and possibly transformer leakage inductance leading to higher voltage spikes and losses in the power devices). This paper, therefore, discusses power-electronics-design strategies particularly for a low-voltage, high current FC-stack output.

A final design issue is related to handling the reflected inverter low-frequency ripple current, which can degrade the efficiency and life of the FC stack [22]. For single-phase inverter applications, the peak current drawn from the stack is double for unity-power-factor passive loads and even larger for passive reactive loads compared with the average dc current [8]. For harmonic loads, the ripple depends on the load power factor and the harmonic content of the load current [22]. Overall, to handle such current ripples, the stack has to be significantly oversized, which increases the installation and operating costs. Typically, capacitive filter solutions are used to limit the low-frequency current drawn from the stack. In this paper, we present a design guideline to choose the optimum size of a capacitive input filter from the standpoints of the overall system energy density and cost.

II. SYSTEM DESCRIPTION AND OPERATION

The overall dc-link capacitor-less power-electronic system [Fig. 3(a)] consists of four HF phase-shifted zero-voltageswitched (ZVS) FB converters (connected in parallel at the input) and a single line-frequency ac/ac cycloconverter [8] followed by an *LC* filter [Fig. 3(a)]. Because of lowinput voltage, current handled by the primary-side devices is significantly high leading to higher conduction and switching losses. To reduce loss, this topology consists of parallel modules on the primary side. Such an arrangement also results in individual transformers with lower turns-ratio, thereby reducing the leakage inductance for each of them. To provide the desired bus voltage for generating a 110 V/60-Hz output, the secondaries of the transformers are connected in series.

The switches of the HF converter are sinusoidally modulated based on the output of a voltage-mode controller. For high-energy density, we operate the converter at high switching frequencies (reducing the size and weight of the magnetic components). While being advantageous from the energy density point of view, HF operation also leads to the increased switching losses. To address this issue, we use surface-mount power MOSFETs (i.e., DirectFET [25]) for the HF converter, which have significantly low conduction and switching losses compared with the conventional power MOSFETs. Because the switches for ac/ac cycloconverter operate at line frequency, their switching losses are minimal.

An energy-buffering unit is used to provide the additional energy requirements during load transients, as shown in Fig. 3(c). This unit provides the additional energy to the load during the short period of high energy demand, and then automatically shuts off when the air and fuel flow rates for the FC stack readjusts to new load demand. A four-module basic dc/dc boost converter is used to step up the battery output voltage (12 V) to the rated bus (i.e., stack output) voltage level (24 V). This converter senses the output voltage of the FC stack and activates only when a sudden dip in the stack voltage occurs due to load transient.

A. Operating Modes of the HF Converter and the AC/AC Cycloconverter

Fig. 4 shows the operating modes and schematic waveforms for the HF converter and the ac/ac cycloconverter for a positive



Fig. 3. (a) System schematic, (b) key waveforms, and (c) energy-flow diagrams for the FC power-conversion system.

transformer primary current. For a positive primary current, the converter operation can be divided into five different modes, as described below. A similar five-mode set exists for a negative primary current. It is noted that, and as shown in Fig. 3(b), the ac/ac cycloconverter essentially unfolds the transformer output generated by the HF converter. For unity power factor operation, this essentially translates to only flipping the negative signals of the sinusoidally encoded bipolar



Fig. 4. (a)-(e) Topologies and (f) waveforms corresponding to the five operating modes of the dc/ac converter for positive primary current.

signals generated by the HF converter in the positive half of a output cycle; while in the negative half of a output cycle flipping the positive signals thereby creating an overall sinuoidally modulated inverter output that is positive or zero in the positive line cycle and negative or zero in the negative line cycle. *Mode 1 [Fig. 4(a)]:* During this mode switches Q_{11} and Q_{21} of the FB converter are ON and the transformer primary current I_{p1} is positive. The output current I_{out} is positive and flows through the bidirectional switch pair S1–S1' and S2–S2' and the output filter. Switches Q_{31} , Q_{41} , S3–S3', and S4–S4' are OFF during this interval.

Mode 2 [Fig. 4(b)]: At the beginning of this interval the gate voltage of switch Q_{11} undergoes a high-to-low transition. As a result, the output capacitance of Q_{11} begins to accumulate charge and at the same time the output capacitance of switch Q_{41} begins to discharge through the external fly capacitor. Once the voltage across Q_{41} goes to zero, it is turned ON under ZVS. The transformer primary current I_{p1} and the output current I_{out} continue to flow in the same direction. Switch Q_{21} and the bidirectional switch pair S1–S1' and S2–S2' are ON, while the switches Q_{31} , Q_{41} , S3–S3', and S4–S4' are OFF. This mode ends when the switch Q_{11} is completely turned OFF and its output capacitance is charged to the FC stack voltage.

Mode 3 [Fig. 4(c)]: This mode starts with the complete turn-OFF of switch Q_{11} . The transformer primary current I_{p1} is still positive, and free wheels through the diode Q_{41} and Q_{21} . In addition, the output current continues to flow in the same direction as before. This mode ends at the commencement of turn-OFF of switch Q_{21} .

Mode 4 [Fig. 4(d)]: At the beginning of this interval the gate voltage of switch Q_{21} undergoes a high-to-low transition. As a result, the output capacitance of Q_{21} begins to accumulate charge and at the same time the output capacitance of switch Q_{31} begins to discharge. The charging current of Q_{21} and discharging current of Q_{31} together add up to the primary current I_{p1} . The transformer current makes a transition from positive-to-negative. Once the voltage across Q_{31} goes to zero, it is turned ON under ZVS. The output current flows in the same direction as before, but makes a rapid transition from the bidirectional switches S1-S1' and S2-S2' to S3-S3' and S4-S4', and during this process, Iout splits between both the transformer secondaries and flows through both the bidirectional switches. This mode ends when the switch Q_{21} is completely turned OFF and its output capacitance is charged to the FC stack voltage.

Mode 5 [Fig. 4(e)]: This mode starts with the complete turn-OFF of switch Q_{21} . The primary current I_{p1} is negative, while the output current is positive.

A low-cost phase-shift pulsewidth modulation controller UCC3895 (which implements control of the HF converter by phase shifting the switching of one of the legs with respect to the other leg of the FB) is employed [Fig. 5(a)]. A single master control signal drives all the HF-converter modules for synchronization. By allowing controllable dead times between the switching of the top and bottom devices of each leg, it allows resonant ZVS capabilities [26]. Mazumder et al. [26] also outline analytically the issues related to transformer leakage inductance including duty-cycle loss, ZVS range, and device stress that are not repeated in this paper. The line-frequency-modulating signals for the ac/ac cycloconverter switches are generated by a zero-crossing detector circuit (which compares the bipolar sine wave with



Fig. 5. Schematic of the controllers for (a) inverter and (b) energy-buffering boost converter unit.



Fig. 6. Comparison of gate charge and ON-resistance among different power devices of similar ratings (80-100 V, $\sim40-50$ A) demonstrates the rationale for selecting DirectFET.

the ground level and generates square wave output depending on the polarity of the sine wave). Current-mode controller is used for the boost converter in the energy buffering unit and is shown in Fig. 5(b).

III. DESIGN METHODOLOGY

A. Selection of Power Devices

DirectFET was chosen as the switching devices because of their extremely low gate charge and low ON-state resistance (see Fig. 6). Although DirectFET has a low ON-state resistance of ~15 m Ω , the conduction loss for a single device while conducting rated current (~30-A rms) is significant. Therefore, each switch of the FB converter was designed as a parallel combination of multiple such devices. The choice of the switching devices for the ac/ac cycloconverter is critically important because of the large voltage and current stresses handled by the circuit. For instance, to generate 110 V output rms, the minimum nominal voltage stress would be >200 V across each device. However, due to the presence of voltage spike at the secondary of the transformer (due to resonance between the leakage inductance of the transformer and the device output capacitance of the HF converter), the peak voltage stress was estimated to be >500 V. Devices with higher breakdown voltage, therefore, must be used. However, high voltage rated devices, especially power MOSFETs, generally exhibit large ON-state resistance, thereby leading to high conduction loss. However, because the line-frequency operation of the ac/ac cycloconverter switches does not pose any significant requirement on the switching speed, device with low conduction loss has been selected along with external antiparallel diode which switches at twice the frequency of the HF converter. For the diode, a combination of factors such as forward conduction drop, reverse-recovery charge and time, and breakdown voltage needs to be considered. We explored the possibility of using Schottky diodes, which has almost zero reverse-recovery charge to reduce the switching loss at HF. Because there exists no commercial Si Schottky diode with such high blocking voltage rating, GaAs Schottky diode (part# DGSS-20-06CC) has been used.

B. Transformer Design

Proper choice of transformer leakage inductance is critical for an efficient inverter design. The effects of the leakage inductance on the losses of the FC inverter are summarized as follows.

- 1) Conduction losses of the power devices and the transformer increase with an increase in the leakage inductance because of the corresponding increase in duty-ratio loss [8].
- Switching losses of the HF converter decrease with increasing in the leakage inductance due to an increase in ZVS range [8].
- Switching losses of the ac/ac cycloconverter diodes (connected antiparallel to the controlled device) decrease with an increase in the leakage inductance as the peak reverse current of the diodes decreases [8].

Therefore, to achieve higher efficiency, the leakage inductance of the transformer has to be properly optimized. In addition, an interaction between the leakage inductance and the parasitic capacitances of DirectFET devices results in voltage spike across the device during turn-OFF. Lowering the overall parasitic inductance (including trace inductance and leakage) reduces the device stress. Moreover, to ensure that the secondary voltage is not distorted, the duty-ratio losses of all the modules (and hence, the leakage inductances of the transformers) need to be closely matched. Choice of planar transformer serves the dual purpose of low and uniform leakage and compact and lightweight sizing. Following [26], Fig. 7 shows the total estimated power loss of the overall inverter as a function of the transformer primary leakage inductance for different load power factors. Power loss increases with the increasing reactive power given higher circulating/reactive current. With regard to leakage inductance, power loss increases at lower inductances, since



Fig. 7. Total power loss as a function of transformer primary leakage inductance for various load power factors.





ZVS effectiveness reduces; while power loss also increases at higher inductances due to a reduction in effective duty cycle [26] that needs to be compensated leading to higher switch ON state time and conduction loss.

C. Input Filter Design

An FC stack can be modeled as a current-dependent voltage source and the equivalent area-specific-resistance (ASR) can be calculated from experimentally measured characteristics. Using a resistor in series with a constant voltage source, we can emulate the behavior of the stack. The experimentally measured characteristics are shown in Fig. 8.

When no active/passive input filter is used, we obtain the following equation describing instantaneous FC current:

$$I_{\rm FC} = \frac{V_{\rm OC}}{2R_{\rm ASR}} \\ \pm \frac{\sqrt{V_{\rm OC}^2 - 4R_{\rm ASR} \left(\frac{V_m I_m}{2\eta} [\cos(\phi) - \cos(2\omega t + \phi)]\right)}}{2R_{\rm ASR}}$$
(1)

where R_{ASR} is ASR of FC stack, V_{OC} is stack open-circuit voltage, V_m and I_m are inverter output peak voltage and current, φ is power factor angle, and η is inverter efficiency.



Fig. 9. Estimated monetary gains and total area savings of the FC energy system with variation of the input capacitor and the optimal range.



(c)

Fig. 10. (a) Experimental prototype of the FC power-electronics system with energy buffering unit. (b) DirectFET-based compact HF converter board layout and a compact planar HF transformer (compared with a conventional transformer). (c) Test setup of the inverter with a planar SOFC stack.

From (1), we observe that for nonunity power factor, the current drawn from the FC could be negative. Because the FC cannot support such a current, an input filter is required to support nonunity power factors. If a capacitor (C) is used



Fig. 11. Operating signals of the FB converter and the cycloconverter.

as the input filter, the output voltage of the FC (V_{FC}) is given by the following nonlinear differential equation:

$$-V_{\rm FC}\frac{dV_{\rm FC}}{dt} - \frac{V_{\rm FC}^2}{CR_{\rm ASR}} + \frac{V_{\rm FC}V_{\rm OC}}{CR_{\rm ASR}} - \frac{V_m I_m}{2C\eta} \times [\cos(\phi) - \cos(2\omega t + \phi)] = 0.$$
(2)

We numerically solve (2) to calculate the FC current ripple and relate it to the FC-stack efficiency. Even for unity power factor, the power-electronic system draws a low-frequency current ripple from the FC in addition to the dc current. To provide this current, the FC stack has to be significantly oversized. The stack size can be substantially reduced by allowing the low-frequency current to flow through the input filter capacitor. This leads to higher stack efficiency by reducing ripple percentage, which effectively translates into cost saving on stack [8]. However, this comes at the cost of increasing the component cost and foot-print area of the power electronics. Based on the DOE specification of SOFC stack cost (\$400/kW) [27], we calculate the monetary gain achievable by increasing filter capacitor size and the total foot-print area (sum of stack and converter area) to determine the optimum range of input filter size (Fig. 9).

IV. EXPERIMENTAL RESULTS

The experimental prototype of the proposed HF inverter and the energy buffering unit is shown in Fig. 10 with the following parameters: 1) output power of 3 kW; 2) output voltage of 110 V (rms); 3) 35 A (rms) rated load current;



Fig. 12. Experimental results illustrating (a) output voltage and current of the inverter operating at an output power of 2 kW and input voltage of 28 V and (b) variation of THD with power levels.



Fig. 13. Efficiency of the HF inverter.

4) line frequency of 60 Hz; 5) switching frequency of 0.2 MHz; and 6) filter inductance and capacitance of 500 μ H and 5 μ F, respectively. As shown in Fig. 10(b), the HF operation yields a compact planar transformer (with low leakage inductance), which due to modular HF converter, has a multiplicative reduction in size and a compact output filter.

Fig. 11 shows the gate signals of the FB converter and the cycloconverter. The small dead-time between the switching of the switches in each leg ensures that there is no shoot-through problem due to a short across the FB input. In addition, the dead-time is necessary to ensure ZVS turn-ON of the FB switches. Cycloconverter switches operate at line frequency, thereby minimizing switching losses. Fig. 12(a) shows the output voltage and current waveforms of the inverter



takes over and voltage increases

Fig. 14. Experimental results illustrating the performance of the energy buffering unit during load transients.

operating with a resistive load. The variation of the totalharmonic distortion (THD) of the output voltage with output power is shown in Fig. 12(b). The proposed inverter operates within desired THD bounds (<5%) as per the IEEE standards.

The efficiency of the HF inverter, as a function of the output power, is shown in Fig. 13. Design 1 is based on DirectFET-based inverter. Changes made in the Design 2 are the introduction of low-leakage HF transformer and GaAs Schottky diode and they improved the overall efficiency of the inverter as can be seen from Fig. 13. The breakdown of the component losses of the inverter as a function of the total loss at rated power is approximately as follows: 1) HF-converter's MOSFET conduction and switching losses (14% and 7.6%, respectively); 2) ac/ac converter's MOSFET conduction loss (22%); 3) diode conduction and switching losses (22% and 6.3%, respectively); 4) transformer's copper and core losses (9% and 6.8%, respectively); 5) loss in snubbers placed across the drain and source of the MOSFETs (7.6%); and 6) output filter loss (4.7%).

Fig. 14 shows the performance of the energy buffering unit during a load transient from 1.5 to 2 kW and vice versa with the boost converter providing or absorbing the 500 W. The energy buffering unit takes a finite amount of time to respond to the load transient. This results in a sharp drop in the inverter input voltage when the load transient is initiated before it recovers back to the operating voltage level, as shown in Fig. 14. The reason the FC stack voltage does not normalize after the transient is because of the lack of availability of a balance of power systems for the FC stack.

V. CONCLUSION

In this paper, the design guideline for a high-power density modular inverter for low-voltage and high-current FC stack applications is presented. Such a direct-powerconversion inverter can lead to savings in volume and weight due to HF operation. A guideline to determine the optimal size of the input filter is outlined from the standpoint of FC-energy-system cost. It is also illustrated that, for such a topology, an optimal choice of transformer leakage inductance is necessary to achieve low power loss and establish a balance between efficiency and reliability. This is achieved using a planar transformer design. Further, to reduce the device losses for the isolated two-stage inverter, DirectFET devices (with low-ON resistance and gate charge) are used for the primary-side HF inverter; while line-frequency-switched devices (with low forward drop) along with high-voltage reduced-recovery GaAs Schottky diodes are used for the secondary-side ac/ac cycloconverter. Transient in load demands, which may jeopardize the FC stack reliability, is handled through a (low-voltage and low-cost) batterysourced energy-buffering unit. Because of the voltage-level mismatch between the commercially available battery source and the FC stack rating, boost converter is used for the energy buffering. Experimental results demonstrating the nominal operations of inverter and energy buffering unit are presented.

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