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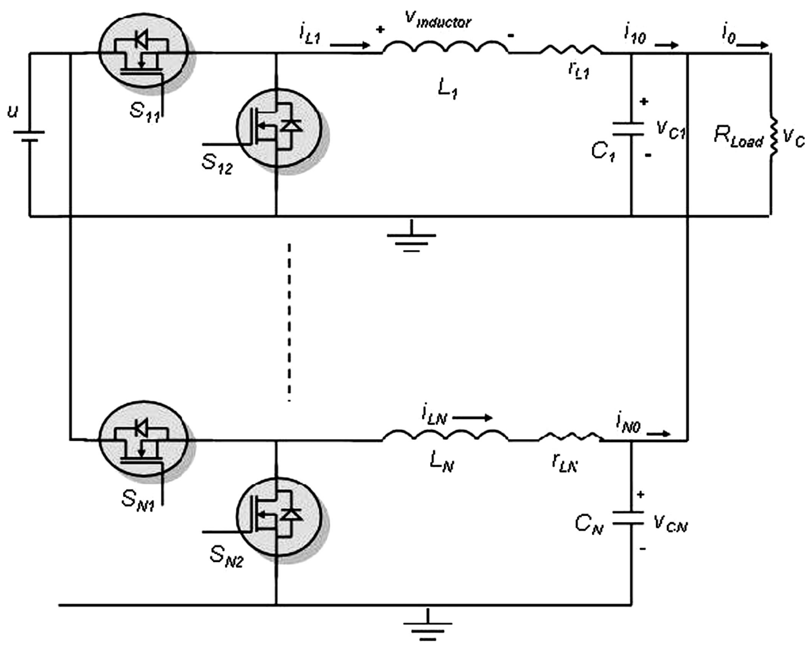
9.6 Nonlinear Control of Interactive Power-Electronics Systems

Sudip K. Mazumder

Introduction

Interactive power-electronics systems (IPNs), such as parallel DC–DC or parallel muniphase converters, are nonlinear hybrid dynamical systems [1,2]. The instability in such switching systems, owing to their discontinuity, can evolve on slow and fast scales. Conventional analyses of IPNs and their subsystems are based on averaged models, which ignore fast-scale instability and analyze the stability on a reduced-order manifold. As such, the validity of the averaged models varies with the switching frequency, even for the same topological structure. The prevalent procedure for analyzing the stability of IPNs and their subsystems is based on linearized averaged (small-signal) models that require a smooth averaged model. Yet there are systems (in active use) that yield a nonsmooth averaged model [2]. Even for systems for which smooth averaged model is realizable, small-signal analyses of the nominal solution/orbit do not provide anything about three important characteristics [1–3]: region of attraction of the nominal solution, dependence of the converter dynamics on the initial conditions of the states, and the postinstability dynamics. As such, conventional linear controllers for IPNs, designed based on small-signal analyses, may be conservative and may not be robust and optimal.



[AQ1] **FIGURE 9.65** A parallel DC-DC converter.

Clearly, there is a need to design nonlinear controllers for such hybrid systems, thereby achieving a wider stability margin, improved robustness against parametric variations, feedforward and feedback disturbances, switching nonlinearities, interactions, and enhanced performance.

Applications

Parallel dc–dc converter

Parallel DC-DC converters, as shown in Figure 9.65 are widely used in telecommunication power supplies [4–16]. They operate under closed-loop feedback control to regulate the bus voltage and enable load sharing [1, 4–16]. These closed-loop converters are inherently nonlinear systems. The major sources of nonlinearities are switching nonlinearity and interaction among the converter modules.[1] Yet, most conventional controllers for parallel DC–DC converters are linear. Recently, there have been many studies of the nonlinear control of standalone DC–DC converters [17–26], which have focused on variable-structure controllers (VSC) [27,28], Lyapunov-based controllers [29–33], feedback linearized and nonlinear H_∞ controllers [34–39], and fuzzy logic controllers [40–42]. However, there are few studies on the nonlinear control of parallel DC–DC converters where, unlike standalone converters, there is a strong interaction among the converter modules apart from the feedforward and feedback disturbances.

In Ref. 43, a fuzzy-logic compensator is proposed for the master–slave control of a parallel DC–DC converter. The controller uses a proportional-integral-derivative (PID) expert to derive the fuzzy inference rules; it shows improved robustness as compared to linear controllers. However, the control design is purely heuristic and the stability of the overall system has not been proven. In Ref. 44, a VSC has been developed for a

[1]The uniform distribution of power flow among the parallel connected converter modules is important for reasons of cost effectiveness and long term reliability. Parallel modules are not identical because of finite tolerances in power stage and control parameters. As a result the load current is not equally distributed among the modules, leading to excessive component stresses. Modules delivering higher currents will have a shorter lifetime and system reliability is degraded. Therefore, the control scheme should ensure equal distribution of power among the parallel connected converters.

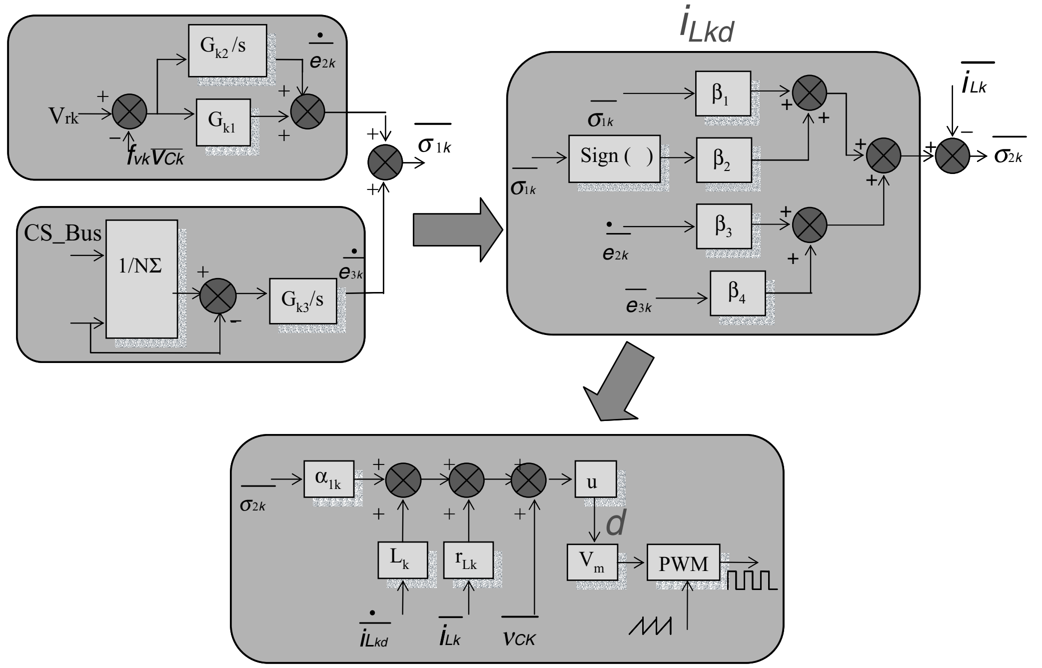


FIGURE 9.66 Methodology for duty-ratio ("d") and PWM signal generation using the nonlinear controller.

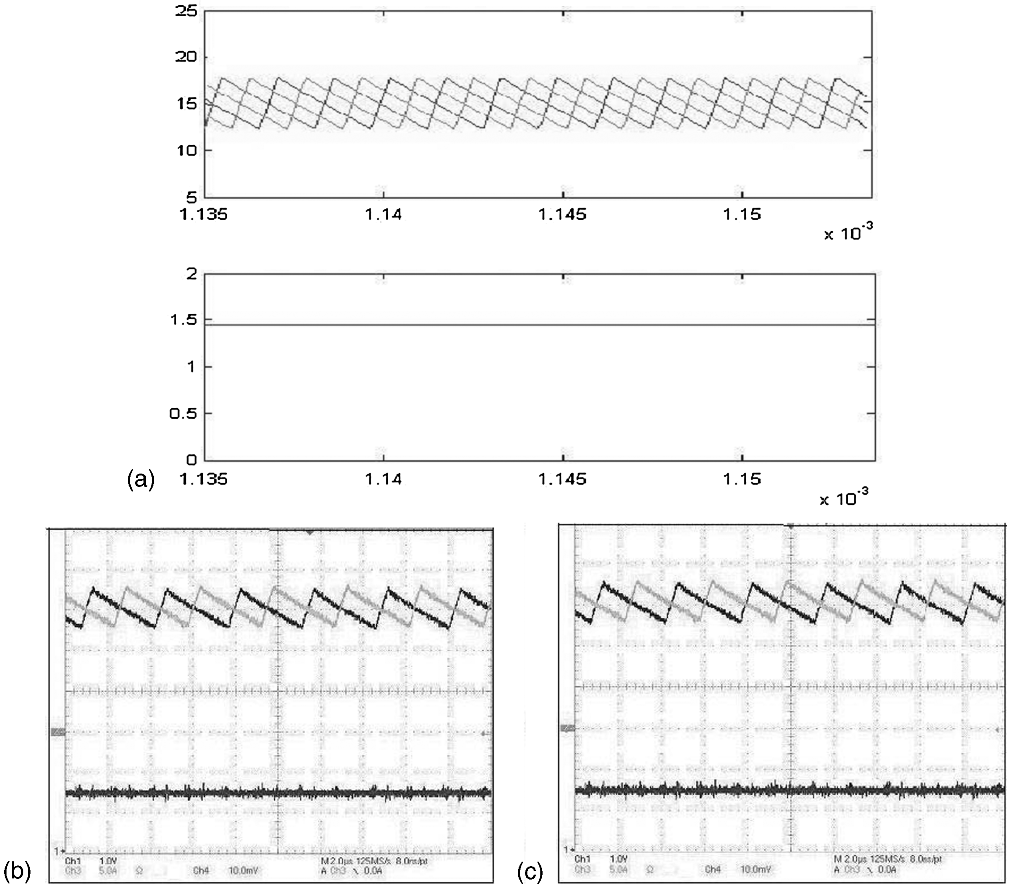
buck converter using interleaving. However, the interleaving scheme works only for three parallel modules. Besides, this paper gives no details regarding the existence and stability of the sliding manifolds.

In Ref. 45, Mazumder et al. have developed integral-variable-structure control (IVSC) schemes for N parallel DC–DC buck converters. The choice of a VSC is logical for power converters because the control and plant are both discontinuous. All of the nonlinear controllers mentioned earlier [21–26], which are not based on VSC, have completely relied on the smooth averaged models of the power converters. Therefore, control is valid only on a reduced-order manifold. The IVSC retains all of the properties of a VSC, that is, simplicity in design, good dynamic response, and robustness. In addition, the integral action of the IVSC eliminates the bus-voltage error and the error between the load currents of the converter modules under steady-state conditions. It also reduces the impact of very high-frequency dynamics due to parasitics on the closed-loop system.

Finally, when the error trajectories are inside the boundary layer[1] by modifying the control using the concepts of multiple-sliding-surface control (MSSC) [46,47] or the block-control principle [48,49], we are able to reject mismatched disturbances [50–53] and keep the steady-state switching frequency constant. This is achieved by calculating the duty ratio for each buck converter, as shown in Figure 9.66, "from a global stability" point of view (using Lyapunov's method). The error signals ensure that the output bus is regulated at a predetermined voltage reference while the load sharing among the N modules is maintained under transient and steady-state conditions. The fundamental difference in computing the duty ratio for the nonlinear controller and that for a conventional linear controller yields superior transient performance of the buck converter without compromising its steady-state performance [45]. This is because inside the boundary layer, using the duty ratio, one can implement PWM control as well as interleaving [45].

The results of an application of the nonlinear controller, for a four-phase voltage-regulated module (VRM) for next-generation Intel processor, are shown in Figure 9.67 through Figure 9.69. The power-stage

[1]The limits of this boundary layer correspond to the maximum and minimum values of a ramp of switching frequency f_s. At the beginning of each switching cycle, the mode of operation is determined by whether the trajectories are within the boundaries or outside.

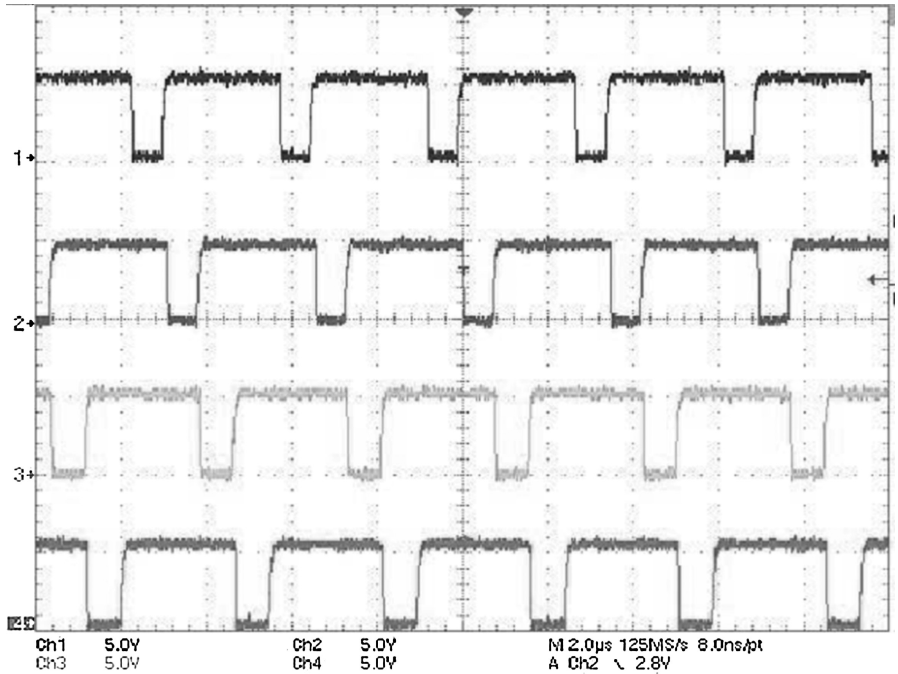


[AQ1] **FIGURE 9.67** Inductor currents in the four modules and the output voltage: (a) simulated; (b) experimental (modules 1 and 3), and (c) experimental (modules 2 and 4).

architecture of the VRM is the same as that shown in Figure 9.65. The VRM transient and steady-state specifications, which are "extremely stringent," are described in Table 9.1. Figure 9.67, shows the output voltage and the inductor currents in the four modules of the VRM, under steady-state conditions. The four inductor currents are interleaved, i.e., they differ in phase by 90°, which yields an output-ripple frequency four times that of the module switching frequency, thereby reducing the size of the output capacitor. The interleaving is also confirmed by the four equally-phase-shifted low-side gate-driver signals, as shown in Figure 9.68. Additionally, the VRM steady-state performance satisfies the stringent 2% tolerance. Finally, the transient performance of the VRM using the nonlinear controller is shown in Figure 9.69. The slew rate of the load transient is 50 A/microsecond. The results show that, even though the slew rate of the load transient is extremely fast, the nonlinear controller satisfies the VRM specifications in Table 9.1 during both no-load to full-load as well as *vice versa* conditions.

Parallel Multiphase Converter

Applications of parallel multiphase power converters are on the rise [54–65] because they provide several advantages including capability to handle high power, modularity, high reliability, less voltage or current ripple, and fast-dynamic response. Traditionally, a parallel multiphase converter either has a transformer at the ac side [57–59] or uses separate power supplies [56]. This approach, however, results in a bulky and expensive system because of the line-frequency transformer and the additional power supplies.

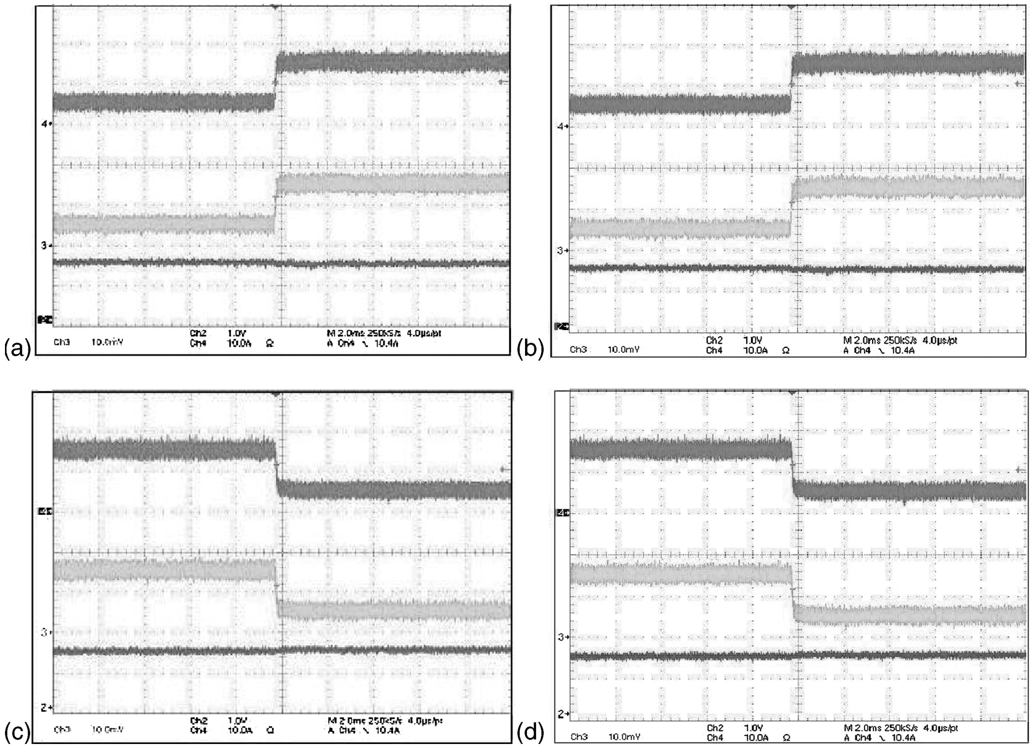


[AQ1] **FIGURE 9.68** Gate signals of the four VRM modules showing the equal-phase-shifted operation.

A recent approach to overcome these problems is to directly connect three-phase converters in parallel; one such system is shown in Figure 9.70. The parameters of the parallel three-phase boost rectifier (PTBR) are tabulated in Table 9.2. When two three-phase PWM modules are directly connected, circulating currents can exist in all of the phases [60,64,65], as shown in Figure 9.71(a) and Figure 9.71(b). Several methods have been proposed to reduce the cross-current among the modules. Using a linear controller and space-vector modulation (SVM) schemes, which do not use the zero vectors, Xing et al [60] have developed schemes for standardized three-phase modules to reduce the cross-current. The advantage of such schemes is that the communication between the modules is minimal. However, the transient response of the PTBR is not satisfactory and the magnitude of the zero-sequence current under steady-state conditions is not shown. Recently, Ye et al. [63] have proposed a linear control scheme[1], which is simple and minimizes the zero-sequence current under steady-state conditions by simply varying the duration of the zero space-vector. The steady-state performance of the PTBR using CS_{LINEAR} is shown in Figure 9.71(c). However, if the system saturates, the control scheme will not work effectively, even under steady-state conditions. This is because, when the system saturates, the zero vector can not be applied. Furthermore, the performance of the system under transient conditions has not been demonstrated [63].

Recently, three nonlinear control schemes were proposed by the author [64,65] to improve the transient performances of the PTBR as compared to those obtained using CS_{LINEAR}. The first two control schemes (CS_{CONT1} and CS_{CONT2}) are developed in the continuous domain, whereas the third scheme ($CS_{DISCRETE}$) is developed in the discrete domain. The former control schemes stabilize the errors on the *dq*-axis sliding surfaces and rely on blocking the pure zero-sequence current path, the inductor size, and the switching frequency to bind the errors on the zero-axis sliding surfaces. The steady-state ripple of the PTBR obtained using CS_{CONT2} is slightly better than that obtained using CS_{CONT1}, because the former uses a hysteretic comparator, which has an inner and an outer hysteretic band. The steady-state ripple of the PTBR obtained with $CS_{DISCRETE}$ is better than those obtained with the other two proposed control schemes because the

[1]In this chapter, we will refer to this control proposed by Ye et al. [63] as CS_{LINEAR}.



[AQ1] **FIGURE 9.69** Experimental inductor currents and the output voltage during a load transient Step-up load transient: (a) modules 1 and 3 and (b) modules 2 and 4. Step-down load transient: (c) modules 1 and 3 and (d) modules 2 and 4.

TABLE 9.1 Intel VRM 9.0 Design Guidelines

Electrical Specifications	Intel VRM 9.0 Design Guidelines
Output voltage	1.408 – 1.5 V (*our nominal reference: 1.45 V*)
Output current	60 A
No-load operation	Outputs ≤110% of the maximum value
Overshoot at turn-on/turn-off	Must be within 2% of the nominal output voltage set by VID code
Slew rate	50 A/μS
Current sharing	Should be accurate within 10% of the rated output current, except during initial power-up and transient responses

former combines SVM and nonlinear control, and stabilizes the zero-axis disturbance as well. Hence, the steady-state ripple has a constant frequency, and the deviation of the zero-axis current from its reference value (= 0) is minimized.

Figure 9.72, demonstrates the transient and steady-state performances of the PTBR using these three nonlinear control schemes. We also compare the performances of the three proposed controllers with the linear controller CS_{LINEAR}. We find that CS_{LINEAR} stabilizers the circulating current. However, its transient response is inferior to the proposed control schemes for even moderate feedforward and feedback disturbances. For even larger disturbances, the transient performance of the controller proposed by Ye et al. [63] suffers considerably.

Next, using Figure 9.73, we investigate the sharing of the line currents between M1 and M2, when the PTBR is subjected to a large disturbance in either the voltage (case 1) or the load (case 2). For case 1, we see that the best transient response is achieved using CS_{CONT1}; the response time is comparable to the other two

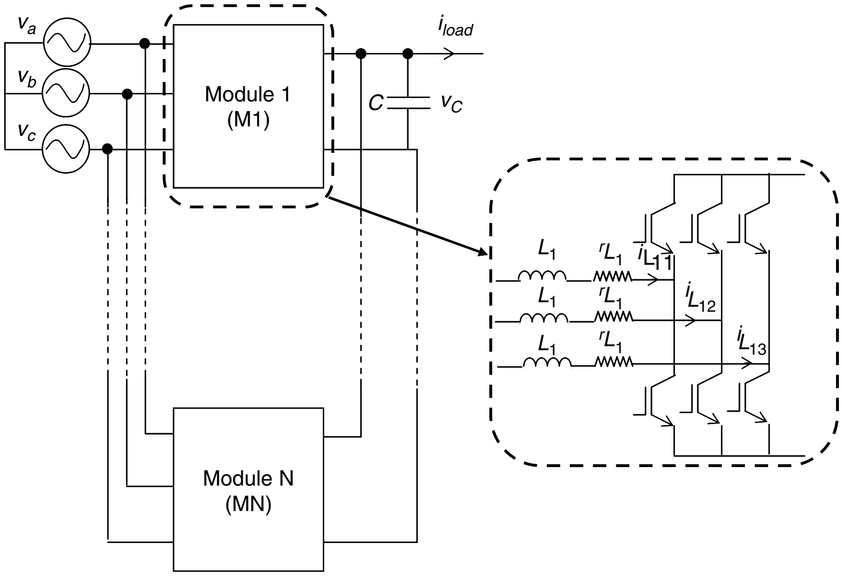


FIGURE 9.70 Schematic of a parallel three phase boost rectifier (PTBR) with N modules.

TABLE 9.2 Nominal Parameters of the PTBR

Parameter	Nominal Values
$v_{ab} = v_{bc} = v_{ca} = v_n$	208 V (rms)
v_C (regulated)	400 V
Nominal switching frequency (=1/T)	32 kHz
$L_1 = L_2 = L_n$	500 μH
$^rL_1 = {}^rL_2 = {}^rL_n$	0.5 Ω
Bus capacitance (C)	1200 μF
Load resistance (R)	4 Ω
Power ratings of M1 and M2	20 kVA

proposed schemes. The recovery time of the PTBR obtained with CS_{LINEAR} is the longest. Moreover, immediately after the change in the voltage, there is a undershoot and an overshoot in two of the phase currents, which are not evident in the responses obtained with the proposed control schemes. For case 2, among the three proposed control schemes, $CS_{DISCRETE}$ achieves the best compromise between the response time and current sharing. The recovery times of CS_{CONT1} and CS_{CONT2} are smaller than that of $CS_{DISCRETE}$. The response of the PTBR obtained with CS_{LINEAR} is significantly inferior to those obtained with the proposed control schemes, both in terms of the response time and current sharing.

Finally, in Figure 9.74, we show the impact of the proposed control schemes on the steady-state ripples of the phase currents (in the $\alpha\beta$ frame) and on the zero-axis current that circulates between the two modules. For all of these plots, we choose $L_1 = 0.85L_n$ and $L_2 = L_n$. All other parameters are kept the same as before. The steady-state ripple obtained with $CS_{DISCRETE}$ is better than those obtained using CS_{CONT1} and CS_{CONT2}. More importantly, the zero-axis current obtained with $CS_{DISCRETE}$ has a smaller magnitude compared to the previous cases. The steady-state results obtained using $CS_{DISCRETE}$ and CS_{LINEAR} are close. *Therefore, the nonlinear controller $CS_{DISCRETE}$ attains the best compromise between the dynamic- and steady-state performances.*

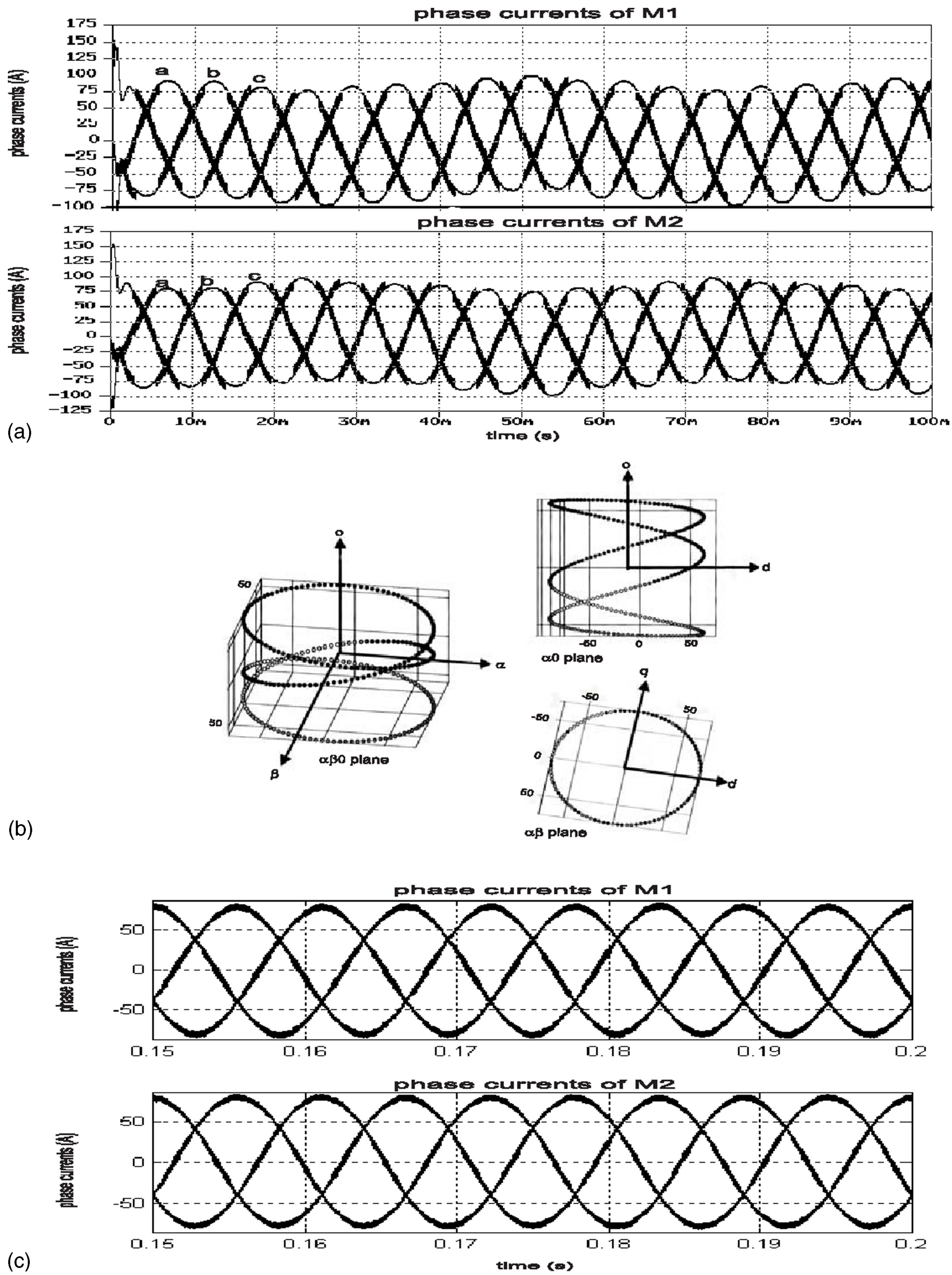
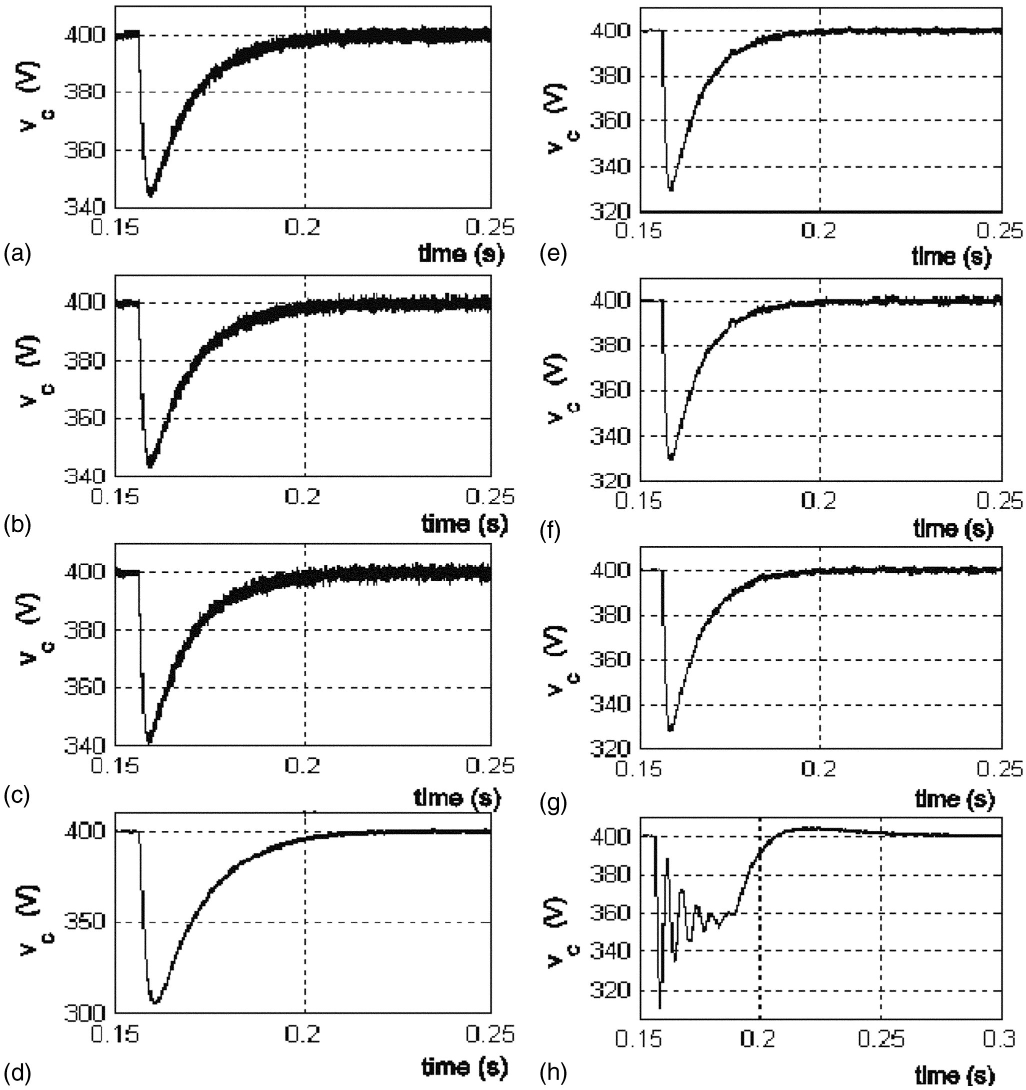


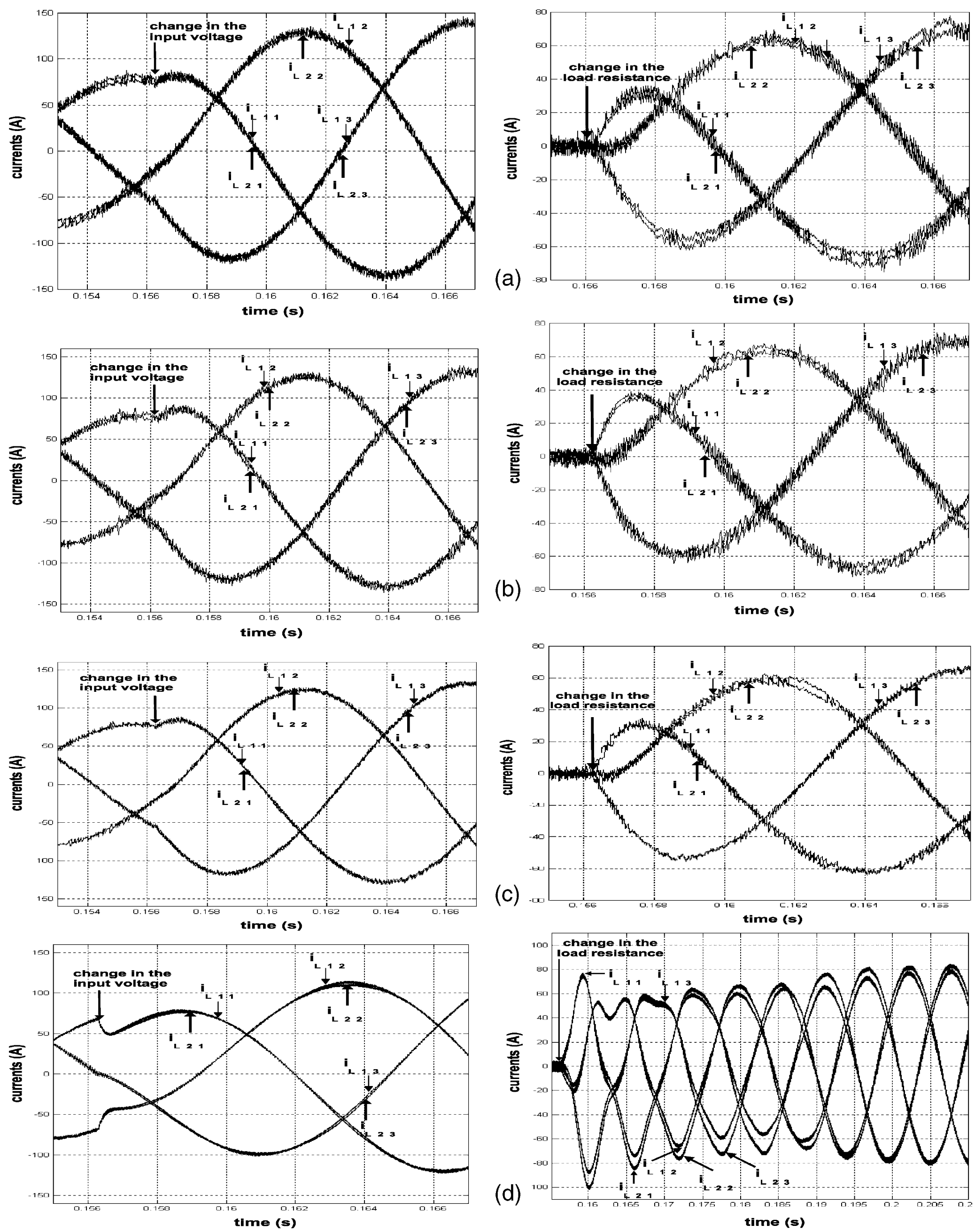
FIGURE 9.71 (a) The phase currents of M1 and M2, using a conventional *dq* controller, when the parameters of the modules are the same, except L_1 is 95% of L_2. The result shows the limitation of a conventional *dq* controller in ensuring even-load [AQ1] distribution when the two modules have parametric variations. (b) Three-dimensional view of the unbalanced phase currents of M1 in the $\alpha\beta o$ frame. It shows that a conventional *dq* controller can not see the zero-sequence current because it lies on a perpendicular axis. (c) The phase currents of M1 and M2 obtained using CS_{LINEAR} when the parameters of the modules are the same, except L_1 is 95% of L_2. By adding a zero-sequence controller, the effect of the overall unbalance as seen in Figure 9.71(a) has been minimized.



[AQ1] **FIGURE 9.72** Change in the bus voltage obtained using CS_{CONT1} (a, e), CS_{CONT2} (b, f), $CS_{DISCRETE}$ (c, g), and CS_{LINEAR} (d, h) for *case 1* (figures on the left) and *case 2* (figures on the right). Case 1 corresponds to a large transient in the input voltage, while case 2 corresponds to a large transient in the load. For either case, the drop in the bus voltage is larger when using CS_{LINEAR}, even though it is implemented for a smaller variation (5%) L_1 as compared to the proposed control schemes (15%).

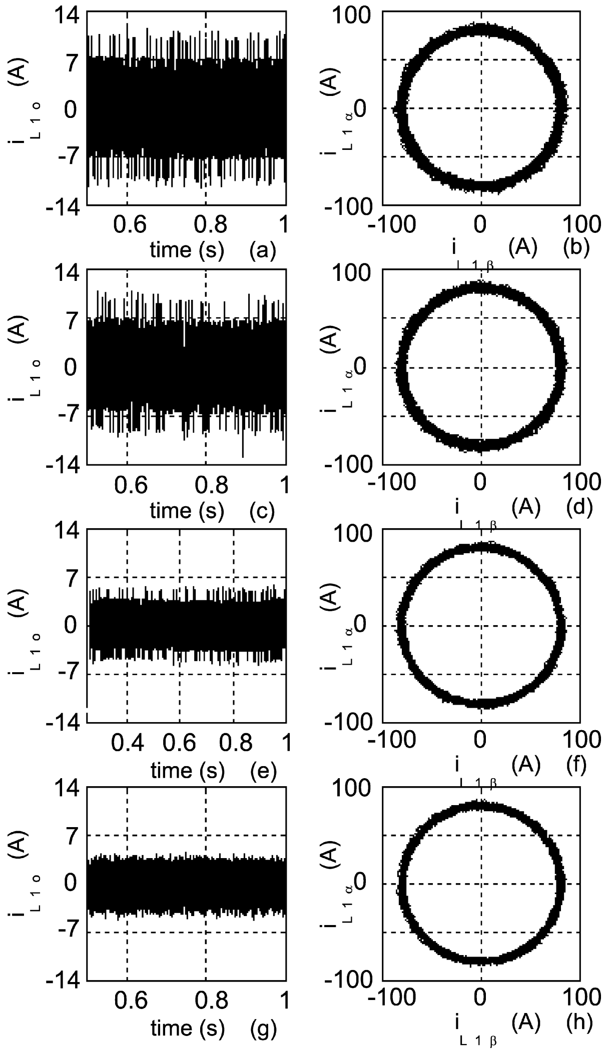
Research Issues

It is obvious from the above results that nonlinear controllers can and will play an increasingly effective role for the stabilization and performance optimization of progressively complex IPNs. However, to maximize the effectiveness of these nonlinear controllers, they need to be designed by treating an IPN model as a hybrid system and not as a smooth averaged model. This is a major challenge because the issues of existence of solutions and equilibrium stability for hybrids are difficult propositions to resolve. Additionally, to enhance the use of nonlinear controllers, their designs need to be systematic and not just intuitive. A further issue to be



[*AQ1*] **FIGURE 9.73** Distribution of the line currents between M1 and M2 obtained using (a) CS_{CONT1}; (b) CS_{CONT2}; (c) CS_{CONT3}, and (d) CS_{LINEAR} for *case 1* (figures on the left) and *case 2* (figures on the right). The proposed control schemes and CS_{LINEAR} operate with $L_1 = 85\%\ L_n$ and $L_1 = 95\%\ L_n$, respectively.

resolved is the need and procedure to quantify the improvement in performances of an IPN using a nonlinear controller with those that are obtained using a linear controller. Finally, strategies for distributed nonlinear control of IPNs needs to be developed, which take into account dynamic changes in the network and network processing delays leading to wider stability and power optimization.



[AQ1] **FIGURE 9.74** Steady-state currents on the zero axis and the $\alpha\beta$ axes for M1 obtained using CS_{CONT1}; (a) CS_{CONT2}; (c) $CS_{DISCRETE}$ (e-f), and CS_{LINEAR} (g-h). All of the cases have the same parametric variations. As such, the harmonic distortion and the zero-sequence current of $CS_{DISCRETE}$ and CS_{LINEAR} are close.

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9.7 Uninterruptible Power Supplies

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Uninterruptible power supply (UPS) systems are presented in this chapter. Topologies, operation, and control principles of UPS systems are explained in detail. In addition, a brief description of conventional UPS systems, their disadvantages, scope for improvement, and advanced architectures in UPS research are presented in this chapter.

Introduction

Uninterruptible power supply (UPS) systems are designed to provide reliable and high quality continuous power to critical loads in the face of events on the utility supply. These events can range from overvoltage and undervoltage conditions to complete disruption of the mains. UPS systems ensure power without break for the load as operating along with the mains as well as suppress line transients and harmonic disturbances.

UPS systems are being applied for a wide variety of critical equipment, such as medical facilities, life support systems, financial transaction handlers, data storage and computer systems, telecommunications, industrial processing, and on-line management systems [1].

The objective of UPS systems is to provide sinusoidal input current with low total harmonic distortion (THD) and to realize power line conditioning that has sinusoidal output voltage and unity power factor. In addition, an ideal UPS should have seamless transition capability when a failure occurs, high reliability, and high efficiency. Furthermore, the UPS system should be low maintenance, low cost, and light weight [2].

UPS systems are reviewed in terms of classification, operation, and control in this chapter. They are explained as static, rotary, and hybrid static/rotary systems in section 'Classification'. Static UPS systems are defined in detail in this chapter. In the section 'Applications', distributed and centralized applications are presented. The section 'Control Techniques' deals with suitable control techniques for these systems. Finally, the section 'Conclusion' summarizes the results obtained in this chapter.