Modulation Scheme for Three-Phase Differential-Mode Ćuk Inverter

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***Abstract*—Three-phase differential-mode inverters are single-stage inverters, which have the potential to reduce the number of devices and cost with higher power density. Among such inverter topologies, differential-mode three-phase Ćuk inverter (DTCI) has some advantage over other topologies, including modularity, lower number of switches, bidirectional power flow capability, and galvanic isolation. DTCI is a promising configuration for renewable-/alternative-energy applications with isolated and non-isolated structures. The continuous modulation scheme (CMS), which was introduced originally for the DTCI, activates all of three modules of the inverter. CMS increases the circulating power in modules and hence increases inverter power loss. This paper describes a discontinuous modulation scheme (DMS) for the DTCI which deactivates one module at a time resulting in a discontinuous operation of the inverter modules. The experimental open- and closed-loop results of DMS- and CMS-based DTCI are provided and compared. DMS reduces the circulating power, device voltage ratings, and mitigates the DTCI losses. The DTCI exhibits a nonlinear voltage gain with both DMS and CMS. It has been demonstrated that by feed-forwarding the input voltage and incorporating a static linearization method, the harmonic distortion of the output voltage is considerably reduced.**

***Index Terms*—Ćuk, differential-mode, feed-forward, high-frequency link, inverter, linearization, modulation, rectifier, renewable/alternative energy, single stage, switched-mode power supply (SMPS), three phase.**

I. Introduction

As photovoltaics, batteries, and other renewable/alternative power sources continue their rapid growth, inverters are getting increasingly important both economically and environmentally. Many topologies have been introduced for three-phase inverters in the literature [1]–[3]. A typical transformer-less topology has a bridge architecture [4], [5]. It can be cascaded with boost converter on the dc side to achieve a peak gain higher than unity [6]. These topologies may yield common-mode leakage current for some applications [7], [8]. For some other applications, higher peak voltage gain requirement may give rise to the need for a transformer [9]. Given the need for low-cost inverter with galvanic isolation, high-frequency-link (HFL) inverters have emerged as a potential front runner [10]–[15]. The simplest HFL topology often has a multistage topological architecture to accommodate the high-frequency transformer. The stages of multistage topology may be decoupled by a dc-link capacitor or dc-link inductor [16]. That may add to system cost, reliability, loss, and power density. Slightly modified topologies have been presented [10], [12]. They remove the dc link capacitor/inductor by using special modulation techniques [14]–[16], while they may achieve reduction in switching loss. Overall, for low-power applications, the cost-benefit tradeoff of a multistage HFL inverter topology requires careful attention. As such, for low-power three-phase HFL inverter applications, there is an enhanced thrust to seek single-stage topological solutions [17]–[20].

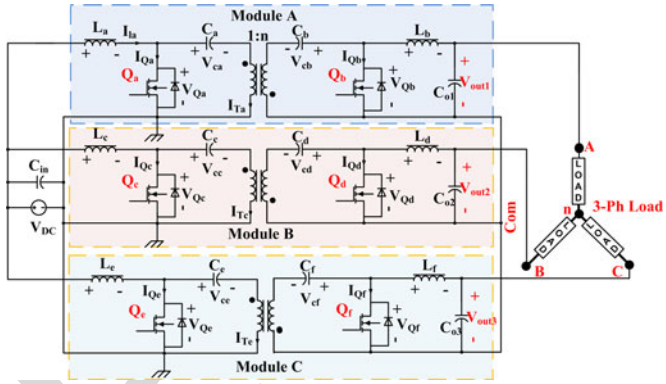

Fig. 1. Illustration of the DTCI topology, which comprises three modules (Module A, Module B, and Module C).

Single-stage topologies [21] are categorized, reviewed, and compared in [3]. Input-series output-parallel topologies are introduced in [22] and [23]. Three-phase SEPIC-based inverter is shown by Diab *et al.* [24]. Differential-mode single-phase Ćuk inverter is introduced in [25], and its design and modulation are presented in [26] and [27]. In [22] and [28], it is shown that topological embodiment of the differential inverter with Ćuk converter has some advantages. The general concept of polyphase differential inverters are introduced and the original differential-mode three-phase Ćuk inverter (DTCI) topology is proposed in [29]. The DTCI control and design using continuous modulation scheme (CMS) are presented by Ćuk and Erickson [30].

This paper presents the isolated DTCI as shown in Fig. 1. The isolated DTCI topology comprises three modules, which are connected in parallel at the dc side and connected to common ground at the ac side. Three phase load is connected differentially to the positive terminal of each module. The DTCI yields several useful features [30] that directly impact the cost,

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reliability, and power density. The DTCI comprises a limited number of switches all of which are low-side driven. Further, the inverter has the ability to support bidirectional power flow using the same set of switches and a seamless control. Yet another feature of the inverter is its ability to support voltage step-up and step-down functionalities that also enables the utility of the basic differential-mode topology for even nonisolated applications. An added capability of the HFL Ćuk inverter is its ability to support line-frequency ripple current without a large isolation transformer. Due to the presence of the two blocking capacitors on the primary and secondary sides of the transformer, the magnetizing current of the transformer is essentially devoid of any line-frequency current component. Finally, the possibility of coupled inductors and transformer has been introduced by Ćuk and Erickson [31], which enhances the compactness of the inverter and leads to reduced input and output ripples. The DTCI topology with a CMS outlined by Diab *et al.* [24], in which primary devices have three-phase sinusoidal modulating signals with a dc offset as common mode. The secondary-side devices are complementary with respective primary-side switch and considering a proper dead time. The common-mode dc offset of the output terminal voltages cancel each other because the load is connected differentially across the output-voltage terminals. However, this modulation scheme leads to circulation of power or reactive power flow through modules even with resistive load. This yields higher switching and conduction losses. Further, the dc offset voltage on output terminals of modules increases the peak voltages on the devices [32].

There is hardly any discussion on the need for proper modulation scheme for the DTCI in the literature [24], [25]. The discontinuous modulation to overcome the issue for single-phase differential-mode Ćuk inverter is proposed in [32]; however, there are substantial differences between implementation of modulation for single-phase and three-phase inverter. As such, this paper outlines a discontinuous modulation scheme (DMS) for the DTCI along with a description of the CMS in Section II. Further, the paper provides analytical insight into the performance comparison of DMS and CMS in Section III. The nonlinear behavior of the inverter leads to distortion of its output voltage when operating with either of the modulation schemes. A static linearization method with input voltage feed-forward is proposed to address the problem in Section IV. It has been shown that by using this method, the total harmonic distortion (THD) is reduced significantly below the acceptable level. Closed-loop control system is designed based on proportional resonant (PR) compensator [33] and experimentally implemented. Section V presents the experimentally obtained results of efficiency, device peak voltages, closed-loop transient, and THD. The experiments are carried out with proposed structures in the paper for both modulation schemes. They verify the analytical/simulation results of Section III and show the significant superiority of DMS over CMS. In the rest of the paper, the inverter refers to the DTCI.

II. Modulation Schemes for the DTCI

In this section, we first present the CMS for completeness of the discussion. The power flow mechanism will be presented to point to the motivation for searching another modulation technique. Then, the DMS will be proposed as a way to reduce the circulation power. It helps to mitigate part of losses and to reduce the ratings of the active devices. Its implementation on a digital control processor is also easy as it does not involve complex control algorithms.

A. Continuous Modulation Scheme

The line voltages of the inverter (V_{AB}, V_{BC}, and V_{CA}) are calculated by subtraction of output terminal voltages ($V_{\text{out}1}$, $V_{\text{out}2}$ and $V_{\text{out}3}$). Based on that, the normalized static line-voltage gain (g_{AB}, g_{BC}, and g_{CA}) relations can be defined as follows:

$$\begin{cases} g_{AB} = \dfrac{V_{AB}}{nV_{\text{DC}}} = g_A - g_B = \dfrac{V_{\text{out}1}}{nV_{\text{DC}}} - \dfrac{V_{\text{out}2}}{nV_{\text{DC}}} \\ \quad = \left(\dfrac{D_a}{1-D_a} - \dfrac{D_c}{1-D_c}\right) \\ g_{BC} = \dfrac{V_{BC}}{nV_{\text{DC}}} = g_B - g_C = \dfrac{V_{\text{out}2}}{nV_{\text{DC}}} - \dfrac{V_{\text{out}3}}{nV_{\text{DC}}} \\ \quad = \left(\dfrac{D_c}{1-D_c} - \dfrac{D_e}{1-D_e}\right) \\ g_{CA} = \dfrac{V_{CA}}{nV_{\text{DC}}} = g_C - g_A = \dfrac{V_{\text{out}3}}{nV_{\text{DC}}} - \dfrac{V_{\text{out}1}}{nV_{\text{DC}}} \\ \quad = \left(\dfrac{D_e}{1-D_e} - \dfrac{D_a}{1-D_a}\right) \end{cases} \tag{1}$$

where D_a through D_e are duty cycles of switches Q_a through Q_e, respectively, V_{DC} is the dc input voltage, n is turns ratio of the transformers and g_A, g_B, and g_C represents the normalized voltage gain of the phases. The method of modulation that suggested by Barzegar and Ćuk [29] is to generate three phase sinusoidal waveforms at the output terminals of the modules. The output voltages of the modules are unipolar, thus a common-mode dc-offset is added to the sinusoidal voltages of the terminals. It is assumed that the common-mode dc-offset voltages are equal for all phases; therefore, they cancel out on the line voltages. Thus, the normalized phase-voltage gains (g_A, g_B, and g_C) of the inverter with CMS are defined as follows:

$$\begin{cases} g_A = g^* \left(1 + \sin\left(\omega t + \gamma\right)\right) \\ g_B = g^* \left(1 + \sin\left(\omega t - \dfrac{2\pi}{3} + \gamma\right)\right) \\ g_C = g^* \left(1 + \sin\left(\omega t - \dfrac{4\pi}{3} + \gamma\right)\right). \end{cases} \tag{2}$$

Line voltages are also obtained as follows, in which g^* is normalized peak phase-voltage gain, ω is angular line frequency, and γ represents an arbitrary initial phase

$$\begin{cases} V_{AB} = \sqrt{3} n V_{\text{DC}} g^* \sin\left(\omega t + \dfrac{\pi}{6} + \gamma\right) \\ V_{BC} = \sqrt{3} n V_{\text{DC}} g^* \sin\left(\omega - \dfrac{\pi}{2} + \gamma\right) \\ V_{CA} = \sqrt{3} n V_{\text{DC}} g^* \sin\left(\omega t - \dfrac{7\pi}{6} + \gamma\right). \end{cases} \tag{3}$$

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This modulation is called CMS because the power flows continuously in all modules. In order to understand the effect of modulation on the power loss, the flow of power in the modules is investigated next. It is shown that using CMS, the reactive power flows in modules even in the case of pure resistive load. Assuming that the three-phase load is resistive, the output currents of the modules are in synchronism with their respective phase voltage as are captured by

$$\begin{cases} I_A = \dfrac{nV_{\rm DC}g^*}{R}\sin(\omega t+\gamma) \\ I_B = \dfrac{nV_{\rm DC}g^*}{R}\sin(\omega t-2\pi/3+\gamma) \\ I_C = \dfrac{nV_{\rm DC}g^*}{R}\sin(\omega t-4\pi/3+\gamma) \end{cases} \tag{4}$$

where R is the load resistance. The instantaneous power of module (p_A, p_B, or p_C) is the multiplication of the respective phase voltage and the phase current as shown in

$$\begin{cases} p_A = \dfrac{(nV_{\rm DC}g^*)^2}{R}\left[\sin^2(\omega t+\gamma)+\sin(\omega t+\gamma)\right] \\ p_B = \dfrac{(nV_{\rm DC}g^*)^2}{R}\left[\sin^2\left(\omega t-\dfrac{2\pi}{3}+\gamma\right)\right. \\ \qquad \left.+\ \sin\left(\omega t-\dfrac{2\pi}{3}+\gamma\right)\right] \\ p_C = \dfrac{(nV_{\rm DC}g^*)^2}{R}\left[\sin^2\left(\omega t-\dfrac{2\pi}{3}+\gamma\right)\right. \\ \qquad \left.+\ \sin\left(\omega t-\dfrac{2\pi}{3}+\gamma\right)\right]. \end{cases} \tag{5}$$

Fig. 2 illustrates the simple implementation of CMS-based DTCI and it also shows the waveforms of the modulating signals, output terminal voltages, and line voltages. Fig. 3 shows the power waveforms of the three modules of the inverter operating with CMS during a complete line cycle; they are derived using (5). The piecewise power flow direction diagrams are also illustrated. It can be seen that the power flow is positive during half a cycle for modules, which implies that power is transmitted from source to load with a peak of $2\frac{(nV_{\rm DC}g^*)^2}{R}$. During the other half of the same line cycle, a small amount of negative power flows, which reaches the peak of $-\frac{1}{4}\frac{(nV_{\rm DC}g^*)^2}{R}$ at two points. This implies that, during this time, a part of power that has been transmitted to the load side by other module(s) returns to the source. So it is evident that instantaneous power changes direction, which indicates the presence of circulating (or reactive) power. The reactive power is not desirable because it increases the peak power which leads to higher peak voltage or higher current stress on the components; further, the conduction and switching loses increase as well. The reactive power of the CMS-based DTCI will be mathematically calculated and it will be compared with the corresponding results obtained using DMS; this will be illustrated in next section.

B. Discontinuous Modulation Scheme

The CMS was originally introduced for the low-power amplifiers of analog circuits [29] with limited focus on power loss.

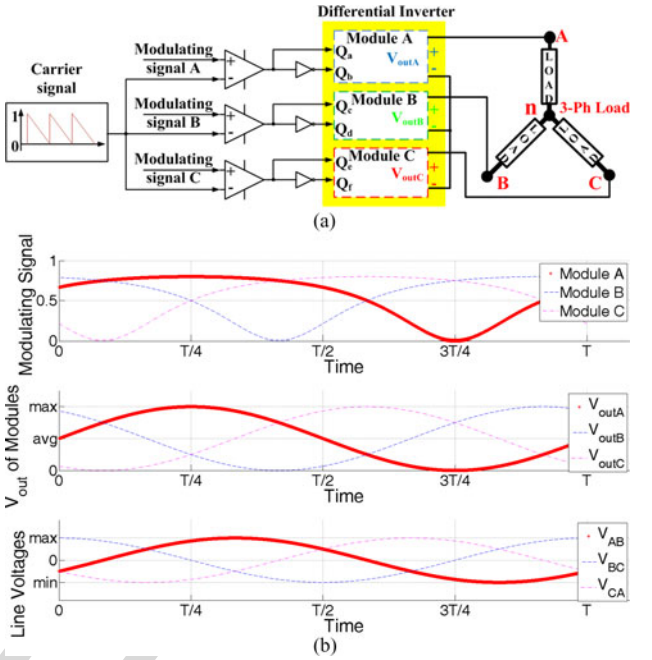

Fig. 2. (a) Illustration of realization of the CMS for the inverter. (b) Illustration of the modulating signal of the primary side switches (duty cycle), terminal voltages ($V_{\rm out1}$, $V_{\rm out2}$, and $V_{\rm out3}$) of Modules A, B, and C, and line voltages (V_{AB}, V_{BC}, and V_{CA}) of the inverter using the CMS.

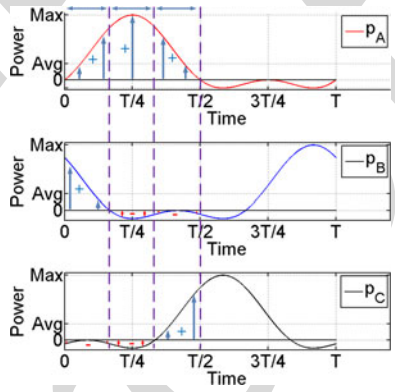

Fig. 3. Instantaneous output powers waveforms of the inverter when it is operating with CMS.

For the inverter, and as evident from the illustration in Fig. 3, the modulation scheme needs to be revised with enhanced emphasis on reducing circulating power and associated power loss. Therefore, the major motivation for development of a new scheme is to mitigate the circulating power. A similar concept of modulation method for single-phase inverter in [32] is used, but implementation of the concept for three phase inverter is different. A closer scrutiny of (5) reveals that, because the first term is squared and is always positive, the negative portion of the power is caused by the second expression inside the bracket. This expression is originated from the dc offset voltage at the output terminal voltages. So a reduction in the dc-offset voltage will reduce the circulating power and the device voltage stress.

The reason for adding a common-mode dc-offset voltage to the phase voltages is to meet the voltage polarity restriction of the modules. It is noted that loads are connected differentially

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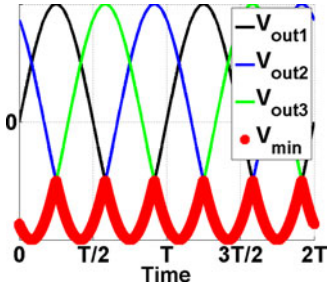

Fig. 4. Three phases of the output terminal voltages of DTCI assuming no dc-offset. The highlighted lower push of waveforms shows the minimum of the three phase voltages.

between terminals and this common-mode voltage do not appear on them. With ideally bipolar modules, there is no need for offset voltages to be added and terminal voltages would look like Fig. 4. In the case of DTCI, a common-mode offset voltage is needed to keep the terminal voltage positive. But the point is that, this common-mode voltage does not need to be a dc value and it can vary with the time. $V_{\min}$ is the smallest voltage between three terminal voltages (V_{out1}, V_{out2}, and V_{out3}) of the above mentioned ideal inverter, as highlighted in Fig. 4. The idea is to add a variable-offset voltage, which is equal to absolute value of the voltage $V_{\min}$ ($|V_{\min}|$) at each instant of the line cycle. The advantage of using this minimized variable common-mode voltage is the reduction of reactive power going through the inverter as can be inferred by (5). The $V_{\min}$ is identical to one of the phases at each 120°; as a result, one terminal voltage equals to zero during a 120° interval. The positive terminal voltages are always guaranteed with offset voltage minimized at each instant of the time, by using the described offset voltage.

The output terminal voltage will be zero during the one-third of a line cycle with the proposed method. As such, this modulation scheme is referred to as DMS. The mathematical presentation of output terminal voltages of inverter operating with DMS is shown below:

$$\begin{cases} V_{\text{out1}} = nV_{\text{DC}}g^*\left[\sin\left(\omega t+\gamma\right)+|V_{\min}|\right] \\ V_{\text{out2}} = nV_{\text{DC}}g^*\left[\sin\left(\omega t-\dfrac{2\pi}{3}+\gamma\right)+|V_{\min}|\right] \\ V_{\text{out3}} = nV_{\text{DC}}g^*\left[\sin\left(\omega t-\dfrac{4\pi}{3}+\gamma\right)+|V_{\min}|\right] \end{cases} \tag{6}$$

in which $V_{\min}$ is defined by

$$V_{\min} = \begin{cases} \sin\left(\omega t-\dfrac{4\pi}{3}+\gamma\right) & \text{if } -\dfrac{\pi}{6}+2\pi m<\omega t+\gamma<\dfrac{\pi}{2}+2\pi m \\ \sin\left(\omega t-\dfrac{2\pi}{3}+\gamma\right) & \text{if } \dfrac{\pi}{2}+2\pi m<\omega t+\gamma<\dfrac{7\pi}{6}+2\pi m \\ \sin\left(\omega t+\gamma\right) & \text{if } \dfrac{7\pi}{6}+2\pi m<\omega t+\gamma<\dfrac{11\pi}{6}+2\pi m \end{cases} \tag{7}$$

where m is an integer.

Fig. 5 shows the ideal waveforms of the modulating signals, output terminal voltages, and line voltages of the DMS-based DTCI. Even though the output terminal voltages do not look like sinusoidal waveforms and have discontinuity, the line voltages (i.e., phase-to-phase) are clean sinusoidal waveforms. Fig. 6 illustrates the power flow direction along with power waveforms. The power varies between the positive peak of $1.616\frac{(nV_{\text{DC}}g^*)^2}{R}$ and negative peaks of $-0.116\frac{(nV_{\text{DC}}g^*)^2}{R}$. Comparing the results for DMS with the same results for CMS shows DMS has smaller positive and negative peaks at the first place.

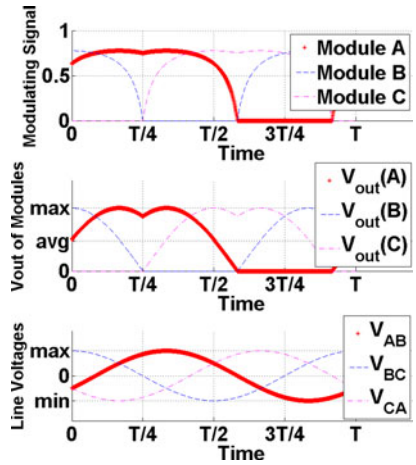

Fig. 5. Illustration of the modulating signal (representing the duty cycle) of the primary-side switches, terminal voltages (V_{out1}, V_{out2}, *and* V_{out3}) of Modules A, B, and C, and line voltages (V_{AB}, V_{BC}, and V_{CA}) of the DMS-based DTCI.

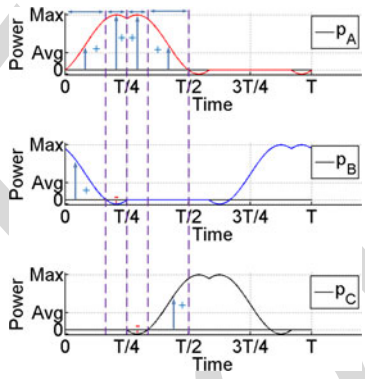

Fig. 6. Instantaneous output powers waveforms of the inverter when it is operated using DMS.

III. Analysis

This section provides the theoretical evaluation and analysis of the CMS and the DMS assuming ideal switches. Section V provides validating experimental results.

A. Circulating Power

As explained in Section II, both modulations yield circulating power, but the magnitudes of the circulating power are different. In order to have a base for measurement and comparison of the circulating power in the inverter modules, the more general definition of the reactive power, known as Fryze's definition [34], will be used. Because each of the nominal modules

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of the inverter has identical topology, only one module (i.e., Module A) is selected here for the calculation of the active and reactive power of the inverter. Fryze's definition of reactive power is a comprehensive definition, which also encompasses nonlinear circuits. The following equations are based on this definition and can be used to capture the reactive power of Module A:

$$P_A = < p_A(t) >_{\text{avg}} = \frac{1}{T}\int_0^T V_{\text{out1}}(t) I_A(t) dt \tag{8}$$

$$\begin{aligned} S_A^2 &= P_A^2 + Q_A^2 = V_{\text{out1}}^2\,(\text{rms})\, I_A^2\,(\text{rms}) \\ &= \frac{1}{T}\int_0^T V_{\text{out1}}^2\,(t)\, dt \frac{1}{T}\int_0^T I_A^2(t) dt. \end{aligned} \tag{9}$$

where $p_A\,(t)$ is the instantaneous power, P_A is the active power, Q_A is the reactive power, S_A is the apparent power, and V_{out1} and I_A are output terminal voltage and phase current of Module A. Using (8) and (9), the ratio of the reactive to the active power can be derived as follows:

$$\frac{Q_A}{P_A} = \sqrt{\frac{\frac{1}{T}\int_0^T V_{\text{out1}}^2\,(t)\, dt \frac{1}{T}\int_0^T I_A^2(t) dt}{\left[\frac{1}{T}\int_0^T V_{\text{out1}}\,(t)\, I_A(t) dt\right]^2} - 1}. \tag{10}$$

Now assuming a load with unity power factor and a negligible THD of the load voltage and the load current, we obtain the following relations for the CMS-based DTCI:

$$\begin{cases} I_A = \dfrac{nV_{\text{DC}}g^*}{R}\sin(\omega t + \gamma) \\ V_{\text{out1}} = g_A n V_{\text{DC}} = nV_{\text{DC}}g^*\left(1 + \sin(\omega t + \gamma)\right). \end{cases} \tag{11}$$

Substituting V_{out1} and I_A from (11) into (10) and simplifying the resultant expression, one obtains (12) as shown bottom of the page.

It is noted that (12) is valid only for a unity-power-factor load and for a lossless CMS-based DTCI. It shows that the ratio of the reactive power to the active power is constant and do not vary with peak voltage gain of inverter. Also it is noted that the reactive power of DTCI is due to the nonlinear nature of inverter and it is not caused by any passive components of the topology.

Similar calculation is carried out for DMS-based DTCI to compare the results with those obtained using CMS-based DTCI. Current I_A is obtained in (4) and V_{out1} for DMS-based DTCI is described by (6) and (7). If these values are substituted into (10), one obtains the ratio of the reactive power to the active power as follows:

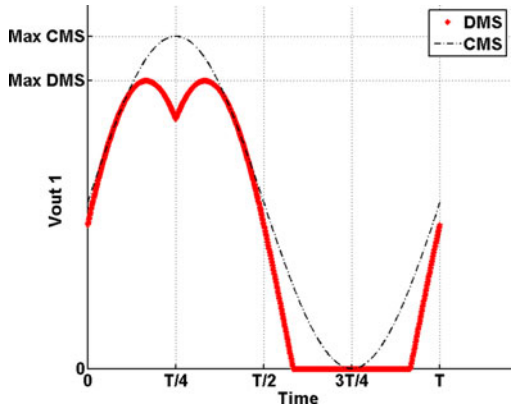

Fig. 7. Comparison of the output terminal voltages of DTCI operating with CMS and DMS. The CMS-based DTCI results in higher peak for the output terminal voltage; even though the line voltage of the inverter remains the same for both cases.

$$\frac{Q_A}{P_A}(\text{DMS}) = \sqrt{\frac{\left(1 + \frac{3\sqrt{3}}{8\pi}\right) \times \frac{1}{2}}{\left[\frac{1}{2}\right]^2} - 1} = \sqrt{1.413} = 1.188. \tag{13}$$

It is noted that circulation power in the case of single-phase inverter operating with DMS is zero [32]. In a case of DTCI, the ratio is not zero, however, smaller than that obtained for the CMS-based DTCI. By dividing these ratios, we will have the circulating power ratio of CMS to DMS for three-phase inverter, which is $\frac{Q_{\text{CMS}}}{Q_{\text{DMS}}} = 1.19$. It means that CMS has 19% more circulating power than DMS. The circulating power leads to both higher conduction losses and higher switching losses. Furthermore, it is noted that there is no switching at one third of times when using DMS (refer to Fig. 5) that impacts the switching losses. The significant effect of the DMS on inverter efficiency will be shown by experimental results in Section V.

B. Device Rating

The other advantage of using DMS over CMS is to reduce the stress on some of the components. The mathematical comparison of the peak voltage on the active components is provided below. The simulation results are also provided to compare the voltage and current peaks on other components.

Fig. 7 compares the output terminal voltage of phase A (V_{out1}) of DTCI operating with CMS and DMS under the equal line-voltage levels. The peak voltage of V_{out1}, (i.e., by V_{out1}^*), is higher for DTCI operating with CMS [V_{out1}^* (CMS)]. Using (11), V_{out1}^*(CMS) is found to be $2nV_{\text{DC}}g^*$, while the peak line voltage is $\sqrt{3}nV_{\text{DC}}g^*$. In order to obtain V_{out1}^* for DMS, one of

$$\frac{Q_A}{P_A}(\text{CMS}) = \sqrt{\frac{(nV_{\text{DC}}g^*)^2\int_0^T (1+\sin(\omega t+\gamma))^2\, dt \left(\frac{n\times V_{\text{DC}}\times g^*}{R}\right)^2 \int_0^T \sin^2(\omega t+\gamma)\, dt}{\frac{(nV_{\text{DC}}g^*)^4}{R^2}\left[\int_0^T (1+\sin(\omega t+\gamma))\sin(\omega t+\gamma)\, dt\right]^2} - 1} = \sqrt{\frac{\frac{3}{2}\times\frac{1}{2}}{\left[\frac{1}{2}\right]^2} - 1} = \sqrt{2} = 1.414. \tag{12}$$

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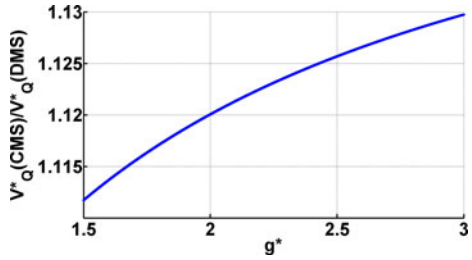

Fig. 8. $V^*_{Qa}(\mathrm{CMS})/V^*_{Qa}(\mathrm{DMS})$ as a function of g^*.

the phase voltages should be calculated by substituting (7) into (6) as demonstrated below for phase A: (14) as shown bottom of the page.

As evident from (14), the peak output terminal voltage of DTCI operating with DMS $[V^*_{\mathrm{out1}}(\mathrm{DMS})]$ equals $\sqrt{3}nV_{\mathrm{DC}}g^*$ and the line voltage matches that obtained using the DMS-based DTCI. The following equation summarizes these results as

$$\begin{cases} V^*_{\mathrm{out1}}(\mathrm{CMS}) = 2nV_{\mathrm{DC}}g^*, \\ V^*_{\mathrm{out1}}(\mathrm{DMS}) = \sqrt{3}nV_{\mathrm{DC}}g^*. \end{cases} \tag{15}$$

Following Fig. 1, the off-state voltage of each device in the module (V_{Qa}, V_{Qb}) is given by the following set of expressions:

$$\begin{cases} V_{Qa} = V_{ca} + \dfrac{V_{cb}}{n} \\ V_{Qb} = nV_{ca} + V_{cb} \end{cases} \tag{16}$$

where V_{ca} and V_{cb} are the voltages across the blocking capacitors C_a and C_b, respectively. In the steady state, using $V_{ca} = V_{\mathrm{DC}}$ and $V_{cb} = V_{\mathrm{out1}}$, (16) yields

$$\begin{cases} V_{Qa} = V_{\mathrm{DC}} + \dfrac{V_{\mathrm{out1}}}{n} \\ V_{Qb} = nV_{\mathrm{DC}} + V_{\mathrm{out1}}. \end{cases} \tag{17}$$

The voltage ratings of the devices should be designed for the worst-case condition, which happens at the peak output voltage. The ratio of the peak voltage of either of devices using CMS-based DTCI to the peak voltage of the device with DMS-based DTCI can be obtained by using (15) and (17). This ratio is simplified as a function of peak phase-voltage gain as follows, where V^*_{Qa} and V^*_{Qb} are peak voltages on primary and secondary switches, respectively:

$$\begin{aligned} \frac{V^*_{Qa}(\mathrm{CMS})}{V^*_{Qa}(\mathrm{DMS})} = \frac{V^*_{Qb}(\mathrm{CMS})}{V^*_{Qb}(\mathrm{DMS})} &= \frac{V_{\mathrm{DC}} + \frac{V^*_{\mathrm{out1}}(\mathrm{CMS})}{n}}{V_{\mathrm{DC}} + \frac{V^*_{\mathrm{out}}(\mathrm{DMS})}{n}} \\ &= \frac{1+2g^*}{1+\sqrt{3}g^*}. \end{aligned} \tag{18}$$

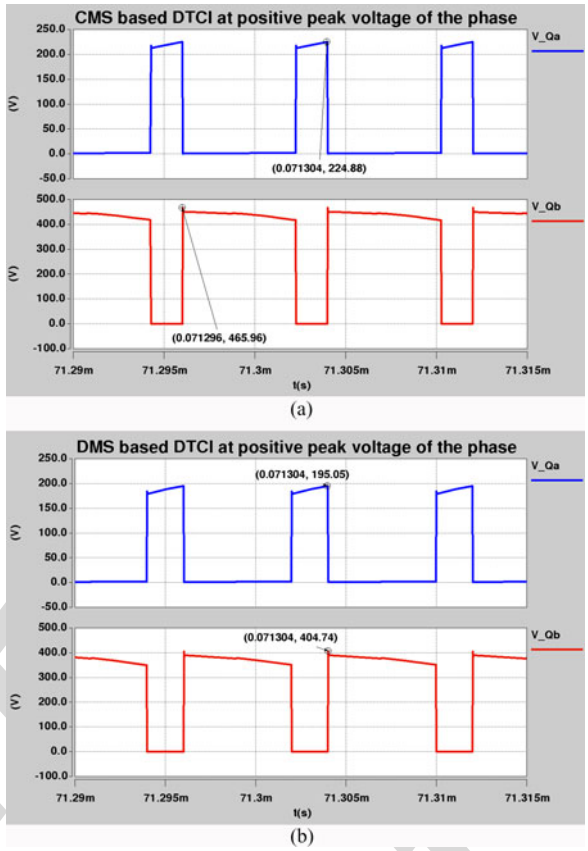

Fig. 9. Simulation results for V_{Qa} and V_{Qb} obtained using (a) CMS and (b) DMS when the output voltage attains the maximum positive value.

It is noted that (18) does not include any device voltage spike, which is dependent on the load, leakage inductance of the transformer, the off-state voltage of the device, and printed-circuit-board layout. As such, the actual peak voltages are slightly higher than (17). Nevertheless, (18) still provides a good approximation for comparison purposes as proved by experimental results in Section V.

The ratio $\frac{V^*_{Qa}(\mathrm{CMS})}{V^*_{Qa}(\mathrm{DMS})}$ as described by (18) is plotted in Fig. 8. The ratio is always greater than one and the ratio increases with increasing normalized phase-voltage gain. The purpose of the plot is to demonstrate the effect of modulation on reduction of device voltage rating following (18) and is validated using simulation and experimental results as follows.

Fig. 9 shows the (Saber-based) simulation results for the peak drain-to-source voltages of Q_a and Q_b operating with DMS and CMS. These simulations are carried out using circuit parameters that match those of the experimental prototype described in Section V. Using these parameters, the ratios of $\frac{V_{Qa}(\mathrm{CMS})}{V_{Qa}(\mathrm{DMS})}$ and

$$V_{\mathrm{out1}} = \begin{cases} \sqrt{3}nV_{\mathrm{DC}}g^* \sin\left(\omega t - \dfrac{\pi}{6} + \gamma\right), & \text{if } -\dfrac{\pi}{6} + 2\pi m < \omega t + \gamma < \dfrac{\pi}{2} + 2\pi m \\ \sqrt{3}nV_{\mathrm{DC}}g^* \sin\left(\omega t + \dfrac{\pi}{6} + \gamma\right), & \text{if } \dfrac{\pi}{2} + 2\pi m < \omega t + \gamma < \dfrac{7\pi}{6} + 2\pi m \\ 0, & \text{if } \dfrac{7\pi}{6} + 2\pi m < \omega t + \gamma < \dfrac{11\pi}{6} + 2\pi m. \end{cases} \tag{14}$$

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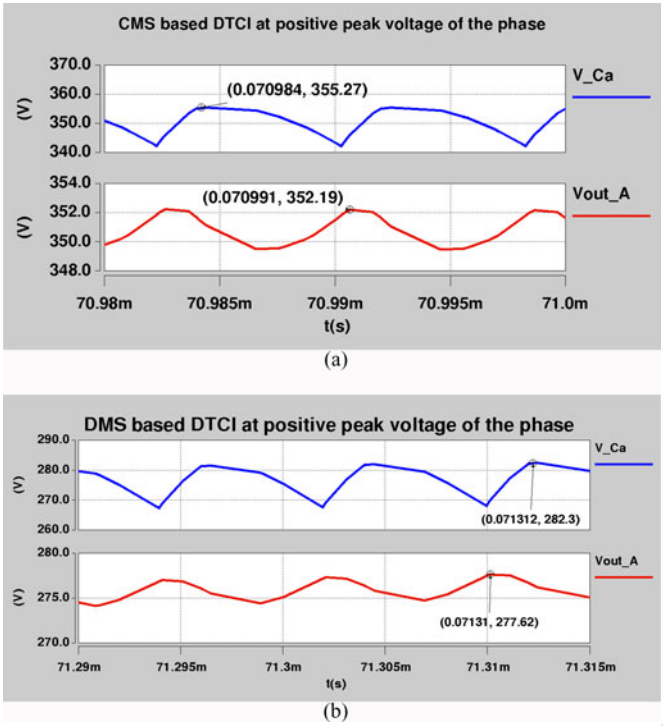

Fig. 10. Simulation results showing $V_{\mathrm{out}A}$, V_{cb}, I_{La}, and I_{Ta} for the inverter shown in Fig. 1 when the inverter is operated using (a) CMS and (b) DMS and when the output voltage attains the maximum positive value.

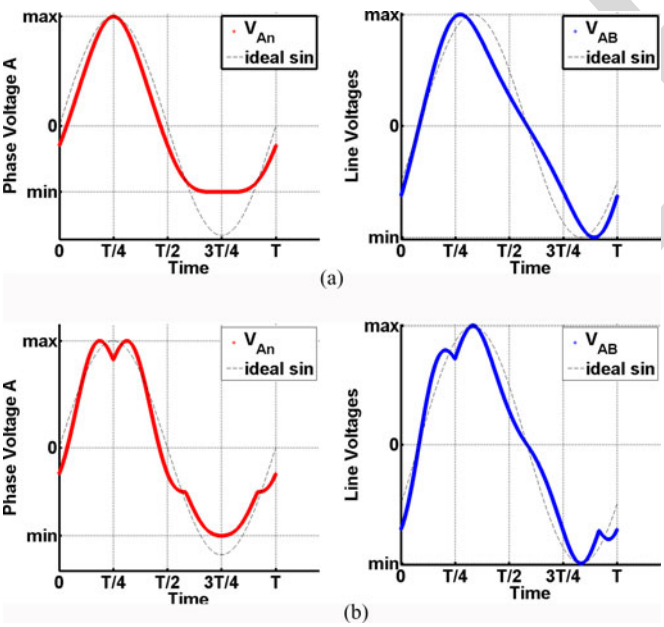

Fig. 11. Phase voltage and line voltage of DTCI operating with (a) CMS and (b) DMS.

$\frac{V_{Qb}(\mathrm{CMS})}{V_{Qb}(\mathrm{DMS})}$ are found to be 1.15, respectively, for $g^* = 3$, $V_{\mathrm{DC}} = 50$ V, $V^*_{\mathrm{out}} = 295$ V, and an output power (P_{out})of 500 W. This is found to be close to the theoretically predicted value as shown in Fig. 8 for $g^* = 3$. In addition, Fig. 10 shows that, using DMS, a reduction in the voltage of output capacitor ($V_{\mathrm{out}A}$) and blocking capacitor (V_{cb}) of the inverter is also achieved. Further, all of

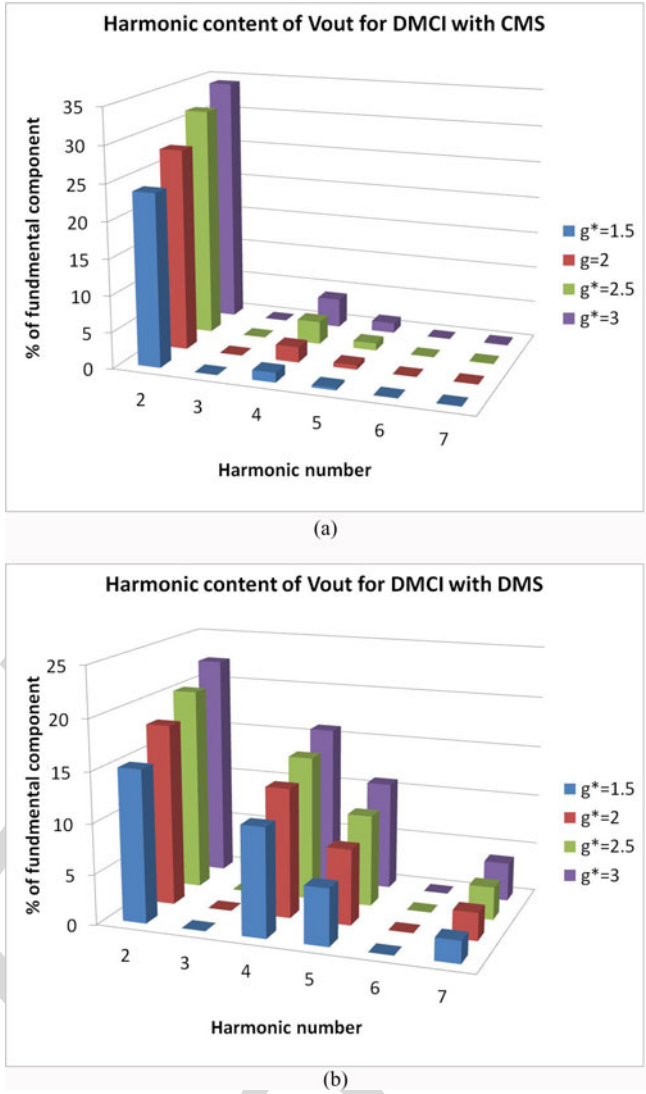

Fig. 12. Harmonic analysis of the line-voltage distortion caused by the nonlinearity in the static voltage-gain of the DTCI operated with (a) CMS and (b) DMS. Magnitudes of the second, third, fourth, fifth, sixth, and seventh harmonics are shown as a percentage of the fundamental-frequency (60 Hz) component magnitude versus peak phase-voltage gain.

these results are captured during the positive peak of the output voltage with transformer turns ratio of 2 (i.e., $n = 2$).

C. Distortion

The line voltage of the inverter is a nonlinear function of the duty cycle for both CMS and DMS as evident in (1). In order to compare the nonlinearity of the CMS and DMS, open-loop sinusoidal modulating signal is applied to DTCI operating with CMS and DMS. The simulation results are provided along with harmonic contents. Fig. 11(a) shows phase voltage (V_{An}) and line voltage (V_{AB}) of DTCI operating with CMS, while open-loop sinusoidal modulating signals are applied. Fig. 11(b) shows the similar waveforms for DTCI operating with DMS. Both simulations are carried out for line frequency of 60 Hz and $g^* = 3$. Fourier series analysis for line voltages versus g^* are shown in Fig. 12. The plots show the magnitude of Fourier series

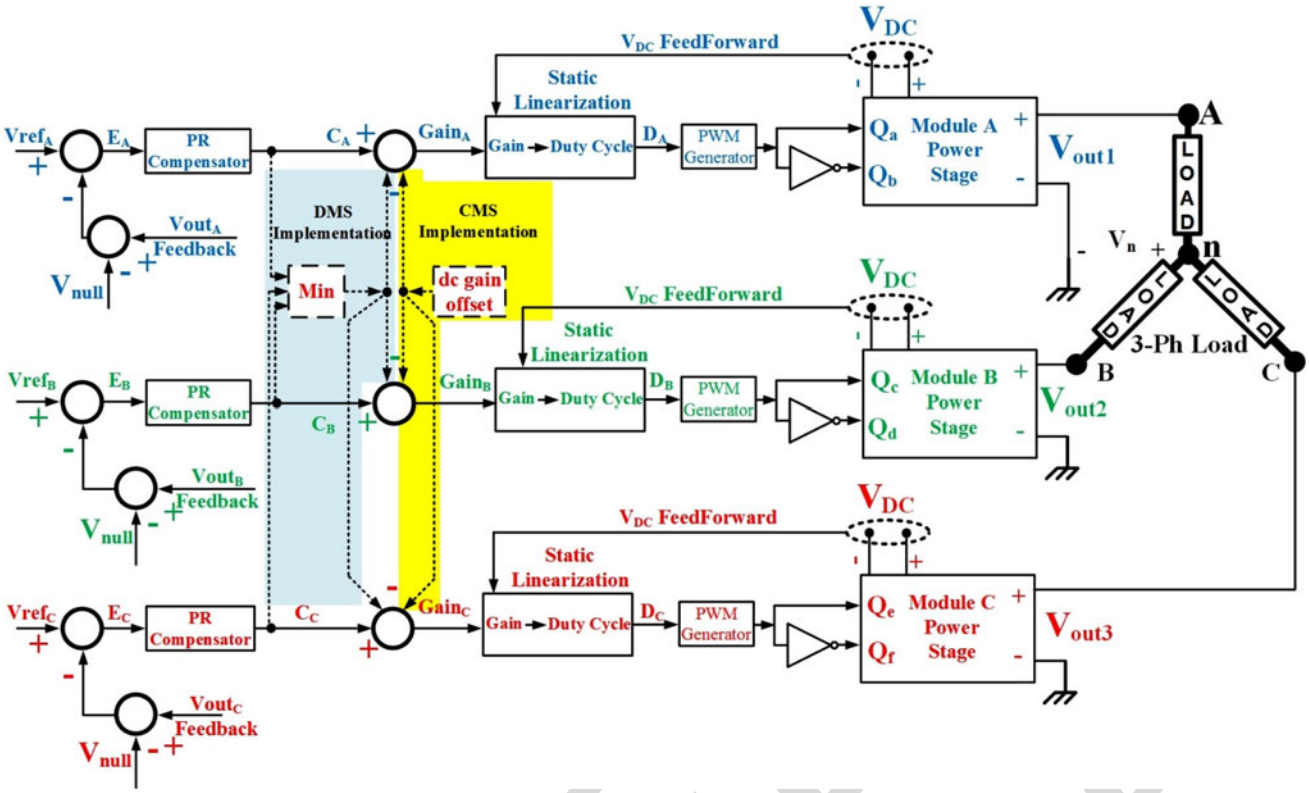

Fig. 13. Proposed architecture of the closed-loop controller for DTCI. Both CMS and DMS implementations are shown in a single diagram. The difference in the implementations is shown by dotted lines and highlighted part (right) for CMS and highlighted part (left) for DMS.

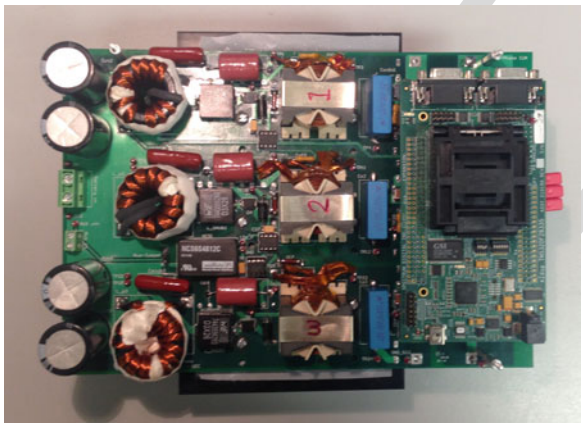

Fig. 14. Experimental prototype of DTCI. It shows the TMS320F28335 DSP-based digital controller on the top right, three transformers in the middle, and primary-side filter inductors and capacitors to the left.

coefficients as a percentage of the magnitude of fundamental-frequency component. It is evident from these results that the nonlinear voltage gain of DTCI causes distortion in the output voltage but the distortion is different for CMS and DMS. The distortion magnitude also depends on the variation of the duty cycle during a line cycle. The range of duty cycle swing is proportional to normalized peak phase-voltage gain (g^*). As expected, the magnitude of the harmonics increase at higher gains, because duty cycle swing is larger for CMS- and DMS-based DTCI. Also, comparison of CMS and DMS results reveals that DTCI exhibits considerable distortion while operating with CMS and DMS. The distortion of the inverter operating with CMS appears mostly as second harmonic; however, the harmonic distortion of the inverter operating with DMS is spread over a wide range of harmonics which is apparent from time-domain waveforms of the inverter operating with DMS. This is because of varying common-mode offset modulating signal with sharp edges (see Fig. 4) in DMS. Part of this varying common-mode modulating signal passes to the output voltage because of nonlinearity of the inverter. The large signal harmonic analysis of converter is done analytically in [35]. Section IV is devoted to discuss this issue and closed-loop implementation of the DMS-based DTCI.

IV. Nonlinearity and Closed Loop

In Section III, it is shown that the nonlinearity in the voltage gain of the inverter causes considerable amount of voltage distortion. Darwish *et al.* [30] uses harmonic compensation (HC) method to reduce the THD by eliminating some specific harmonics. The same method has been adopted generally for single-phase inverters to reduce the THD [32]. However, harmonic compensator reduces the loop gain bandwidth. Nonlinear compensation method may lead to enhanced transient responses while yielding lower THD [36]. Furthermore, as evident from Fig. 12, at least four harmonics with considerably large magnitudes should be mitigated using four HCs. This implies additional computational overhead for the DSP-based controller and further impact on the transient response/stability of the system.

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TABLE I
SPECIFICATIONS OF THE DTCI EXPERIMENTAL PROTOTYPE

Input voltage	Peak output voltage (0)	Output power	Output frequency	Transformer turns ratio (n)	Switching frequency	Primary-side filter inductance/Capacitance	Secondary-side filter inductance–Capacitance	Blocking Capacitance of Primary side/Secondary side
30–100 V	300 V	500 W	60 Hz	2	125 kHz	50 μH / 60 μF	100 μH / 8.8 μF	6.8 μF / 1.5 μF

The dynamic behavior of DTCI is nonlinear like most of the converters and a proper component selection and control design should be carried out for a practical system. The dynamic model and closed-loop controller design consideration of Ćuk-topology-based inverters have been studied extensively in literatures [29], [30], and [37]. But a major part of the output voltage distortion is due to nonlinear static relation of the inverter as shown in Fig. 12. It is noted that the distortion results of Fig. 12 are obtained by simulating a simple DTCI without considering dynamics of the system. This paper proposes the PR compensator for the inverter in conjunction with a static nonlinearity compensator along with feed-forward of input voltage. The compensator architecture is shown in Fig. 13.

The reference voltages ($V_{\mathrm{ref}A}$, $V_{\mathrm{ref}B}$, and $V_{\mathrm{ref}C}$) in Fig. 13 represent the voltage reference signals for the three phases. The measured phase voltages are fed back to close the control loops. Phase voltage (V_{An}, V_{Bn}, or V_{Cn}) is the potential difference of output terminal voltage of each DTCI module and the mid-point (null point) voltage (V_n). Voltage V_n is with respect to negative output terminals of the modules and can be measured directly by a sensor or can be calculated based on output terminal voltages with assumption of a symmetrical three-phase load as

$$V_n = \frac{V_{\mathrm{out}1} + V_{\mathrm{out}2} + V_{\mathrm{out}3}}{3}. \tag{19}$$

Error signal is fed to the PR compensator and the outputs of the compensators (C_A, C_B, or C_C) are fed to the modulator as shown in Fig. 13. The common-mode dc-offset voltage is added to control signal for the implementation of CMS as highlighted in Fig. 13. The resultant signal (i.e., Gain_A, Gain_B, and Gain_C) is applied to linearization block, which is followed by PWM generating block for implementing CMS.

The block which is labeled as "min" in Fig. 13 calculates the minimum of three-phase control signals (C_A, C_B, or C_C). This block is used for implementation of DMS, as highlighted in Fig. 13. The generated minimum signal (i.e., $C_{\min}$) is subtracted from each of three-phase control signals (C_A, C_B, or C_C). The resulting signal (i.e., Gain_A, Gain_B, and Gain_C) is applied to linearization block, which is followed by PWM generating block for implementing DMS. It is noted that the PWM generator block generates pulses with constant frequency and variable duty cycle, and linearization block is explained next.

Section III shows how the output voltage of the inverter is distorted in open-loop operation without linearization. The distortion shown in Figs. 11 and 12 is only due to nonlinear static relationship between voltage-gain and duty cycle in (1). This nonlinearity can be mitigated effectively by calculating the inversion of relationship in (1). The phase-voltage gain of phase A (G_A) and normalized phase-voltage gain (g_A) is given by

$$\begin{cases} G_A = \dfrac{V_{\mathrm{out}1}}{V_{\mathrm{DC}}} = n\dfrac{D_a}{1-D_a} \\ g_A = \dfrac{G_A}{n} = \dfrac{V_{\mathrm{out}1}}{nV_{\mathrm{DC}}} = \dfrac{D_a}{1-D_a}. \end{cases} \tag{20}$$

With rearrangement of D_a in terms of g_A in (20), one can obtain

$$D_a = \frac{g_A}{1+g_A} = \frac{V_{\mathrm{out}1}}{nV_{\mathrm{DC}} + V_{\mathrm{out}1}}. \tag{21}$$

The output signal of the first stage of modulator (i.e., Gain_A) can be assumed to be proportional to the output terminal voltage. This assumption is useful because both Gain_A signal and $V_{\mathrm{out}1}$ are supposed to have a single frequency and added offset. Note that the added offset value to Gain_A (and consequently to $V_{\mathrm{out}1}$) is not important, because this value is added equally to all phases and will be canceled out on line and phase voltages. Thus, the following assumption is purposefully made for phase A, and identical assumptions can be made for other phases as well:

$$\mathrm{Gain}_A = k_s V_{\mathrm{out}1} \tag{22}$$

where k_s is the scaling factor that can be obtained by using loop gains after controller design. By substituting (22) into (21), one obtains

$$D_a = \frac{g_A}{1+g_A} = \frac{\mathrm{Gain}_A}{k_s n V_{\mathrm{DC}} + \mathrm{Gain}_A}. \tag{23}$$

Equation (23) is important because, it captures the relationship between the duty cycle and Gain_A. The other parameters are either constant (n and k_s) or can be measured (V_{DC}). Thus, if (23) is implemented between the gain signals and duty cycle signals for CMS and DMS, it will remove the static nonlinearity of the open-loop gain of DTCI. We represent this block as "static linearization block" or SLB as illustrated in Fig. 13. The new open-loop module consists of series connection of SLB, PWM generator, and power module. The static voltage gain relation of this new open-loop system is linear as defined by (22).

V. EXPERIMENTAL RESULTS

This section provides the experimental results of the inverter operating using DMS and CMS. A 500-W experimental prototype of the inverter, as shown in Fig. 14, is implemented and tested with CMS and DMS. A TMS320F28335 DSP-based digital controller, with a 150-MHz clock, is used for implementing DMS and CMS. Real-time execution time for closed-loop control is close to 5 μs for DTCI with CMS or DMS. Specifications of the inverter prototype are provided in Table I. This

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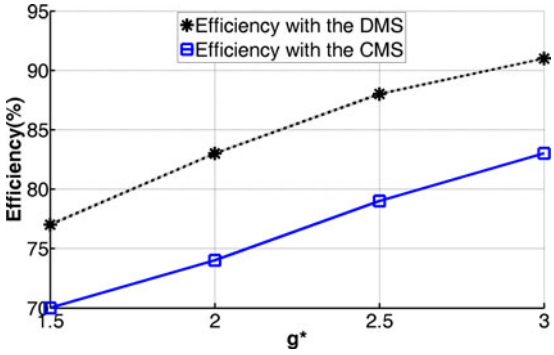

Fig. 15. Experimental efficiency of the inverter for varying normalized peak phase-voltage gain obtained using DMS and CMS.

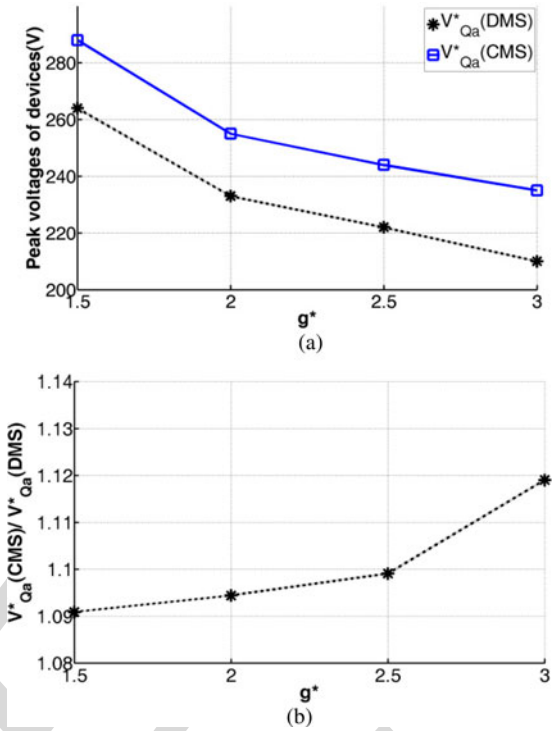

Fig. 16. (a) Experimentally determined peak voltage of the primary-side switches of the inverter with CMS (solid line) and DMS (dotted line). (b) Ratios of the two traces in (a).

section continues with experimentally obtained efficiency results first, which demonstrates a significant improvement in performance of the DMS-based DTCI compared to that obtained using the CMS-based DTCI. Subsequently, the measured peak device voltages are provided using CMS and DMS. These results are consistent with analytical and simulation results in Section III. The open-loop oscilloscope results will be presented as well, with and without SLB. The results prove the effectiveness of SLB to reduce distortion. Then, experimental transient and steady-state results for the proposed closed-loop schemes (see Fig. 13) are provided, which prove the effectiveness of the control structure.

Fig. 15 shows the efficiency of the inverter for a line voltage fixed at 208 V (RMS) and an output power of 500 W with normalized dc-voltage gain varying between 1.5 and 3 (corresponding to an input voltage ($V_{\rm DC}$) variation between 50 and 100 V). The difference between the efficiencies of the inverter operating with DMS and CMS is found to be significant. The improvement is almost constant at different peak gains and is consistent with the prediction from Section III-A, because the reactive power ratio of DTCI operating with CMS to that of operating with DMS is constant and it is not dependent on peak voltage gain.

Next, the peak voltages of the switches (Q_a, Q_c, or Q_e) on the primary side of DTCI obtained using DMS and CMS are measured and plotted in Fig. 16(a). It is noted that the voltage ratings of the switches on the ac side are proportional to the switches on the dc side with the proportionality constant being the transformer turns ratio. To obtain the plots in Fig. 16, the input voltage is varied between 50 and 100 V for a constant output power of 500 W, while keeping the line voltage set at 295 V (Peak). The results show that the gap between the peak voltage of the switches using DMS and CMS increases a little with increasing normalized phase-voltage gain. The ratios of the measured peak voltages of the primary-side switches of the inverter are shown in Fig. 16(b) and they are consistent with the predictions in Fig. 8 and the simulation results of Fig. 9.

Next, distortion caused by nonlinearity of the open-loop inverter operating with DMS and CMS is presented with experimental results. First, the open-loop DTCI without SLB is excited with sinusoidal signals for both modulation schemes. The experimental line voltages and phase voltages of the inverter operating using CMS are shown in Fig. 17(a) and (b), respectively. Fig. 18(a) and (b) shows the line voltages and phase voltages of DTCI operating using DMS, respectively. For these experiments, the peak instantaneous line voltages for both results are set at 295 V (corresponding to 208-V ac RMS), while the input voltage and output power are set respectively at 50 V and 500 W. The 30% THD is measured for this experiment with DMS, while CMS yields THD of 26% under the similar conditions. Further illustration of the problem is provided in Fig. 19, which compares the measured THD results for the open-loop DTCI operating with CMS (solid line) and DMS (dotted line) versus peak line-voltage gains. The progressively adverse effect of the line-voltage THD with increasing peak line-voltage gain is predictable with increasing range of duty cycle swing. Higher THD results for DMS-based DTCI compared to CMS-based DTCI are consistent with Section III-C results. The effect of SLB on open-loop responses is pursued next.

The static linearization method to overcome the distortion problem is discussed in Section III and static linearization method is proposed in Section IV based on (23). The SLB is implemented for the experimental DTCI using a DSP controller. The experiments are carried out for open-loop DTCI with SLB, under the identical operating condition used to carry out the experiments of Figs. 17–19. The line voltages and phase voltages of the inverter operating with CMS are shown in Fig. 20(a) and (b), respectively. Fig. 21(a) and (b) shows the line voltages and phase voltages of DTCI operating using DMS, respectively.

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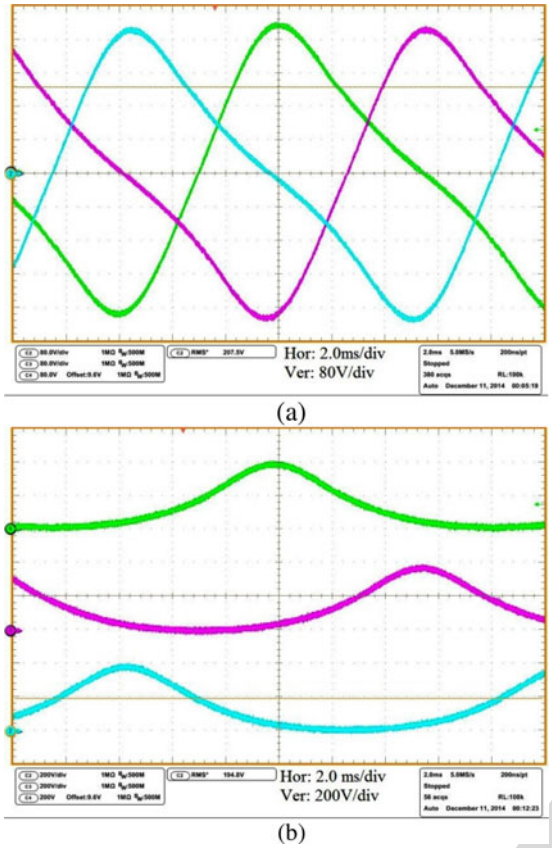

Fig. 17. Open-loop (a) line voltages and (b) phase voltages of DTCI, operating with CMS. The inverter is excited with sinusoidal signals without SLB.

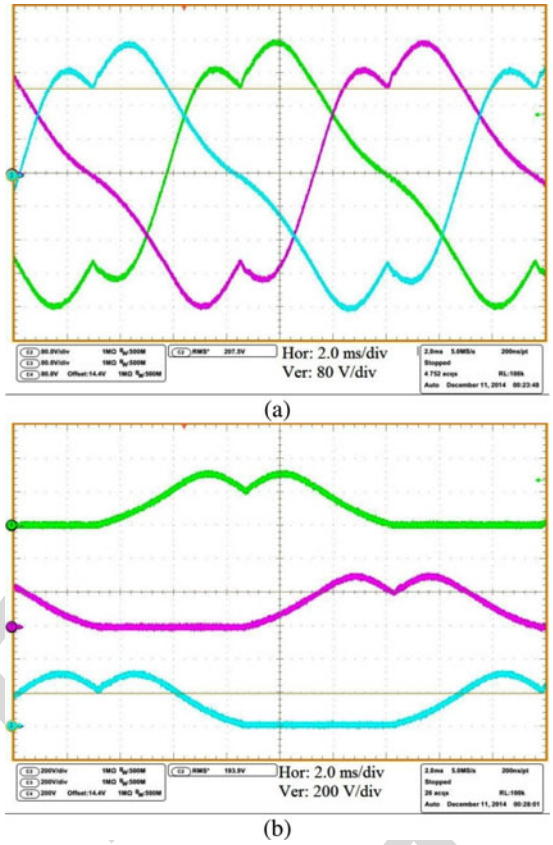

Fig. 18. Open-loop (a) line voltages and (b) phase voltages of DTCI, operating with DMS. The inverter is excited with sinusoidal signals without SLB.

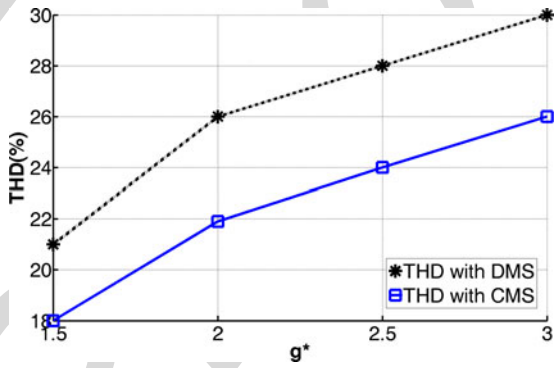

Fig. 19. Line-voltage THD results for open-loop DTCI without SLB operating with CMS (solid line) and DMS (dotted line), versus peak line-voltage gain.

Both experiments are carried out with SLB and DTCI is excited by three-phase sinusoidal signals (Gain_A through Gain_C). A THD of about 6% is measured for these experiments with CMS and DMS under similar operating conditions. Further, illustration of the problem is provided in Fig. 22, which compares the measured THD results for the open-loop DTCI with SLB operating with CMS (solid line) and DMS (dotted line) versus peak line-voltage gain. The significant reduction of THD by using SLB proves the effectiveness of the method. Also, it is evident that DTCI with DMS yields even better THD results than using CMS with SLB.

The remaining distortion after using static nonlinear compensation is primarily due to two factors: one is nonideal practical static phase-voltage gain, which does not exactly follow (20). The reason is the dead-time effect on the voltage gain of modules. The other important factor of distortion is the dynamic behavior of DTCI. The improved THD of DTCI obtained using DMS (as compared to that obtained using CMS) is due to the second factor. The different dynamic behavior of the inverter with two modulations can be explained by small-signal average model concept [30]. Each module equally contributes in the overall inverter total number of poles and zeroes in the model. DMS turn one of the modules off at each time, which means deactivating one-third of the contributing circuit to the dynamic response of the system. This results in reduced order dynamic of the system and it affects the distortion of the inverter.

Subsequently, the closed-loop controllers, as illustrated in Fig. 13, are implemented and the steady-state and transient results are presented below. The PR compensator is tuned to keep a balance between satisfactory steady-state performance and acceptable transient response [33], [38]. The peak line voltages for both experiments are set at 295 V (corresponding to 208-V RMS), while the output power are set at 500 W. Fig. 23 shows the THD of the line voltage of the closed-loop DTCI as a function

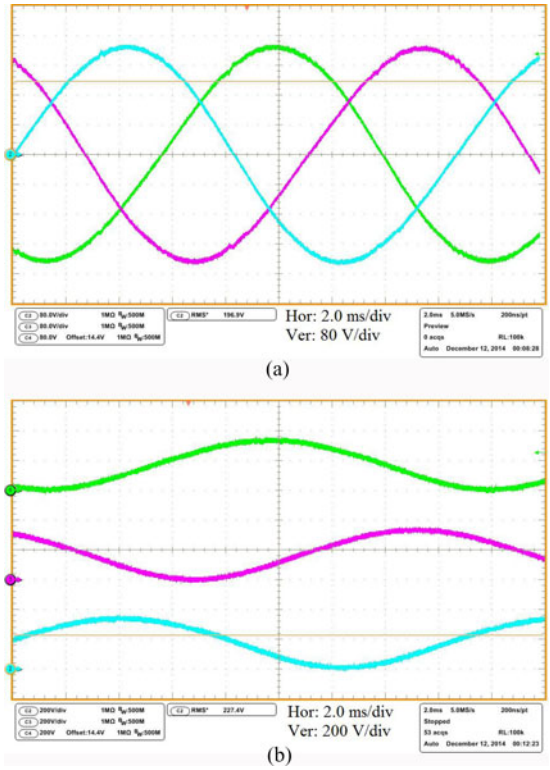

Fig. 20. Open-loop (a) line voltages and (b) phase voltages of DTCI, operating with CMS. The inverter is excited with sinusoidal signals applied to SLB.

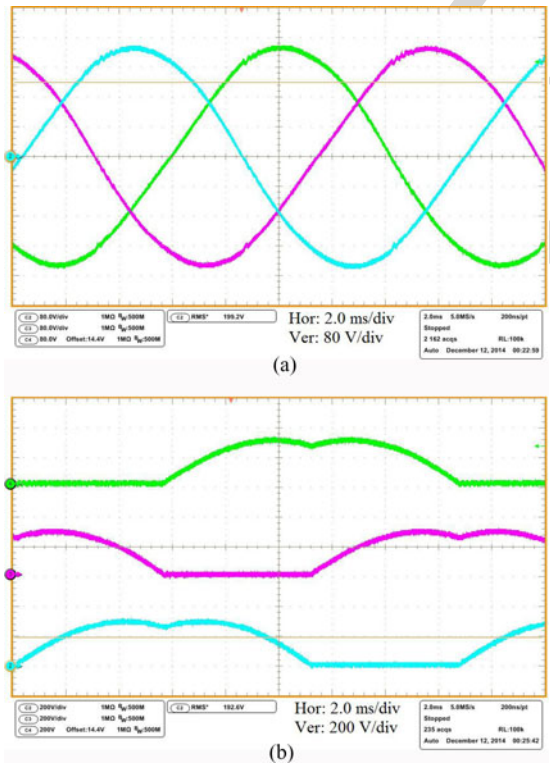

Fig. 21. Open-loop (a) line voltages and (b) phase voltages of DTCI, operating with DMS. The inverter is excited with sinusoidal signals applied to SLB.

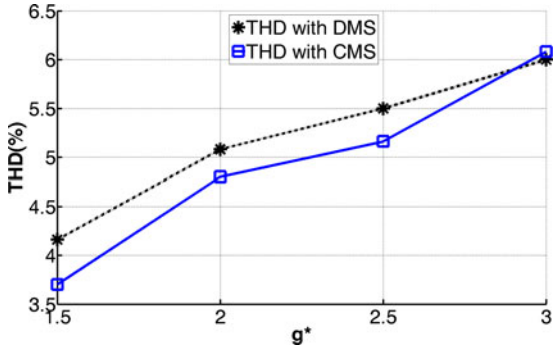

Fig. 22. Line-voltage THD results for the open-loop DTCI along with SLB. The inverter operating with CMS is solid line and DMS-based DTCI is represented by dotted line, versus peak line-voltage gain. It shows a marked improvement in the THD of DTCI using SLB.

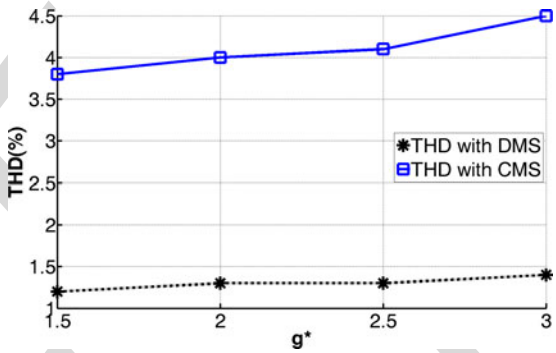

Fig. 23. Experimentally obtained THD of the line voltage as a function of the normalized peak line-voltage gain of the closed-loop DTCI when it is operated using DMS (dotted line) and CMS (solid line).

of the line-voltage gain when the inverter is operated with DMS (dotted line) and CMS (solid line). By comparing the open- and closed-loop results of DTCI, as shown, respectively, in Figs. 22 and 23, one can observe that the closing loop reduces the THD of the DMS-based and CMS-based closed-loop DTCI. In addition, to achieve an acceptable THD, the goal is to achieve an acceptable transient performance for the inverter. Consequently, the gains of the fundamental-frequency compensator have to be so chosen such that an optimal tradeoff between a lower harmonic distortion and a satisfactory transient response is achieved.

In order to investigate the transient behavior of the inverter, step responses of the system to load and reference changes are captured for DTCI operating with CMS and DMS in Figs. 24 and 25, respectively. An induction motor is used as a load in these experiments. A resistive load is paralleled to the motor load using electronic switch to emulate the fast step load changes in Figs. 24(a) and 25(b). Both modulations show similar transient during the step load changes, while DMS shows much faster response to step reference change. The start-up waveforms of line voltages of DTCI operating with CMS and DMS for resistive load are shown in Fig. 26(a) and (b), respectively. Transient responses are found to be satisfactory and they do not exhibit any overshoot or undershoot. The CMS- and DMS-based

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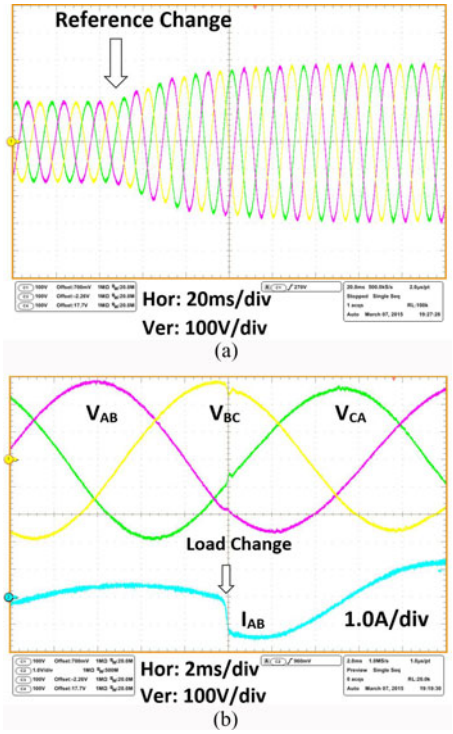

Fig. 24. Experimentally obtained step responses of line voltages of DTCI operating with CMS to (a) reference changes and (b) load changes. The motor is used as a load in these experiments.

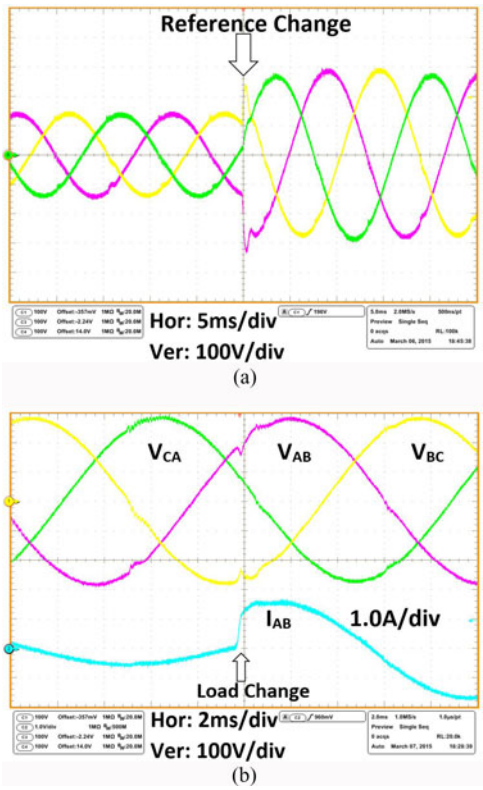

Fig. 25. Experimentally obtained step responses of line voltages of DTCI operating with DMS to (a) reference changes and (b) load changes. The motor is used as a load in these experiments.

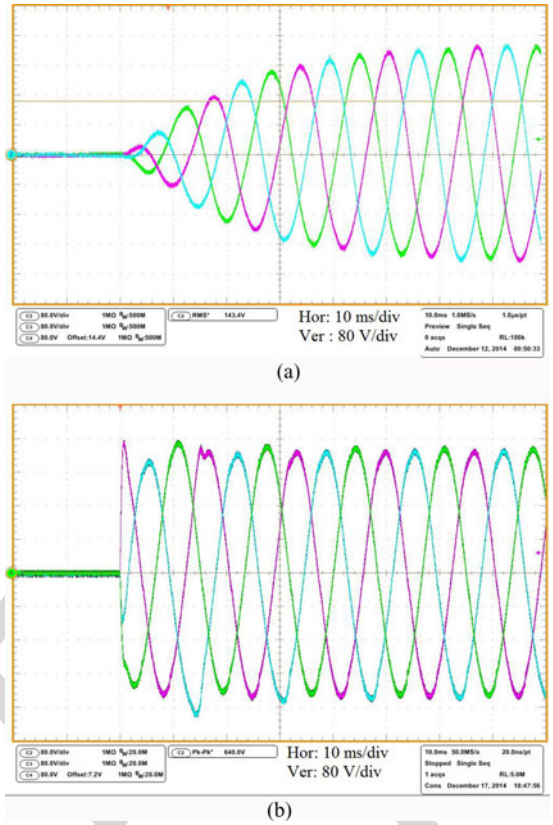

Fig. 26. Experimental obtained transient start-up responses of DTCI operating with (a) CMS and (b) DMS.

DTCI exhibit convergence after the third and second cycle, respectively.

VI. Conclusion

The paper proposes a DMS for a DTCI and compares the mechanism and performance of the DMS-based DTCI to that of a prior-art CMS-based DTCI. The motivation for development of DMS for DTCI was to reduce the circulating power in the modules. An experimental hardware prototype was developed for the inverter to validate and compare the results obtained operating with DMS and CMS with focus on energy-conversion efficiency, device rating, output-voltage distortion, and transient response of the inverter. The experimental results show the significant superiority of DMS in comparison to same results for CMS. The efficiency increase of more than 5% is observed with DMS. The peak device voltage rating reduction of 5–10% observed depending on voltage gain conditions with DMS too. The provided analytical/simulation results are also consistent with the mentioned results.

The analysis shows the distorted output for open-loop DTCI with both modulation schemes. The static linearization method is proposed for inverter as an effective method to reduce distortion. The effectiveness of method is proved by experimental THD results after and before addition of static linearization block for both modulation techniques. Finally closed-loop

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architecture is proposed and implemented. Experimental steady-state and start-up transient results are provided to show the effectiveness of linearization for both modulation schemes. The DMS-based DTCI has a better dynamic response because of the reduced order of dynamic system. So lower THD and faster transient responses are also achieved with DMS as evident from the experimental results.

An overall qualitative comparison between the DMS- and CMS-based operations of the inverter, as implemented currently, indicates that the DMS-based operation of the inverter has the potential to yield relatively higher saving in the power stage due to the reduced requirements of the device breakdown voltage and power handling.

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