Resolving Practical Design Issues in a Single-Phase Grid-Connected GaN-FET-Based Differential-Mode Inverter

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(Highlighted Paper)

***Abstract*—Microinverters for grid-connected photovoltaic (PV) power conversion systems often require voltage boost due to the low dc voltage of the PV panels. A high-frequency (HF) transformer-isolated differential-mode Ćuk inverter (DMCI) is an attractive topology due to its inherent voltage boost capability and high power density. One of the significant operational issue of the DMCI addressed in this paper is the presence of lower order harmonic distortion in the injected grid current. It is shown that lower order odd and even harmonic voltages are generated with this topology. This problem is accentuated due to the low damping offered by the grid to harmonic voltages. A systematic low-complexity control design is proposed to address this issue. It is shown experimentally that the DMCI operates stably with effective attenuation of the lower order harmonics using the proposed design. Practical operational issues of the DMCI with fast switching GaN field-effect transistor (FET) devices are analyzed and solutions are proposed. It is shown that there can be significant HF noise generation in the DMCI with a frequency range higher than the switching frequency. Practical solutions for resolving HF issues using a combination of circuit layout design and additional passive components are proposed and validated. All of the experimental results are demonstrated on a 500-W GaN-FET-based microinverter prototype.**

***Index Terms*—Control, Ćuk, differential-mode inverters, GaN field-effect transistor (FET), harmonic distortion, high-frequency (HF) link, parasitics.**

I. Introduction

VARIOUS power circuit configurations are used for photovoltaic (PV) power-conversion systems [1]. In case of low-power PV systems, microinverters or ac modules are popularly used [2]. Microinverters typically are rated for a few hundred watts. High-frequency (HF) transformer isolated power circuit topologies are attractive for PV microinverters as high power densities can be achieved [1] due to the reduced size of magnetics. For the typical power ratings of the PV microinverters, the input voltage from the PV panels is in the order of few tens of volts. For example, a 300-W PV module has a maximum-power-point voltage of about 36 V [3]. A single-phase microinverter connected to this module has to convert this low voltage to match the single-phase-rated voltage of 120 V. Hence, voltage boost is necessary for many microinverter applications. In this paper, a differential mode Ćuk inverter (DMCI) is considered for a PV microinverter. The Ćuk module used in the DMCI is an HF-transformer-isolated topology. The voltage step up in the DMCI topology is due to a combination of the boost action of the Ćuk module and the turns ratio of the HF transformer. The DMCI uses four low-side driven GaN-FETs, which reduces the complexity of gate-driver design. The continuous input current helps in reducing the capacitance across the PV modules, thereby improving the system reliability.

In this paper, two key issues related to a GaN-FET-based DMCI are analyzed and solutions are proposed. One of the issues relates to the lower order harmonic distortion in the output grid current. The other issue pertains to the HF noise in the DMCI topology.

A. Overview of the Issue of Lower Order Harmonic Distortion

It is known that the boost-derived differential-mode inverter (DMI) topologies result in a lower order harmonic generation [4]–[8]. These harmonics are generated due to the nonlinear input–output relation of the boost-derived inverters and the adopted modulation methodology. The occurrence of the lower order harmonics in continuously modulated DMIs is reported in the literature [4]–[12]. Control techniques specific to the issue of harmonic attenuation are considered in [9]–[12]. These are advanced control techniques and their implementation may require high computation power. Hence, there can be a requirement of fast DSPs or high-end FPGAs, which is undesirable in cost-sensitive microinverter applications.

This paper looks into this issue in a topologically switched DMCI. The topological switching is also termed as discontinuous modulation scheme (DMS). The DMS results in a reduction in the overall losses and enhanced efficiency [13]. Reduction in

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losses also leads to a possible reduction in the heat-sink size, and hence, the inverter volume and cost may also be reduced.

The harmonic spectrum of the DMCI output voltage is analyzed for ideal and practical cases. It is shown that there can be significant lower order odd and even harmonics. The odd harmonics are due to the nonlinearity of the DMCI, whereas the even harmonics are due to the mismatch in the individual HF transformer isolated Ćuk modules of the DMCI. A similar observation is made in a continuously modulated differential-mode buck inverter [14]. The lower order harmonics issue becomes critical in the grid-connected operation of any DMI. This is because there is practically negligible damping offered to any harmonics by the grid. In order to operate the grid-connected DMCI with minimal harmonic distortion, a suitable closed-loop control needs to be developed.

To address the grid current distortion due to the nonlinearity of the DMCI, typically a static inverse transformation is used [6], [15]. Practically, however, it is shown in this paper that this method alone cannot handle the distortion issue effectively because of the additional even harmonics generated. There are also additional odd harmonics due to nonidealities such as dead-time. Hence, in this paper, a combination of the static inverse transformation and multiresonant controller is considered. Even though the multiresonant controller is known in the literature, its design in a DMCI poses challenges. In this context, a systematic design method is developed in this paper for selecting the controller parameters. It is shown that, there is stable operation and a significant reduction in the harmonic distortion when the proposed control design is used.

B. Overview of the Issue of HF Noise

In comparison to Si MOSFETs, GaN-FETs offer much high slew rates, low turn-on resistance, and much smaller output capacitance. On one hand, these advancements help in achieving increased system efficiency, faster switching frequency, and smaller form factors for power converter designs [16]. On the other hand, high slew rate and low output capacitance of GaN-FETs can excite resonance in the adjoining power electronics circuit causing large voltage spikes and electromagnetic interference (EMI) noise [17]–[20]. Additionally, GaN-FETs have a low threshold voltage of around 1.4 V as compared to 3 V of Si MOSFETs. This makes them more susceptible to false triggering in case of oscillations in the gate driver circuit. Also, the allowable gate-driving voltage range for GaN-FETs is much small as compared to Si devices. For instance, minimum gate drive voltage for complete channel formation in GaN Systems (GS66508P) is specified at 7 V and the gate breakdown voltage is specified as 10 V, resulting in a very small allowable operating voltage range. Meeting such tight performance parameters requires special care while designing the printed-circuit-board (PCB) layouts and selecting power components that can work together and leverage on the advantages provided by the GaN-FETs.

The presence of parasitic inductance on the PCB has been identified as one of the major cause for the generation of the HF noise in circuits [17], [21], [21]–[24]. These works mainly focus on PCB level optimization for achieving a reduced loop inductance and/or an improved gate-drive design. However, very limited work is done to study the effects of the high slew rate of GaN-FETs on other circuit components. It is noted in this paper that for the DMCI topology, the nonideal behavior of the passive components affects the HF noise. Specifically, the behavior of blocking capacitors under high slew rate conditions is studied. It is shown that the high slew rate due to fast switching GaN-FETs increases the noise level due to the nonideal behavior of the blocking capacitors. Hence, to limit the occurrence of the HF noise, power-loop design, gate circuit PCB layout guidelines, and the selection of blocking capacitors are provided in this paper.

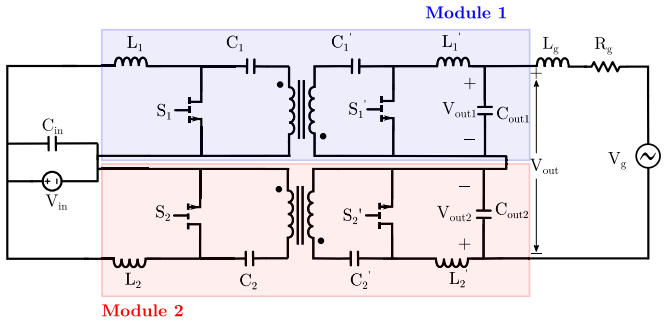


Fig. 1. Grid-connected DMCI topology.

II. DMS-Based DMCI Topology and Operation

Single-phase DMCI topology connected to the grid is shown in Fig. 1. It consists of two identical HF transformer-isolated Ćuk converter modules with input-parallel and output-series connection. In Fig. 1, L_g and R_g correspond to the lumped grid impedance including the wires connecting the DMCI to the point of common coupling of the grid. The topology uses four low-side GaN-FETs and has the advantage of being modular.

Commonly used modulation for DMCI type of inverters is the continuous modulation scheme (CMS) [7], [25], [26]. In this type of modulation, both the Ćuk modules have a dc operating point. A large signal ac perturbation is given to the duty ratio to realize ac voltage in the differential output voltage. With this modulation, both the Ćuk modules will be switching at all the times. As analyzed in detail in [13], this results in circulating power between the modules and has a negative impact on the system efficiency.

In this paper, topological switching is considered for the DMCI. In topological switching, each Ćuk module is active for one-half of the fundamental cycle [13]. This modulation is called DMS. The DMS does not have any circulating power. The device ratings are also lower for the DMS compared to CMS. The advantages of the DMS over CMS are quantified in [13]. With reference to Fig. 1, this modulation can be explained qualitatively as follows. For the positive half cycle of the inverter voltage, module 1 is switched. The duty ratio command is given such that this module generates a half-sinusoidal unipolar voltage. During this period, module 2 is not switching. In module 2, switch S_2 is OFF and S_2' is ON during the complete positive half cycle. Thus, ideally, module 2 produces zero output voltage during this period. Similarly, during the negative half cycle of the desired output voltage, module 2 is switched to realize the necessary output voltage. Module 1 is operated with S_1 OFF and

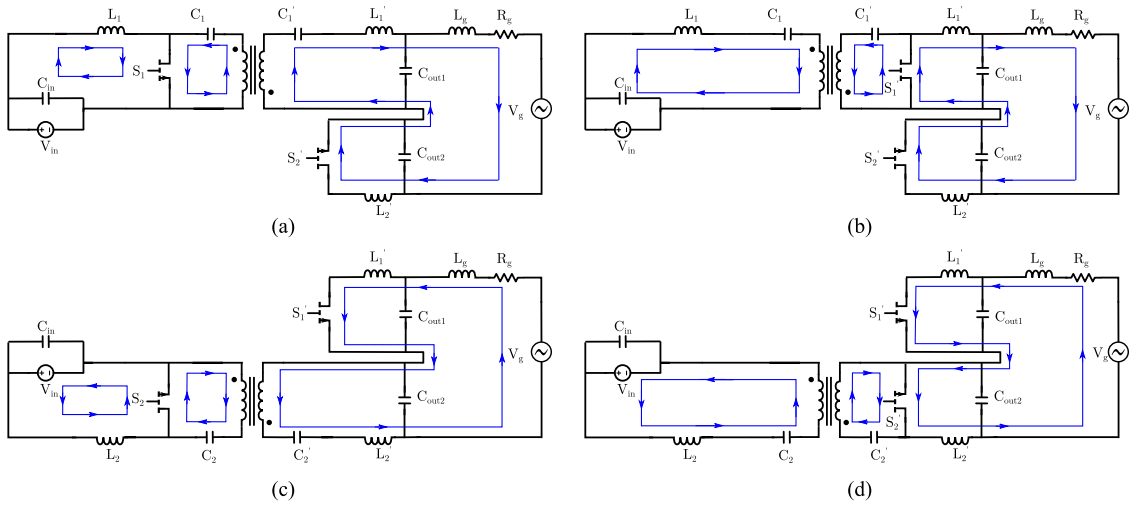


Fig. 2. Modes of operation of the DMCI under DMS for UPF operation. (a) Mode 1, (b) mode 2, (c) mode 3, and (d) mode 4.

S_1' ON so as to produce zero output voltage. As this modulation involves the discontinuous operation of the two modules, it is termed as DMS.

Modes of operation of the DMCI for the DMS for unity power factor (UPF) operation are shown in Fig. 2. During mode 1, shown in Fig. 2(a), the DMCI output voltage is positive and the second module is inactive. The primary-side switch S_1 is turned ON and its complementary secondary-side switch S_1' is turned OFF. The secondary-side switch S_2' of module 2 is turned ON to produce zero module 2 output voltage and to support the grid current. The grid voltage and the grid current are positive during this mode. During mode 2, shown in Fig. 2(b), S_1 is turned OFF and S_1' is turned ON. The second module continues to have S_2' turned ON. During modes 3 and 4, the output voltage is negative. For the UPF operation, the grid current is also negative in this period and the first module is inactive. Its secondary-side switch S_1' is turned ON produce zero module 1 output voltage and to support the grid current. Fig. 2(c) and (d) shows the operation in modes 3 and 4, respectively. The negative output voltage of the DMCI is generated using the second module. It can be seen that the DMCI output voltage is supported alternately by modules 1 and 2 depending on the polarity of the overall output voltage V_{out}. Hence, any mismatch in the modules will be reflected in the DMCI output voltage. The effect of the mismatch is primarily in the generation of dc offsets and even harmonics. This effect is described in detail in Section III.

III. Lower Order Harmonic Distortion Issue and Solution

In this section, the occurrence of lower order harmonics in a DMCI is described. The effect of nonidealities on the lower order harmonics in a practical DMCI is explained. This is followed by the discussion on the required closed-loop control method for the stable operation of the DMCI in grid-connected mode with reduced harmonic distortion. A systematic design method is proposed for the selection of the control parameters based on a small-signal model that is developed for the DMCI for the grid-connected case.

A. Occurrence of the Lower Order Harmonics

The output to input relation for the DMCI modules under the DMS, averaged over a switching cycle is given by

$$\frac{V_{\text{out1}}}{V_{in}} = \frac{nD_1}{1-D_1};\quad \frac{V_{\text{out2}}}{V_{in}} = \frac{nD_2}{1-D_2} \tag{1}$$

where n is the transformer turns ratio; and D_1 and D_2 are the duty ratio commands given to module 1 and module 2 of the DMCI, respectively. Quasi-static assumption is used in arriving at (1) as the switching frequency is very high compared to the fundamental frequency of the DMCI output voltage [13]. As each module operates for one half of the fundamental cycle in the DMS, the natural choice for the duty ratio reference for each module is as shown in Fig. 3.

The overall output of the DMCI is given by

$$V_{\text{out}} = V_{\text{out1}} - V_{\text{out2}}. \tag{2}$$

Ideally, the DMCI output voltage is expected to be sinusoidal. However, due to the nonlinearity in (1), half-sinusoidal duty ratios as in Fig. 3, will not result in half-sinusoidal module output voltages in the DMCI. The individual module voltages for the half-sinusoidal duty ratio are determined using (1) and are shown in Fig. 4. By visual inspection of Fig. 4, it is clear that the output module voltages contain significant lower order harmonics due to the nonlinearity of (1). Each module output contains a dc component, even harmonics, and odd harmonics. The magnitude and phase spectrum of the two module voltages is shown in Fig. 5.

It can be observed from Fig. 5(a) and (b), that the fundamental and the odd harmonics are phase shifted by 180° between the modules. However, the dc component and the even harmonics have zero phase shift between the modules. As the output is synthesized in a differential architecture as indicated in (2), the DMCI output voltage ideally contains only the odd harmonics. The differential output for half-sinusoidal duty ratios is shown in Fig. 6. The total harmonic distortion (THD) is determined as 19.7% which is high.

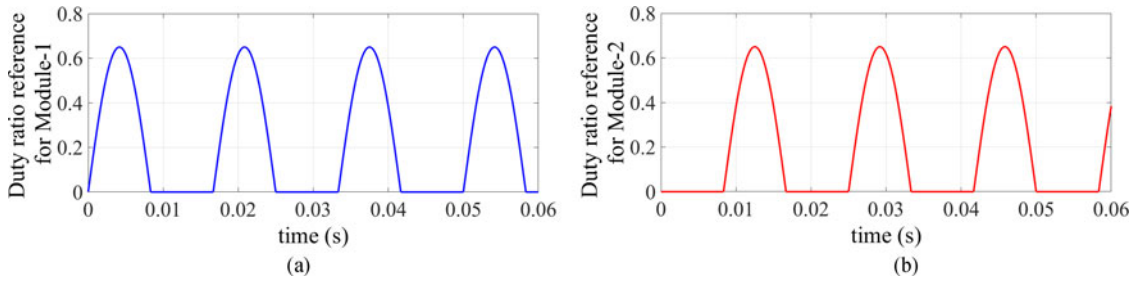


Fig. 3. Half-sinusoidal duty ratio reference. (a) D_1 for module 1 and (b) D_2 for module 2 of the DMCI operating under the DMS.

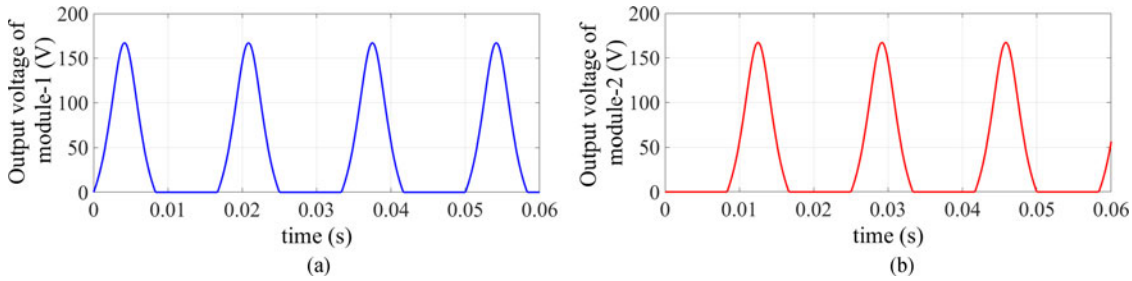


Fig. 4. Output voltages of DMCI modules for half-sinusoidal duty ratio reference. (a) Module 1 and (b) module 2.

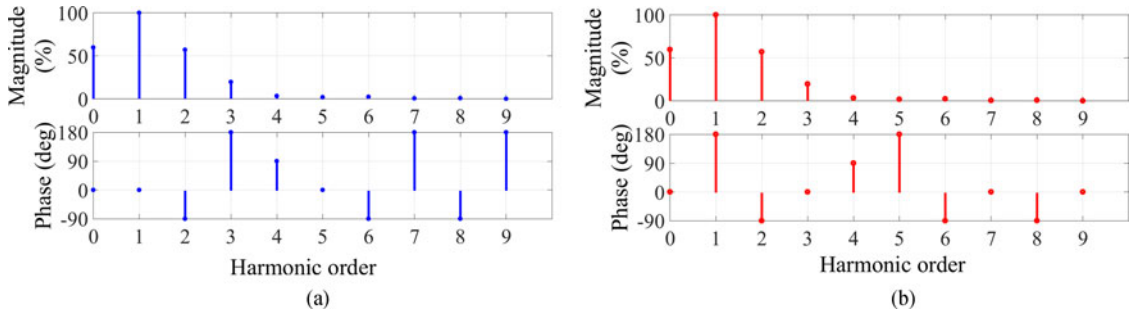


Fig. 5. Output voltage spectrum of DMCI modules for half-sinusoidal duty ratio reference. (a) Module 1 and (b) module 2.

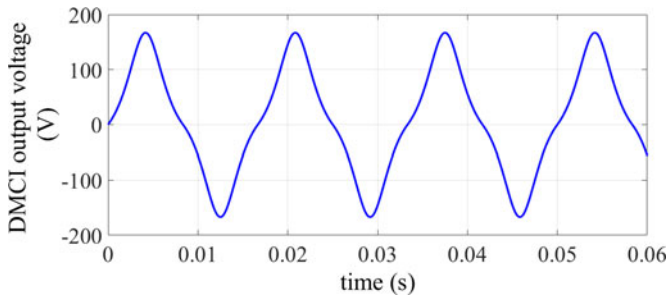


Fig. 6. Output differential voltage of DMCI modules for half-sinusoidal duty ratio references.

1) Occurrence of Even Harmonics in the DMCI Output Voltage: Ideal DMCI output voltage does not contain any even harmonics. This is because, even though individual modules produce even harmonic voltages, they get canceled out in the differential output voltage. Practically, however, it is observed that the DMCI output may contain even harmonics due to the mismatch in the output voltages produced by the two modules. This is due to the mismatch in various components in the modules such as mismatch in the GaN-FETs, mismatch in the impedances of the passive elements, and mismatch in the HF transformers built for each module. The even harmonic voltages can have the following form for each module:

$$V_{\text{out1}}(2h) = \hat{V}_{\text{out1}}(2h)/\underline{\theta_1(2h)};\;\; V_{\text{out2}}(2h) = \hat{V}_{\text{out2}}(2h)/\underline{\theta_2(2h)} \tag{3}$$

where $V_{\text{out1}}(2h)$ is an even harmonic voltage for the first module. The harmonic order is represented as $2h$, where h is an integer and $h \geq 1$. This voltage is expressed in the phasor form with an amplitude of $\hat{V}_{\text{out1}}(2h)$ and a phase of $\theta_1(2h)$. Similarly, $V_{\text{out2}}(2h)$ represents the corresponding even harmonic voltage of the second module. It has an amplitude of $\hat{V}_{\text{out2}}(2h)$ and a phase of $\theta_2(2h)$.

For ideal case, $\hat{V}_{\text{out1}}(2h) = \hat{V}_{\text{out2}}(2h)$ and $\theta_1(2h) = \theta_2(2h)$ for all h. Hence, the output differential voltage $V_{\text{out1}}(2h) - V_{\text{out2}}(2h)$ equals zero. Practically, there can be mismatch in either amplitudes $\hat{V}_{\text{out1}}(2h)$ and $\hat{V}_{\text{out2}}(2h)$ or phases $\theta_1(2h)$ and $\theta_2(2h)$ or both. This would essentially result in a non-zero even harmonic voltage in the output of the DMCI.

For stand-alone systems where the DMCI feeds a load, the problem of even harmonics is negligible as the load may offer sufficient impedance to attenuate the differential even harmonic voltages. However, in the grid-connected mode, the grid appears practically as a very low impedance for the harmonic voltages generated by the DMCI. Hence, even a small even harmonic voltage can result in considerable even harmonic current injected to the grid, hence, negatively affecting the THD of the output current of the DMCI.

2) Occurrence of a DC Offset in the DMCI Output Voltage: Each module of the DMCI produces a dc voltage as seen in the spectra shown in Fig. 5. Ideally, it does not appear in the differential output voltage as both the modules produce identical dc offset. Practically, as in the case of even harmonics, mismatch between the modules may cause a resultant dc offset in the DMCI output voltage. This results in dc injection to the grid, which is undesirable. Hence, the closed-loop DMCI control technique must ensure that the dc injection to the grid is negligible.

B. Closed-Loop Control of the Grid-Connected DMCI

DMCI output voltage contains odd harmonics due to the inherent nonlinearity of (1). Practical DMCI output voltage may contain even harmonics and dc offsets due to module mismatch. Hence, the closed-loop control for the DMCI should be able to mitigate these undesired quantities. Typically, in any stand-alone boost-derived converter, a static-inverse-transformation is used to cancel the nonlinearity in the output-to-input relation given in (1). This transformation between the duty ratio and output voltage for each module of the DMCI can be defined as follows [6], [15]:

$$D_1 = \frac{V_{\mathrm{ref1}}}{V_{\mathrm{ref1}} + n\frac{V_{\mathrm{in}}}{m}};\;\; D_2 = \frac{V_{\mathrm{ref2}}}{V_{\mathrm{ref2}} + n\frac{V_{\mathrm{in}}}{m}} \tag{4}$$

where V_{ref1} and V_{ref2} are the half-sinusoidal voltage references; and D_1 and D_2 are the duty ratio commands to the DMCI modules. Using (4) in (1), the output module voltages are determined as

$$V_{\mathrm{out1}} = mV_{\mathrm{ref1}} \tag{5}$$

$$V_{\mathrm{out2}} = mV_{\mathrm{ref2}} \tag{6}$$

The voltage references V_{ref1} and V_{ref2} are half-sinusoidal signals defined as follows for any integer j:

$$V_{\mathrm{ref1}} = \begin{cases} \sin\omega_0 t, & \text{if } 2j\pi \le \omega_0 t < (2j+1)\pi \\ 0, & \text{if } (2j+1)\pi \le \omega_0 t < 2(j+1)\pi \end{cases} \tag{7}$$

$$V_{\mathrm{ref2}} = \begin{cases} 0, & \text{if } 2j\pi \le \omega_0 t < (2j+1)\pi \\ -\sin\omega_0 t, & \text{if } (2j+1)\pi \le \omega_0 t < 2(j+1)\pi. \end{cases} \tag{8}$$

The differential output voltage of the DMCI using (5) and (6) in (2) is given by

$$V_{\mathrm{out}} = m(V_{\mathrm{ref1}} - V_{\mathrm{ref2}}) = mV_{\mathrm{ref}}. \tag{9}$$

Using (7) and (8) in the aforementioned equation

$$V_{\mathrm{out}} = m\sin\omega_0 t \;\; \forall\, \omega_0 t. \tag{10}$$

It can be seen from (9) and (10) that the DMCI output voltage is sinusoidal and directly proportional to the controller output V_{ref}. Thus, the transformation in (4) results in the elimination of the odd harmonics due to the converter nonlinearity. Normally, m in (4) is taken as the nominal grid voltage peak that can be estimated using a phase-locked loop (PLL). This transformation is called static-inverse-transformation as it works on an average-basis over a switching cycle.

Practically, the odd harmonics are due to a combination of the DMCI nonlinearity and nonideal factors such as deadtime used between the switching transitions of the GaN-FETs of each DMCI module. In addition, there are even harmonics and dc offsets that cannot be eliminated using the static-inverse-transformation alone. The harmonics due to deadtime, even harmonics due to module mismatch are considerably smaller compared to the harmonics due to converter nonlinearity. Hence, in stand-alone systems they can be negligible due to the damping offered by the load. In the grid-connected mode, there is limited damping. Consequently, large distortion may be seen due to these factors. Hence, static inverse transformation alone may not address the lower order harmonics problem in a grid-connected DMCI.

Thus, based on a practical standpoint, a multiple proportional-resonant (MPR) controller along with a static inverse transformation is proposed for the control of the DMCI in grid-connected mode. An MPR controller refers to a fundamental proportional resonant (PR) controller, designated as PR1, and harmonic controllers *R*2, *R*3, and *R*5 to address the second, third, and fifth harmonic components, respectively. An additional integral controller is included to eliminate dc offsets due to module mismatch. Block diagram of the proposed control of DMCI is shown in Fig. 7. The fundamental current reference is represented as I_g^*. The reference for all the harmonics is fixed at zero. The outputs of PR1 and the resonant controllers are added to a feedforward term V_{ff}. This feedforward is taken as normalized grid voltage signal. That is, if m is grid voltage amplitude and V_g is the instantaneous grid voltage, $V_{ff} = V_g/m$. This helps in reducing the effect of grid voltage harmonics in the output current of the DMCI [27].

In the steady state, the MPR and integral controllers ensure that the grid current I_g follows the reference I_g^*. The corresponding steady-state voltage reference V_{ref} in Fig. 7 is sinusoidal. It is converted into half-sinusoidal references using the module reference selector block indicated in Fig. 7. The resulting half-sinusoidal references V_{ref1} and V_{ref2} are fed into the static inverse transformation of (4) to obtain the duty ratio commands D_1 and D_2, respectively. These duty ratio commands are applied to the respective modules of the DMCI. Following the discussion using (4)–(10), the output voltage of the DMCI is sinusoidal. This voltage interacts with the grid voltage V_g and grid impedance to realize the required grid current I_g. It must be noted that in Fig. 7, depending on the polarity of V_{ref}, either module 1 or module 2 is active. Hence, in the system dynamics, only one of the DMCI module is involved. The inactive

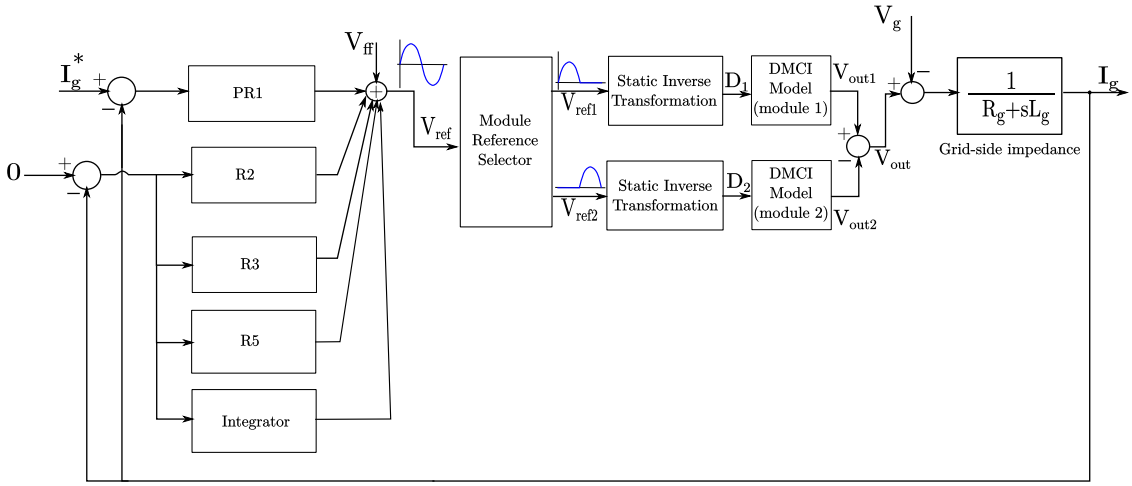


Fig. 7. Closed-loop control of the grid current in a grid-connected DMCI with MPR, integrator, and static inverse transformation.

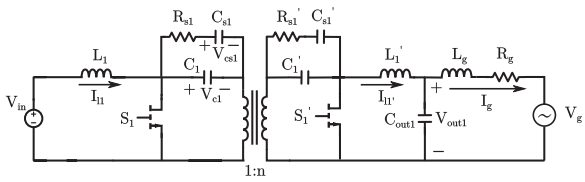


Fig. 8. Circuit schematic of a module of the DMCI operating in a given fundamental half cycle. All the state variables (I_{l1}, I_{l2}, V_{c1}, $V_{\text{out}1}$, and V_{cs1}) have been labeled.

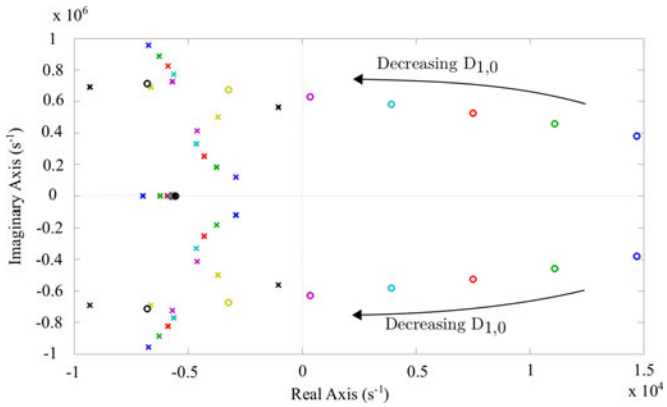


Fig. 9. Pole-zero map of DMCI as $D_{1,0}$ is varied. Poles are marked using cross ($\times$) and zeros are marked using circles ($\circ$). The right-half plane zeros exist for $D_{1,0} > 0.3$.

module ideally operates with zero voltage as described in Section II. This needs to be taken into account while designing the proposed controller parameters.

Other advanced controllers such as repetitive controller can be used to achieve the same objective of grid current control with minimal harmonic distortion. However, the advanced control schemes are not preferred for the low-cost DMCI as they add to control complexity, enhanced computation overhead, and sensing and/or estimation requirements. Another conventional control approach is to use only MPR controllers, i.e., without the static inverse transformation to address all the significant odd and even harmonics. An integrator can be included to eliminate the dc offset. However, such an approach requires significantly large number of resonant controllers. Typically at least about 13 resonant controllers will be required to eliminate all the harmonics due to converter nonlinearity. This also increases the computational burden for the digital controller used.

1) Small-Signal State-Space Model for a Module of the DMCI: In DMS, each DMCI module operates under HF switching for one half cycle of every fundamental. The circuit schematic of module 1 that is switching is shown in Fig. 8. Module 2 has its output switch turned ON, and hence, produces a zero voltage. As the grid current contains fundamental and lower order harmonics, it can be considered as constant over a switching cycle. The DMCI blocking capacitors C_1 and C_1' are connected to a damping RC branch, as done typically in Ćuk converters [28]. This branch is especially needed in the grid-connected operation of DMCI to provide better damping. The value of the damping branch in the primary side is selected iteratively as $R_{s1} = 8\ \Omega$ and $C_{s1} = 22\ \mu$F. The secondary-side damping branch impedances are selected by scaling as per the transformer turns ratio squared, that is, the resistance is scaled up by a factor of 4 and the capacitance is scaled down by a factor of 4, as the turns ratio is 1:2.

The state equations for module 1 of the DMCI are derived in the Appendix A. Note that identical set of equations are derived for module 2, when it is active. These equations are used to determine the transfer function between the output voltage of a DMCI module and its duty ratio, as described in Appendix B. The system matrix A_1 of the state-space model of the DMCI module 1, derived as (A.15) in Appendix A.

As it can be observed from (A.15), the eigenvalues are functions of the quiescent operating duty ratio $D_{1,0}$ that has wide variation in inverter applications. Hence, the control design must ensure that the system is stable for all the operating range of $D_{1,0}$. Note that the quiescent operating point is defined as: $D_1 = D_{1,0} + \tilde{D}_1$, with $\tilde{D}_1$ being the perturbation around the duty ratio variable.

2) Selection of the Controller Parameters: In Fig. 7, static inverse transformation, MPR and the integral blocks are used for harmonic and dc offset elimination from the grid current.

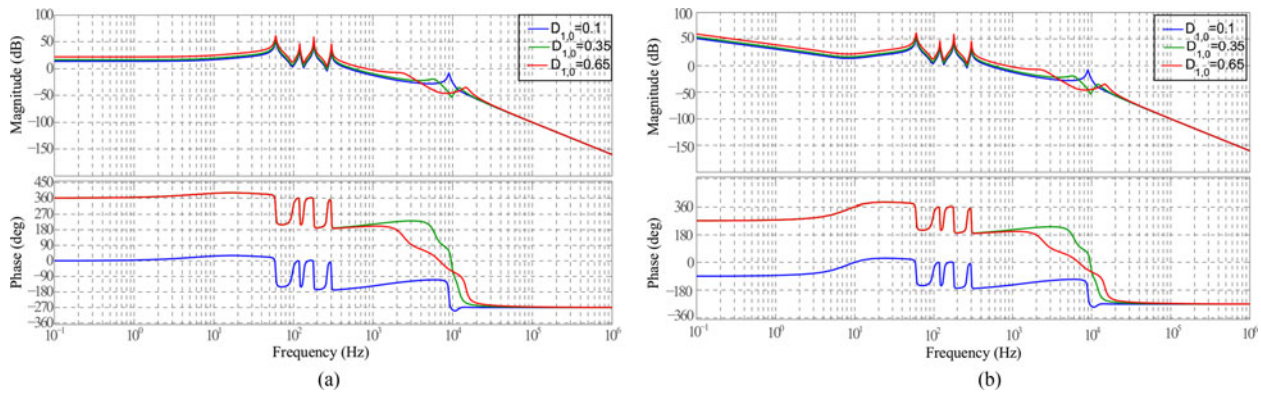


Fig. 10. Bode plot of the forward path transfer function of a DMCI module for output voltage to duty ratio transfer function for different quiescent values of $D_{1,0}$ (a) without an integrator and (b) with an additional integrator. The transfer functions are provided in Appendix B.

The transfer function expressions for the MPR and integral controllers are shown in (B.1) in Appendix B. The control design approach involves the following steps:

1) determining the maximum allowable controller bandwidth for stable operation of the DMCI;
2) selection of the controller gains (MPR + integrator) to ensure stable operation for all the operating points of the DMCI.

Maximum allowable bandwidth places a limit on the number of multiresonant controllers that can be used from the standpoint of stability. For example, if the maximum bandwidth is determined to be 200 Hz, then resonant controllers up to third harmonic (180 Hz) are only feasible. The addition of higher harmonic resonant controllers will significantly reduce the system phase margin and may lead to instability. To determine the maximum possible number of resonant controller blocks, the following procedure is proposed in this paper. For a wide variation of quiescent $D_{1,0}$, the pole-zero map of the DMCI module transfer function given in (B.4) is studied. Note that the same analysis is repeated for module 2 of the DMCI. For control design purpose, the modules are identical. Hence, the following design approach considering module 1 is also applicable to module 2. As the DMCI is boost derived, it contains right-half plane zeros (RHZs). Typically, the bandwidth for the closed-loop control is selected to be at least one decade less than the RHZ location to ensure stability. In the DMCI, the RHZ move depending on the value of $D_{1,0}$. The variation of all the pole-zeros of the transfer function in (B.4) is shown in Fig. 9.

It is observed that, the lowest frequency of the RHZ for the operational range of $D_{1,0}$ is approximately 6.5 kHz. Hence, the bandwidth of the closed-loop DMCI must be at least one decade less than this value for stable operation. Thus, the ideally suitable limit on bandwidth is given by

$$\omega_{\text{bw}} < 650 \text{ Hz}. \tag{11}$$

Practically, a bandwidth of up to 1 kHz may be feasible without significantly affecting the performance of the DMCI. This is because the practical DMCI has a higher damping than what is modeled using Fig. 8. In the practical control implementation, only up to fifth harmonic has been used in this paper as indicated in Fig. 7 because it yields satisfactory results and further improvement in the phase margin.

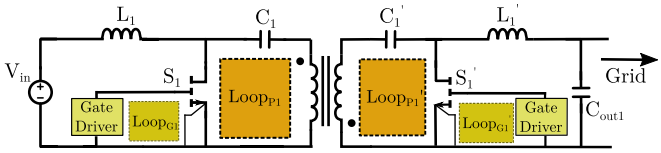


Fig. 11. Single module of a DMCI with marked gate loops Loop_{G1} and $\text{Loop}_{G1}{}'$ and HF power loops Loop_{P1} and $\text{Loop}_{P1}{}'$.

To select the MPR controller parameters, the following iterative approach is developed. First, the DMCI module is considered to be linear with the of $G_{\text{lin}} = \frac{V_{g,\text{peak}}}{V_{\text{ref,peak}}}$. It is assumed that the transformation in (4) leads to this linear gain. Next, following the design procedure in [29], preliminary values of k_p and k_r are determined for the fundamental PR controller, PR1. The transfer functions of PR1 with k_p and k_r, and the resonant blocks are given in (B.1) in Appendix B. These values are adjusted to obtain a bandwidth as per the limit specified in (11). Then, the resonant controller gains R_2, R_3, and R_5 for harmonic compensation are tuned in the range of the k_r determined for PR1. The tuning of gains is so done such that the phase margin for the closed-loop DMCI is not too low for a wide variation of $D_{1,0}$.

The Bode plots of the forward path transfer function or loop-gain comprising PR1, R_2, R_3, R_5, DMCI model and grid impedance are shown in Fig. 10(a) when no integrator is used. Addition of an integrator with a very small gain alters the Bode plot at very low frequencies, as shown in Fig. 10(b). The integrator gives a very high gain at dc so that any dc offset due to mismatch in the module voltages is eliminated in the steady state. With the proposed design, the phase margin is higher than 20° for a wide variation of the duty ratio $D_{1,0}$. Practically, the phase margin obtained is higher due to additional damping elements such as the series resistance of the inductors and transformer etc.

IV. HF Noise Issues and Solutions

This section describes the occurrence of HF noise in a DMCI. Major sources leading to the HF noise injections are identified and suitable solutions are provided to minimize them.

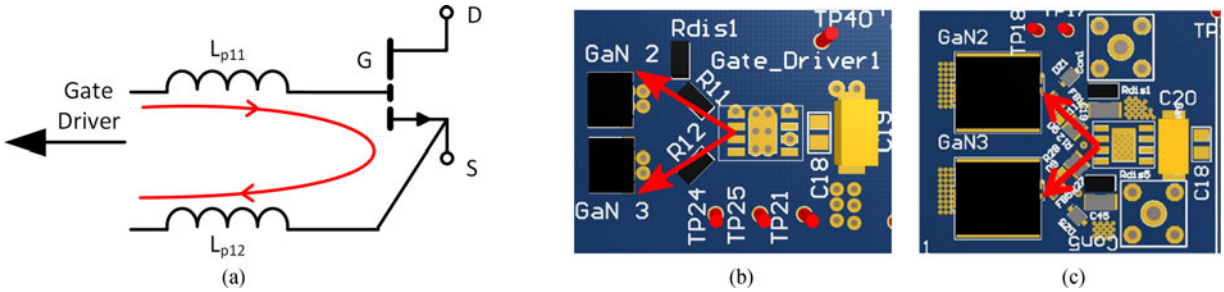


Fig. 12. (a) Schematic drawing showing the location of HF parasitic inductance L_{p11} and L_{p12} in the gate driver loops Loop_{G1} and $\text{Loop}_{G1}{}'$. (b) Primary-side gate driver PCB design for the DMCI implemented using GaN Systems GS66506T and (c) GS66508P as the switching device. The direction of gate-driver current is marked in the event of turn ON.

A. *Occurrence of HF Noise Due to PCB Layout*

In a single module of the practical DMCI circuit, as shown in Fig. 11, there are four major current loops comprising of parasitic inductances that may have a significant impact on the performance of the DMCI. The HF power loops are captured by Loop_{P1} and $\text{Loop}_{P1}{}'$ and mainly comprise of the parasitic inductance between the blocking capacitors, GaN-FET, and HF transformer. The gate driver loops are identified by Loop_{G1} and $\text{Loop}_{G1}{}'$ for the primary- and the secondary-side devices, respectively. They mostly include the parasitic inductance between the gate terminal of the device and the source.

In the past, the effect of parasitic inductance in the HF power loops Loop_{P1} and $\text{Loop}_{P1}{}'$ have been widely studied and given prime importance as it directly affects the switching transition voltage of the FETs and limit their switching frequencies [20], [30], [31]. However, recently after the introduction of GaN-FETs, limiting the parasitic inductance in gate-driver loop Loop_{G1} and $\text{Loop}_{G1}{}'$ has also surfaced as a major concern [32]. This is primarily because of the low threshold and maximum allowable gate voltage for a GaN-FET. As compared to a conventional Si MOSFET, a typical GaN-FET has approximately 10 times lower difference between the optimal and maximum allowable gate voltage and about 4 times lower threshold voltage. This leaves a very limited margin for voltage oscillations in the gate-driver loop. So, if these gate oscillations are not controlled they may lead to false turn ON of the GaN-FETs or can permanently damage them. Hence, one of the key objectives while designing a GaN-FET-based power electronics system is to keep the parasitic inductance in the gate-driver loop minimum.

One way to limit this parasitic inductance in an HF circuit is to design a well laid out PCB. Fig. 12(a) shows the HF parasitic model of the gate-driver circuit with parasitic inductance in Loop_{G1} marked as L_{p11} and L_{p12}. To capture the effect of gate-loop parasitic on the DMCI, two different gate-driver PCB layouts are designed employing GaN Systems GS66506T and GS66508P FETs as shown in Fig. 12(b) and (c), respectively. To achieve a better HF performance, in Fig. 12(c) component are so placed such that, the distance between the output of the gate driver and the gate terminal of the GaN-FET is minimized. This, along with the presence of Kelvin source in GS66508P, may help reduce parasitic inductance in the driver loop considerably. Table I provides a measure of the parasitic inductance in the two circuits shown in Fig. 12(b) and (c) at a switching frequency of 100 kHz. Whereas, Fig. 13 provides its variation as a function of frequency signal varying between 100 kHz to 200 MHz. Parasitic inductance were obtained using finite-element-analysis-based design software EMCoS.[1] From Fig. 13, it can be observed that, the minimum gate-loop parasitic inductance for PCB using GS6650T GaN-FETs is about 9.5 nH at 200 MHz, which is higher than the maximum parasitic inductance of the PCB using GaN Systems GS66506T FETs. To further attenuate the HF oscillations in the gate-driver loop for the PCB employing GS66508P GaN-FETs, surface mounted ferrite beads were added before the gate terminal of the device. Further, parallel operation of the GaN-FETs requires a carefully designed PCB layout. As GaN-FETs have the capability to operate with a small rise and fall times of 3.7 and 5.2 ns, respectively [33], inter-trace signal delays can cause an imbalance in dynamic current sharing between the FETs connected in parallel. To avoid this problem, driver-loop length to all the parallel FETs should be identical. Fig. 12(b) and (c) outline the PCB layout designed for connecting two GaN-FETs in parallel.

TABLE I
PARASITIC INDUCTANCE OF THE GATE-DRIVER CIRCUIT AT THE NOMINAL SWITCHING FREQUENCY OF 100 KHZ

Device	L_{p11}	L_{p12}
GS66506T	3.64 nH	6.58 nH
GS66508P	2.2 nH	5.92 nH

B. *Occurrence of HF Noise Due to High Slew Rate*

The low output capacitance of the GaN-FET may undergo resonating interaction with the parasitic inductance present in the power loops (Loop_{P1} and $\text{Loop}_{P1}{}'$). This may lead to the generation of HF noise in the form of voltage oscillations across the FET drain and source terminals.

As stated earlier, parasitic inductance in the power loops Loop_{P1} and $\text{Loop}_{P1}{}'$ comprise primarily of the transformer

[1]Circuit parasitic elements were extracted using EMCoS PCB VLab v3.2 (http://www.emcos.com/). ODB++ PCB files generated using Altium Designer are directly loaded in the PCB VLab v3.2 and tracks between which parasitic elements were to be measured were defined. RapidRLC solver included in EMCoS PCB VLab package calculates resistance, inductance, and capacitance matrices for complex 3-D geometries and generates lumped equivalent circuit files in SPICE format.

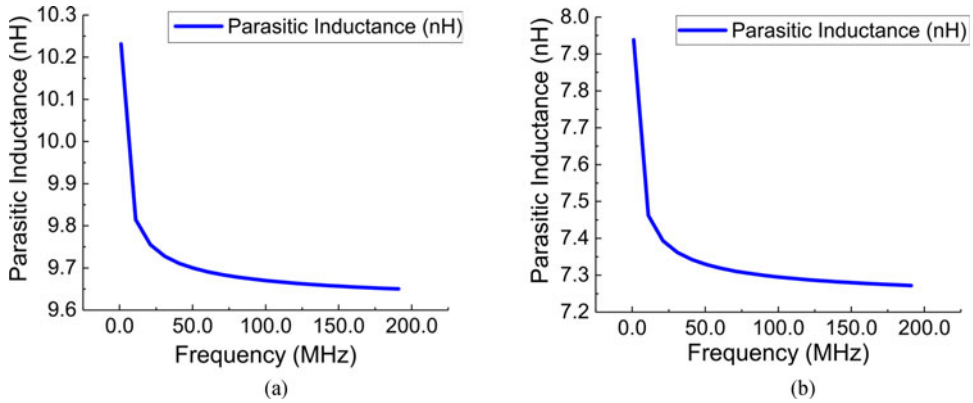


Fig. 13. Simulation result showing the variation of parasitic inductance with frequency in Loop_{G1} for design using (a) GS66506T and (b) GS66508P as the GaN-FET.

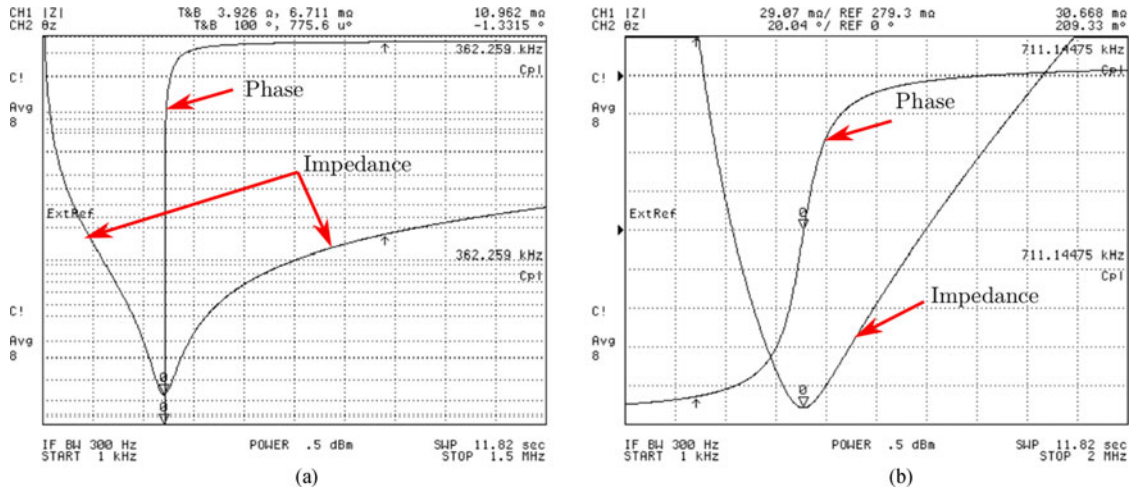


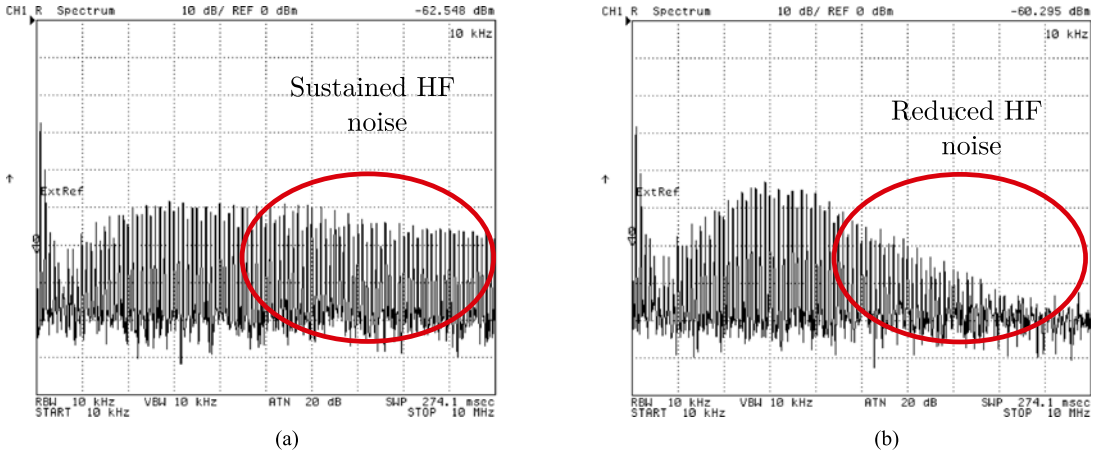
Fig. 14. Impedance magnitude and phase characteristics of (a) C_1 and (b) C_1'.

leakage inductance, device package inductance, and parasitic inductance of the PCB traces. In addition to these, the nonideal behavior of the primary and secondary blocking capacitors in the DMCI also adds to the parasitic inductance present in the power loops. When a power semiconductor device in a power-electronics system undergoes HF switching, HF harmonics are generated, whose frequency depends on the slew rate of the device. Even though most of its signal strength is concentrated near the device switching frequency, higher order harmonics constitute a considerable amount. When such a waveform with a high slew rate is applied to a circuit constituting of the non-ideal passive circuit element, increased conductive EMI noise, and voltage oscillations may be observed.

In Fig. 11, HF power signals are present in the power loops Loop_{P1} and $\text{Loop}_{P1}{}'$, which comprise of the blocking capacitors C_1 and C_1', respectively. Owing to the fast energy capture and release capabilities required by the blocking capacitors, film capacitors with its self-healing ability is found to be a reasonable choice. Capacitor C_1 is chosen to be 5.8 μF (ECW-F2685JA), while C_1' is chosen to be 1.5 μF (B32674D4155K). Impedance response for blocking capacitors C_1 and C_1' are provided in Fig. 14(a) and (b), respectively.

Fig. 14(a) and (b) shows that, the self-resonance frequency for C_1 and C_1' are 362.25 and 711.14 kHz, respectively. As these frequencies are close to the switching frequency of 100 kHz, HF noise components of the switching voltage will encounter different circuit impedances than experienced by the switching frequency component. At the self-resonance frequency, C_1 and C_1' behave as an ideal resistance, however, with increased frequency they start showing inductive nature. This adds to the already present parasitic inductance in the power loops Loop_{P1} and $\text{Loop}_{P1}{}'$ and leads to increased voltage oscillations and conductive EMI noise in the DMCI circuit. Voltage spectrum for a frequency range of 10 kHz–10 MHz across C_1 is provided in Fig. 15(a). It can be observed that, the voltage spectrum comprises of a wide spectrum of HF noise and has its fundamental component (100 kHz) with the maximum amplitude.

A practical solution to this problem is to add an HF ceramic capacitor across the blocking capacitors in the power stage. This HF ceramic capacitor can ensure that a low impedance capacitive path is available to the HF noise components and can in turn limit the parasitic inductance in the power loops. Two 0.1-μF HF ceramic capacitors were added in parallel to the blocking capacitors C_1 and C_1' in the experimental DMCI circuit. Fig. 15(b) provides the spectrum of the voltage across the primary-side blocking capacitor, which now comprises a parallel combination of a film and ceramic capacitor. As is apparent in Fig. 15(b), the spectrum of the voltage across the blocking capacitor has much



(a) (b)

Fig. 15. Experimental spectrum analyzer result for voltage across the primary-side blocking capacitor (a) without a ceramic capacitor in parallel, (b) with a ceramic capacitor in parallel.

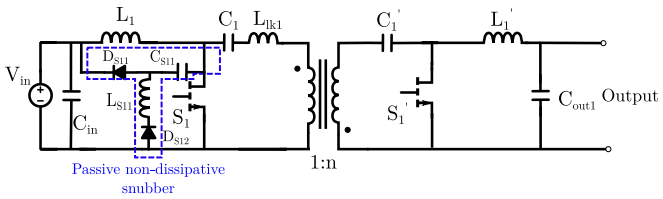


Fig. 16. Schematic of a module of DMCI with a passive snubber.

lower amplitude for the HF noise as compared to Fig. 15(a). It is noted that, due to an increase in the effective inductive behavior of the capacitor combination for midfrequency range, a slight increase in the noise amplitude is observed. However, an overall reduction in the parasitic impedance in Loop$_{P1}$ and Loop$_{P1}{}'$ and conductive EMI noise is observed using this method.

C. *Effect of Snubber Capacitance*

The leakage inductance (L_{lk1}) of the HF transformer cannot be practically made zero. As a result, even with the well-laid-out PCB, there can be HF oscillations resulting in over voltage across the GaN-FETs. Hence, a passive nondissipative diode-based snubber as reported in [34] and [35] for a dc/dc converter is used. In this paper, this snubber has been optimized for the dc/ac operation of the DMCI. The schematic of a single module of DMCI with the passive nondissipative snubber is shown in Fig. 16. This snubber acts as a rate-of-rise control snubber. During turn-off operation of the device, energy from the leakage inductance is diverted to charge the snubber capacitor (C_{s11}) instead of the capacitance of the GaN-FET, thereby reducing the magnitude of voltage spike across the device. Later, when the device turns ON C_{s11} resonates with the snubber inductor (L_{s11}) until the snubber current reaches zero and the diode D_{s12} is reverse biased. Next, when the device turns OFF, this stored energy in L_{s11} is transferred to the source through diode D_{s11}. Hence, The rate of increase of the voltage across the device during turn OFF is primarily controlled by the rate at which a snubber capacitor is charged.

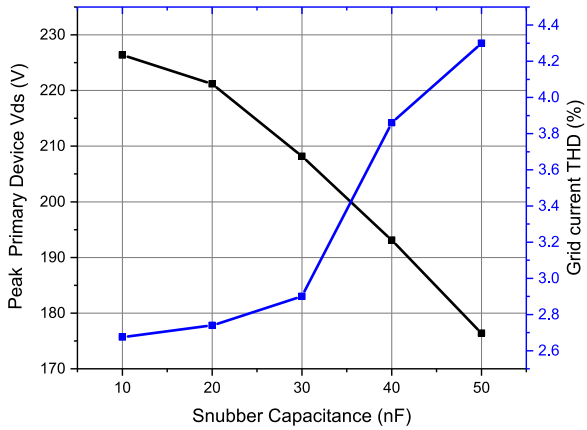


Fig. 17. Effect of snubber capacitance on peak primary device voltage and grid current THD.

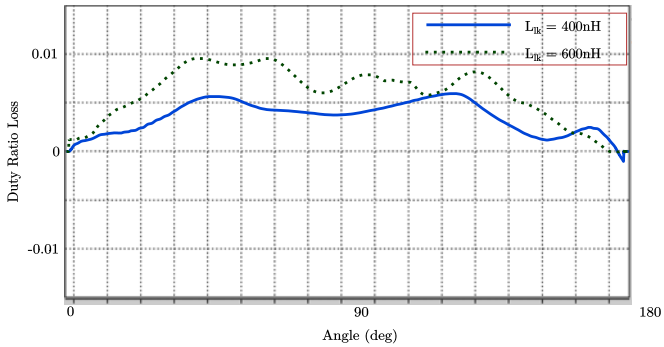
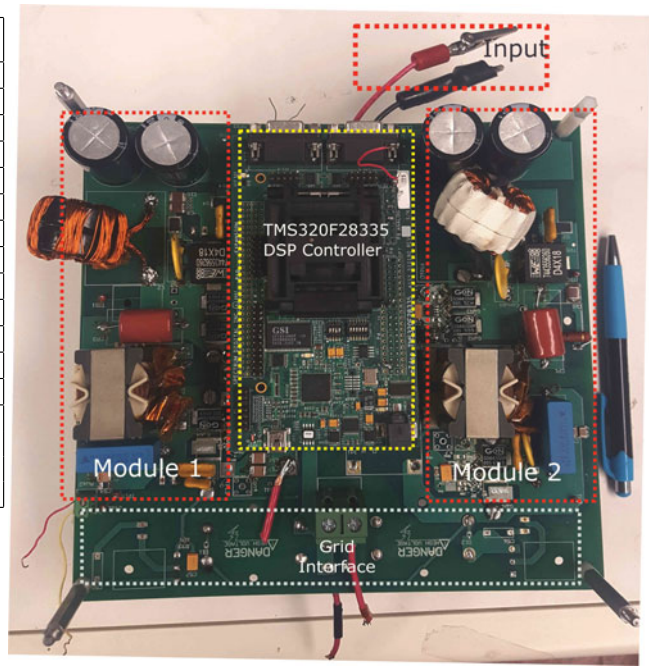


Fig. 18. Loss in the duty ratio as a function of the HF transformer leakage inductance, which manifests as distortion in grid current.

The value of C_{s11} affects the device over voltage and also dictates the duration of dead time to be included in each module. It is to be noted that the dead time affects the lower order harmonics in the grid current [36], [37]. Hence, C_{s11} impacts both higher and lower order harmonic issues in the DMCI. Fig. 17 shows the variation in peak primary device voltage and output grid current THD with the value of C_{s11}.

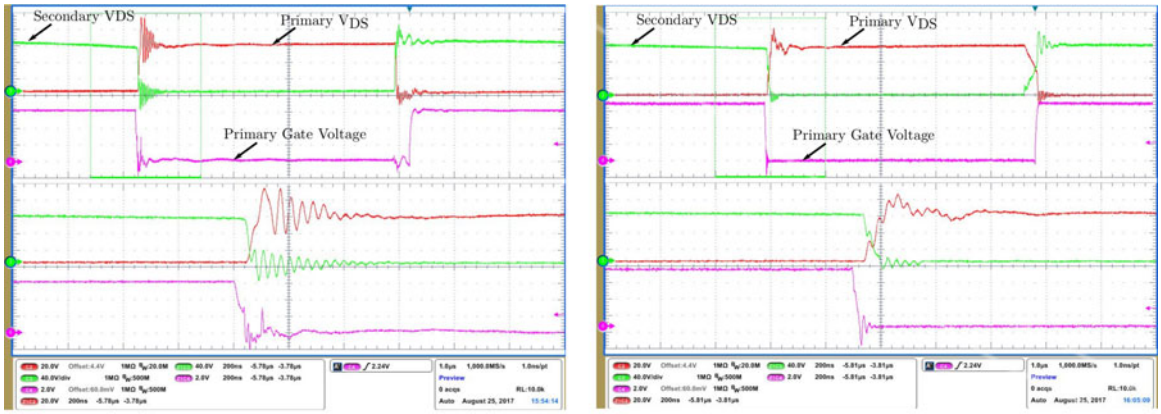
Module and DMCI parameters	Value/ Part number
Input voltage (V_{in})	$35 - 50\ V$
Grid voltage (V_g)	$120\ V_{rms}$
Maximum power rating (P_{max})	$500\ W$
Switching frequency (f_s)	100 kHz
HF transformer turns ratio ($1:n$)	$1:2$
Switching devices (S_1, S_1', S_2, S_2')	GaN Systems GS66508P
Primary side inductance (L_1, L_2)	$50\ \mu$H
Secondary side inductance (L_1', L_2')	$100\ \mu$H
Input capacitance (C_{in})	$4 \times 3300\ \mu$F
Output capacitance (C_{out1}, C_{out2})	$4.4\ \mu$F
Leakage inductance (L_{lk1}, L_{lk2})	$400\ n$H
Magnetizing inductance (L_{m1}, L_{m2})	$100\ \mu$H
Snubber L_{s11} and C_{s11}	$2.5\ \mu$H and $10\ n$F
Controller gains	$k_p = 0.013$, $k_r = 3$ $k_{r2} = 1$, $k_{r3} = 6$ $k_{r5} = 2.3$, $k_I = 0.6$ $\omega_c = 8\ rad/s$

(a)



(b)

Fig. 19. (a) Table listing the module and DMCI parameters of the experimental setup and (b) picture of the DMCI hardware setup.



(a) (b)

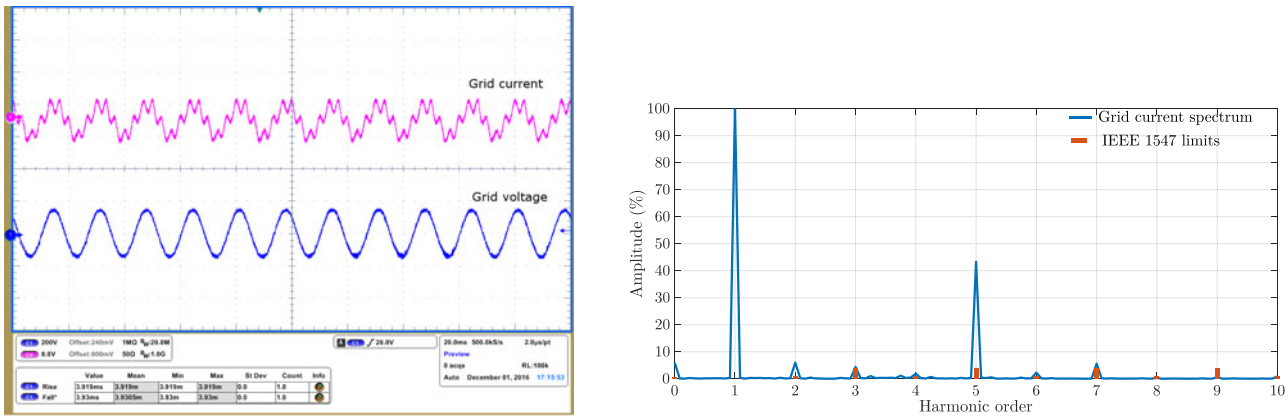
Fig. 20. Primary-side DMCI switching waveform on channel 4 and primary and secondary V_{DS} on channels 2 and 3, respectively, with zoomed view, for the PCB designs employing (a) GaN Systems GS66506T GaN-FETs with a gate loop parasitic inductance of 10.22 nH and (b) GaN Systems GS66508P GaN-FETs with a gate loop parasitic inductance of 8.12 nH.

It can be observed from Fig. 17 that compared to a large value of the snubber capacitor, lower value of the snubber capacitor will tend to absorb the leakage energy fast and will produce a higher voltage spike across the device. Further, using a lower value of the snubber capacitor will also require a lower dead time to be included between the primary- and secondary-side FETs, hence resulting in lower THD in the grid current.

There is an increase in THD of the grid current due to increase in dead time. The magnitude of the dead time is related to the leakage inductance of the HF transformer and C_{s11}. An increase in the leakage inductance increases the lower order harmonics, which are actually a manifestation of the loss in duty ratio when each module is switching. This loss in duty ratio for UPF operation, when module 1 is switching (for a period of $180°$), is shown in Fig. 18. The result shown in Fig. 18 uses a leakage inductance of 200 nH as the reference over which the duty-ratio loss is determined as the leakage inductance is increased to 400 and 600 nH.

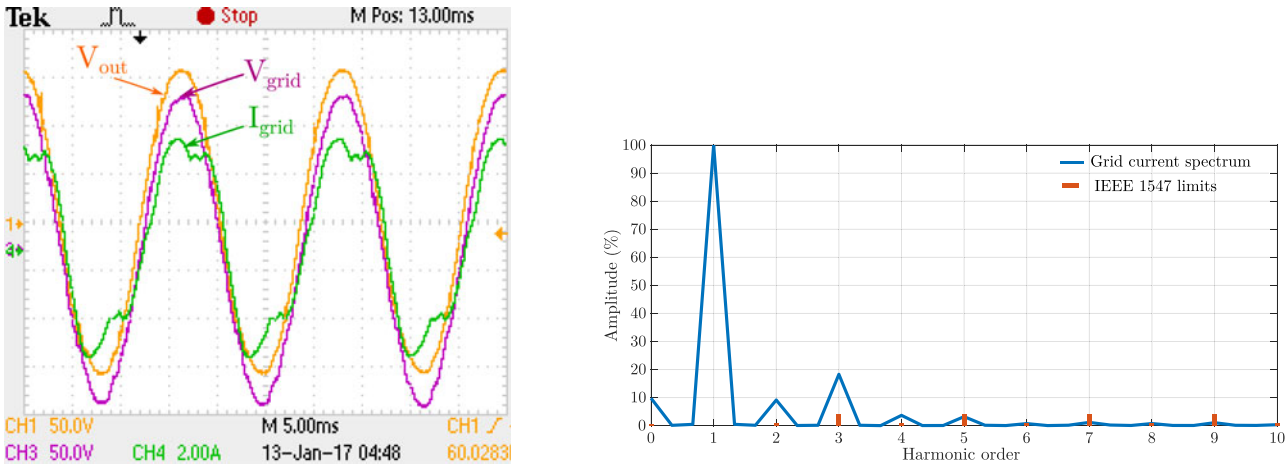
TABLE II
FOUR CASES OF CLOSED-LOOP CONTROL OF THE DMCI

Case	Closed-Loop Control Technique Used
1	PR1 + $R3$
2	PR1 + Static inverse transformation
3	PR1 + $R2$ + $R3$ + $R5$ + $R7$ + $R9$
4	PR1 + Static inverse transformation + $R2$ + $R3$ + $R5$ (Proposed control technique)



(a) (b)

Fig. 21. (a) Experimental result when the current control includes fundamental PR and third harmonic resonant controller blocks (case 1), (b) corresponding spectrum of the grid current. Scale: Grid current (Ch. 4) 8 A/div and grid voltage (Ch. 1) 200 V/div. Horizontal scale: 20 ms/div.



(a) (b)

Fig. 22. (a) Experimental result when fundamental PR + inverse transformation is used (case 2), (b) corresponding spectrum of the grid current. Scale: Grid current (Ch. 4) 2 A/div, grid voltage (Ch. 3) 50 V/div, and $V_{\rm out}$ (Ch. 1) 50V/div. Horizontal scale: 5 ms/div.

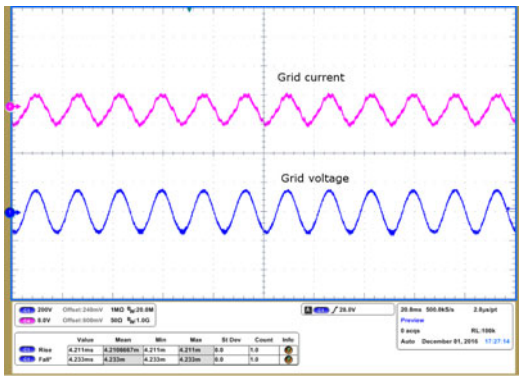
V. Experimental Results

The experimental results are obtained using a GaN-FET-based DMCI. The details of the hardware setup and picture are provided in Fig. 19. The control of the DMCI is implemented using DSP TMS320F28335. For grid-connected mode, a second-order-generalized-integrator-based PLL [38] is used to achieve grid synchronization. The PLL is implemented in the DSP, along with the closed-loop current control method.

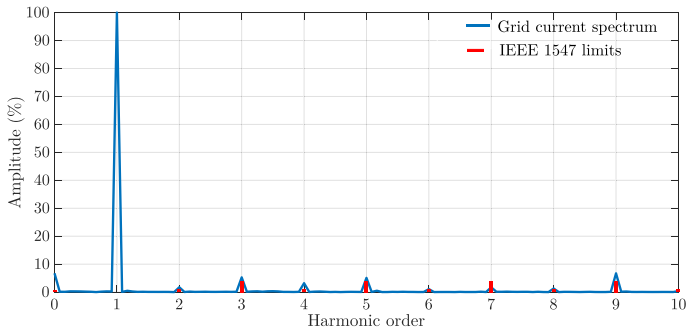
Gate-to-source switching waveform and corresponding drain-to-source voltage ($V_{\rm DS}$) waveforms for the DMCI employing GaN Systems GS66506T and GS66508P GaN-FETs are provided in Fig. 20(a) and (b), respectively. The drain-to-source voltage of the complementary secondary-side switch is also shown. It can be seen from the experimental results that the oscillations in the gate driver circuit are completely eliminated and the oscillations in $V_{\rm DS}$ waveforms are also minimized. It is noted that, along with the reduction in PCB parasitic inductance, use of Kelvin source on GaN Systems GS66508P and SMD ferrite beads helped in obtaining the final result.

Experimental results illustrating the problem of lower order harmonic distortion of the DMCI and its solution are discussed in the following part. Lower order harmonic distortion of the DMCI needs to be compensated using closed-loop control. Experimental results using four cases of closed-loop control techniques are presented and compared. These control techniques are summarized in Table II. Note that, case 4 is the proposed current control.

Fig. 21 shows the experimental result for case 1. The current control uses only fundamental and third harmonic compensation. Static inverse transformation has not been used. It can be seen that there is significant distortion in the grid current, which is highly undesirable. The fifth harmonic amplitude is found to be very high. The overall THD of the grid current is found to be around to 41%. The grid current also contains a dc offset.

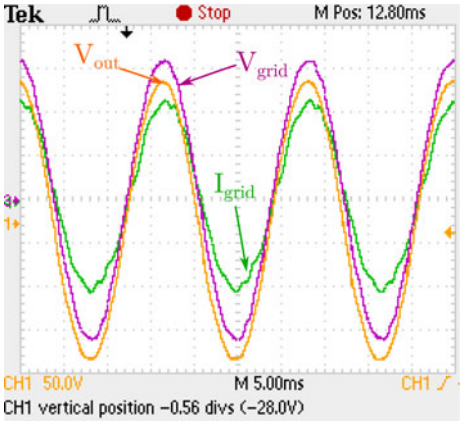


(a)

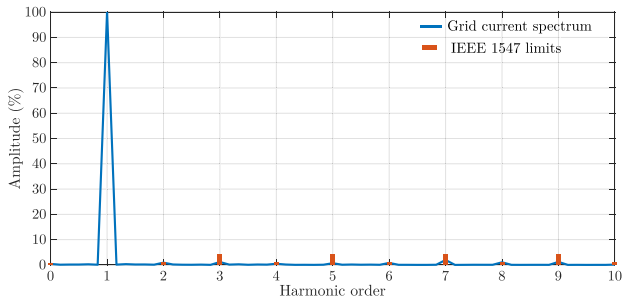


(b)

Fig. 23. (a) Experimental result when the current control has the MPR blocks alone (case 3), (b) corresponding spectrum of the grid current. Scale: Grid current (Ch. 4) 8 A/div and grid voltage (Ch. 1) 200 V/div. Horizontal scale: 20 ms/div.



(a)



(b)

Fig. 24. (a) Experimental result when proposed control with multi resonant blocks and inverse transformation is used (case 4), (b) corresponding spectrum of the grid current. Scale: Grid current (Ch. 4) 2 A/div, grid voltage (Ch. 3) 50 V/div, and $V_{\rm out}$ (Ch. 1) 50 V/div. Horizontal scale: 5 ms/div.

The effect of case 2, which uses the static inverse transformation is illustrated next. It can be seen from Fig. 22 that the distortion in grid current is considerably high. Fig. 22(b) shows the corresponding spectrum of the grid current. It can be seen from Fig. 22 that there is dc offset, even harmonics and odd harmonics. It is clear from this figure that a static inverse transformation alone does not offer any significant improvement in the grid current. The THD is measured to be 28%, which is high, similar to the case seen in Fig. 21. The experimental result for case 3, which uses only the MPR controller blocks up to ninth harmonic is shown in Fig. 23. The static inverse transformation is again not used. It can be observed that the lower order harmonics are reduced in this case. The overall THD is observed to be about 8%, which is still higher than the 5% limit set by the IEEE 1547-2003 standard [39].

The result with the proposed current control (case 4) is shown in Fig. 24(a). It can be observed that the grid current distortion is reduced significantly. This is evident from the spectrum of the grid current in Fig. 24(b). The grid current THD is measured to be 4%, which is within the desired THD limit of 5%. Summary of grid current THD for different control combinations is given in Fig. 25. It can be observed that the proposed control technique results in the least THD for the grid current.

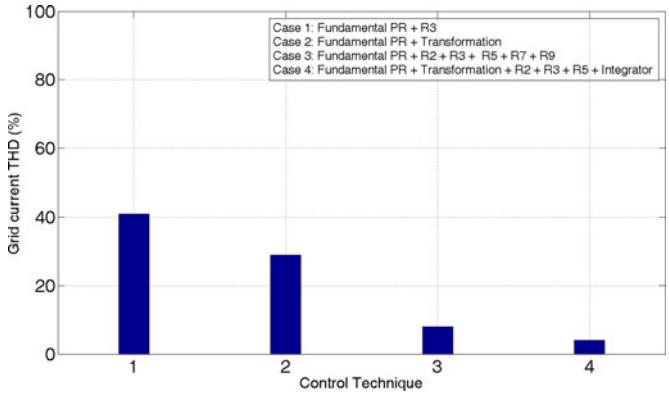


Fig. 25. Grid current THD for different control technique combinations (cases 1–4).

The proposed closed-loop control of the DMCI performs satisfactorily at different operating points as evident from Fig. 26. The grid current reference, in Fig. 26(a), has been reduced to $1A_{pk}$ to inject a power of 85 W to the grid. The grid current THD is found to be 4.4% and found to meet the harmonic requirements. The DMCI is operated in zero power factor (ZPF)

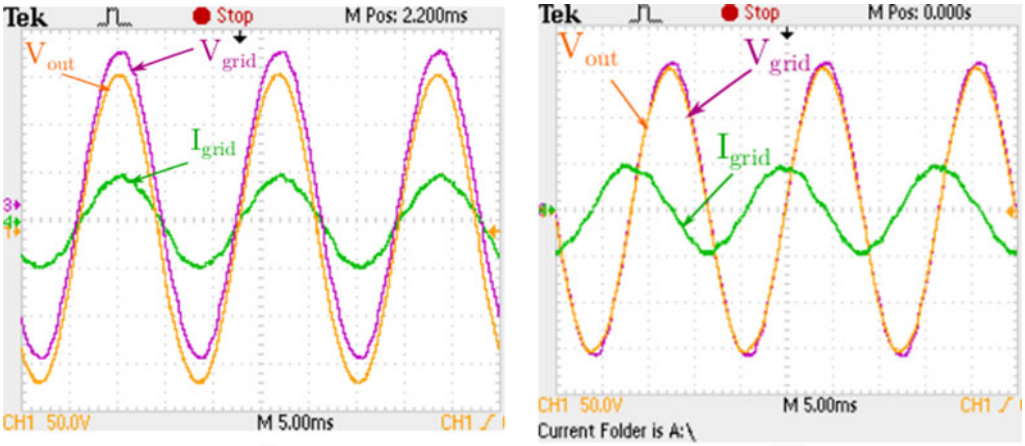


Fig. 26. Performance of the DMCI with the proposed control at (a) low power (85 W) and (b) ZPF operation. Scale: Grid current (Ch. 4) 1 A/div, grid voltage (Ch. 3) 50 V/div, and $V_{\rm out}$ (Ch. 1) 50 V/div. Horizontal scale: 5 ms/div.

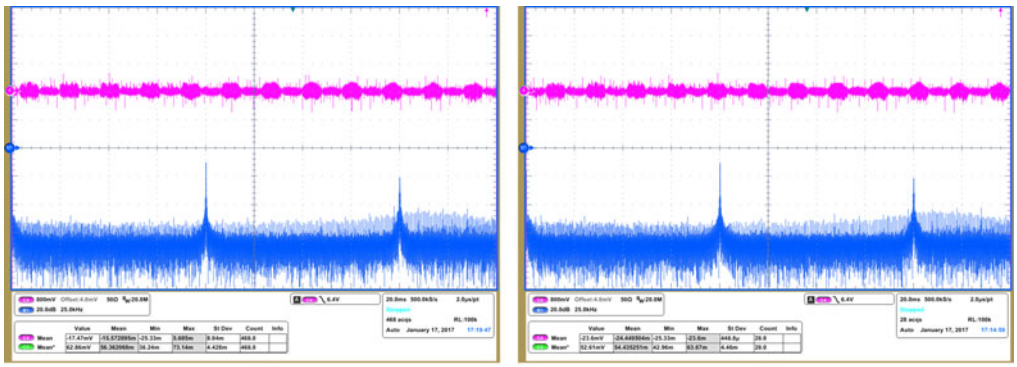


Fig. 27. (a) Experimental CM source current (top trace) and its spectrum (bottom trace) when (a) fundamental PR + inverse transformation control is used (case 2), and (b) proposed control is used (case 4). Scale: CM source current (Ch. 4) 0.8 A/div and its spectrum (Ch. M1) 20 dB/div.

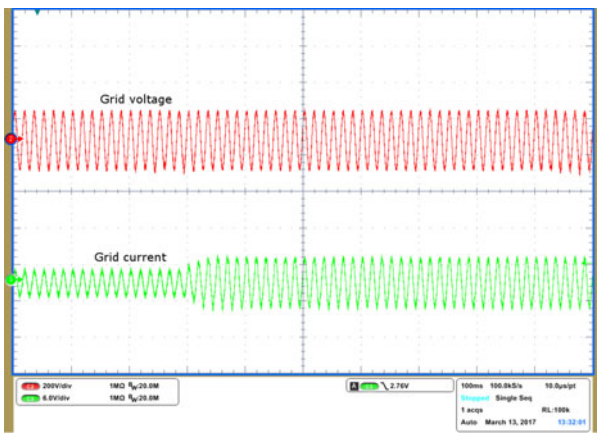


Fig. 28. Response of the proposed current control for a step change in grid current reference. Scale: Grid current (Ch. 3) 6 A/div and grid voltage (Ch. 2) 200 V/div. Horizontal scale: 100 ms/div.

mode injecting only the reactive power to the grid in Fig. 26(b). The grid current THD was observed to be 4.7%.

The effect of deadtime on the grid current THD was observed experimentally. For a deadtime of 180 ns, grid current THD is found to be 3.9%. It increases marginally to 4.1%, when a larger deadtime of 400 ns is used. It is noted that the distortion increases with higher deadtime. The proposed control maintains the grid current THD$<$5% even when the deadtime is made considerably higher. It was also found, as evident in Fig. 27 that the improvement in the response of the DMCI does not come at the price of any increase in the noise in the common-mode (CM) current. The CM current is measured by passing the dc source wires into a common Hall-effect-based current probe. This would cancel out the differential-mode currents and result only in CM current.

Finally, the transient response of the closed-loop DMCI using proposed current control is observed experimentally. A step change is given in the grid current reference. Fig. 28 shows the corresponding transient response. It can be observed that the current reaches the updated reference within three fundamental cycles. The transition is observed to be smooth.

VI. Conclusion

Practical issues of harmonic distortion and HF noise in a GaN-based DMCI are analyzed. A detailed analysis of occurrence of odd and even lower order harmonics in a practical DMCI is presented. It is shown that the conventional control

approach using a static inverse transformation is insufficient to handle all the distortion in the practical DMCI. As a result, a combination of multiresonant controller and inverse transformation is proposed to address the lower order harmonics issue. A small-signal state-space model for the grid-connected DMCI is derived. This model is used to determine the closed-loop controller parameters. The effectiveness of proposed control in addressing the lower order harmonics issue is validated experimentally.

Another important issue is the HF noise in the DMCI. The circuit PCB track inductance, the HF transformer leakage inductance, and nonideal behavior of the circuit passive elements are identified as the major factors contributing to the HF noise in the DMCI. An optimized PCB layout is designed to limit the PCB track inductance. The HF noise due to transformer leakage inductance is attenuated using a passive nondissipative snubber. Addition of suitable passive components based on their HF impedance response is used to further reduce the HF noise in the DMCI. The effect of these modifications in the DMCI in reducing the HF noise has been validated experimentally.

A combination of the hardware design and control design as described in this paper can address the grid current distortion and HF noise issues effectively in a grid-connected fast-switching GaN-based DMCI for PV microinverter application. This has been verified using experimental results.

Appendix A
Small-Signal State-Space Model for a DMCI Module

Consider that S_1 is ON and S_1' is OFF in Fig. 8(a). The state-space equations for module 1 of the DMCI for this case are as follows:

$$\frac{dI_{l1}}{dt} = \frac{V_{\text{in}}}{L_1} \tag{A.1}$$

$$\frac{dI_{l1'}}{dt} = \frac{k_1 V_{c1}}{L_1'} - \frac{V_{\text{out1}}}{L_1'} \tag{A.2}$$

$$\frac{dV_{c1}}{dt} = \frac{-nI_{l1'}}{C_1} - \frac{V_{c1}}{R_{s1}C_1} + \frac{V_{cs1}}{R_{s1}C_1} \tag{A.3}$$

$$\frac{dV_{\text{out1}}}{dt} = \frac{I_{l1'}}{C_{\text{out1}}} - \frac{I_g}{C_{\text{out1}}} \tag{A.4}$$

$$\frac{dV_{cs1}}{dt} = \frac{V_{c1}}{R_{s1}C_{s1}} - \frac{V_{cs1}}{R_{s1}C_{s1}}. \tag{A.5}$$

In (A.1)–(A.5), the state variables I_{l1}, $I_{l1'}$, V_{c1}, V_{out1}, and V_{cs1} are, respectively, the currents flowing through the inductors L_1 and L_1', the voltages across the capacitors C_1 and C_{out1}, and the voltage across the damping branch capacitor C_{s1}. The secondary-side capacitor voltages (C_1' and C_{s1}') are directly proportional to the primary-side capacitor voltages and as such no additional states are needed to capture their dynamics. In (A.2), the parameter k is given by

$$k_1 = n + \frac{C_1}{nC_1'}. \tag{A.6}$$

Similarly, the state-space equations of the DMCI when S_1 is turned OFF and S_2 is turned ON are as follows:

$$\frac{dI_{11}}{dt} = \frac{V_{\text{in}}}{L_1} - \frac{k_1' V_{c1}}{L_1} \tag{A.7}$$

$$\frac{dI_{l1'}}{dt} = -\frac{V_{\text{out1}}}{L_1'} \tag{A.8}$$

$$\frac{dV_{c1}}{dt} = \frac{I_{l1}}{C_1} - \frac{V_{c1}}{R_{s1}C_1} - \frac{V_{cs1}}{R_{s1}C_1} \tag{A.9}$$

$$\frac{dV_{\text{out1}}}{dt} = \frac{I_{l1'}}{C_{\text{out1}}} - \frac{I_g}{C_{\text{out1}}} \tag{A.10}$$

$$\frac{dV_{cs1}}{dt} = \frac{V_{c1}}{R_{s1}C_{s1}} - \frac{V_{cs1}}{R_{s1}C_{s1}}. \tag{A.11}$$

In (A.7), the parameter k' is given by

$$k_1' = 1 + \frac{C_1}{n^2 C_1'}. \tag{A.12}$$

The state variables are initially averaged over a switching cycle. Then, they are linearized around an equilibrium point using duty ratio $D_{1,0}$, input voltage V_{in}, and grid current I_g. Following the procedure in [40] and using (A.1)–(A.11), the resulting linearized state-space system with a small-signal duty ratio as the control variable is found to be of the following form:

$$\dot{\tilde{X}}_1 = A_1 \tilde{X}_1 + F_1 \tilde{D}_1 \tag{A.13}$$

$$\tilde{Y}_1 = C_1 \tilde{X}_1. \tag{A.14}$$

The matrices in (A.13) and (A.14) are defined as follows:

$$A_1 = \begin{bmatrix} 0 & 0 & -\frac{k_1'(1-D_{1,0})}{L_1} & 0 & 0 \\ 0 & 0 & \frac{k_1 D_{1,0}}{L_1'} & -\frac{1}{L_1'} & 0 \\ \frac{1-D_{1,0}}{C_1} & -\frac{nD_{1,0}}{C_1} & -\frac{1}{R_{s1}C_1} & 0 & \frac{1}{R_{s1}C_1} \\ 0 & \frac{1}{C_{\text{out1}}} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{R_{s1}C_{s1}} & 0 & -\frac{1}{R_{s1}C_{s1}} \end{bmatrix} \tag{A.15}$$

$$F_1 = \begin{bmatrix} \frac{V_{\text{in}}}{(1-D_{1,0})L_1} & \frac{nV_{\text{in}}}{(1-D_{1,0})L_1'} & -\frac{nI_g}{(1-D_{1,0})C_1} & 0 & 0 \end{bmatrix}^T \tag{A.16}$$

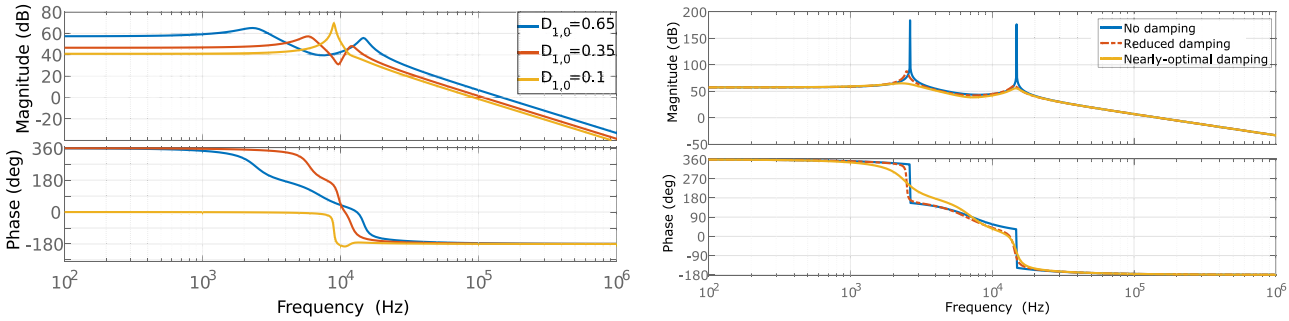
$$C_1 = \begin{bmatrix} 0 & 0 & 0 & 1 & 0 \end{bmatrix}. \tag{A.17}$$

The output $\tilde{Y}_1$ in (A.14), is the small-signal voltage $\tilde{V}_{\text{out1}}$ for the first DMCI module.

The final state equations are given by (A.15)–(A.17). These are used to obtain the Bode plot of the output-to-duty-ratio transfer function of the DMCI, which is used for the closed-loop control design of the DMCI.

Appendix B
Transfer Function Models Used in the Closed-Loop Control of the DMCI

Closed-loop control block diagram of the DMCI is shown in Fig. 7. The transfer functions for the MPR blocks and the



(a) (b)

Fig. B.1. Bode plot of the open-loop DMCI module for output voltage to the duty-ratio transfer function ($G_{vd1}(s)$) for different quiescent values of $D_{1,0}$ and (b) Bode plot of the output voltage to duty ratio transfer function for different levels of damping.

integrator are as follows:

$$G_{\text{PR}} = k_p + \frac{k_r \omega_c s}{s^2 + \omega_c s + (\omega_0)^2}$$

$$G_{R,h} = \frac{k_{rh}\omega_c s}{s^2 + \omega_c s + (h\omega_0)^2};\;\; G_I = \frac{k_I}{s}. \tag{B.1}$$

In the aforementioned equation, the transfer functions of the harmonic compensators are represented using $G_{R,h}$. For proposed control, $h = 2, 3, 5$.

The static-inverse-transformation block follows the MPR and integral controllers. This transformation has to be separated into small- and large-signal parts. Equation (4) can be rewritten as

$$D_{1,0} + \tilde{D}_1 = \frac{V_{\text{ref1},0} + \tilde{V}_{\text{ref1}}}{V_{\text{ref1},0} + \tilde{V}_{\text{ref1}} + nV_{\text{in}}/m}$$

$$= \frac{V_{\text{ref1},0}}{V_{\text{ref1},0} + nV_{\text{in}}/m}\left(\frac{1 + \tilde{V}_{\text{ref1}}/V_{\text{ref1},0}}{1 + \tilde{V}_{\text{ref1}}/(V_{\text{ref1},0} + nV_{\text{in}}/m)}\right) \tag{B.2}$$

In (B.2), $D_{1,0}$ and $V_{\text{ref1},0}$ are the quiescent operating points around which small-signal linearization is performed. Note that V_{ref1} of (4) is written as

$$V_{\text{ref1}} = V_{\text{ref1},0} + \tilde{V}_{\text{ref1}}$$

in (B.2). This equation can be further simplified as

$$D_{1,0} + \tilde{D}_1 \approx D_{1,0} + D_{1,0}\frac{\tilde{V}_{\text{ref1}}}{V_{\text{ref1},0}}$$

$$\Rightarrow \tilde{D}_1 = \frac{D_{1,0}}{V_{\text{ref1},0}}\tilde{V}_{\text{ref1}}. \tag{B.3}$$

The state-space model for the DMCI can be converted into an equivalent transfer function using the following standard transformation:

$$G_{vd1}(s) = \frac{\tilde{V}_{\text{out1}}(s)}{\tilde{D}_1(s)} = C_1(sI - A_1)^{-1}F_1. \tag{B.4}$$

where $\tilde{V}_{\text{out1}}$ and $\tilde{D}_1$ are the small-signal perturbations on the output voltage V_{out1} and duty ratio D_1 around the quiescent point of module 1. The complete expression for the transfer function $G_{vd1}(s)$ can be derived as follows:

$$G_{vd1}(s) = \frac{y_1 + y_2 + y_3}{(D_{1,0} - 1)[x_1 + x_2 + x_3 + x_4 + x_5 + x_6]}. \tag{B.5}$$

The terms in the aforementioned equation are as follows:

$$\begin{aligned}
y_1 &= (k_1 - k_1' n)(C_{s1}R_{s1}s + 1)V_{\text{in}}D_{1,0}^2 \\
y_2 &= (C_{s1}R_{s1}s + 1)(I_g k L_1 n s - k_1 V_{\text{in}} + 2k_1' n V_{\text{in}})D_{1,0} \\
y_3 &= n\left(L_1(C_{s1}R_{s1}sC_1 + C_1 + C_{s1})s^2\right. \\
&\quad \left. + C_{s1}k_1'R_{s1}s + k_1'\right)V_{in} \\
x_1 &= k_1'(C_{s1}R_{s1}s + 1)(C_{\text{out1}}L_1's^2 + 1)(D_{1,0} - 1)^2 \\
x_2 &= L_1 s^2 C_{\text{out1}} k_1 n D_{1,0}^2 \\
x_3 &= L_1 s^2 C_{\text{out1}} C_{s1} k_1 n R_{s1} s D_{1,0}^2 \\
x_4 &= L_1 s^2 C_{\text{out1}} C_{s1} L_1' s^2 \\
x_5 &= L_1 C_{s1} s^2 \\
x_6 &= L_1 s^2 C_1 (C_{s1}R_{s1}s + 1)(C_{\text{out1}}L_1's^2 + 1).
\end{aligned} \tag{B.6}$$

Fig. B.1(a) shows the Bode plot of $G_{vd1}(s)$ of a DMCI module for three cases of $D_{1,0}$. It can be observed that the frequency response is different for the three cases of $D_{1,0}$, as expected due to the shifting of the system eigenvalues. Fig. B.1(b) shows the inherent low damping in the DMCI that was described in Section III-B1.

As can be seen from the output voltage to duty ratio Bode plot presented in Fig. 8(b), the DMCI has negligible damping without the $R_s - C_s$ damper branch. This causes the stable closed-loop control of the DMCI difficult to achieve. Hence, to reach a nearly optimal level of damping the values of the damper branch are computed iteratively. The Bode plot in Fig. B.1(a) for different values of the duty ratio is for an optimal value of $R_s = 8\,\Omega$ and $C_s = 22\,\mu$F.

The remaining transfer function is the grid-side impedance. It is given as

$$Z_g(s) = \frac{1}{R_g + sL_g}. \tag{B.7}$$

The final transfer function expressions in (B.1), (B.3), (B.5), (B.6), and (B.7) are used in the design of the controller gains

described in Section III-B. The loop-gain used for the control parameter design is given by

$$L(s) = [G_{\mathrm{PR}} + G_{R2} + G_{R3} + G_{R5}]G_{vd1}Z_g\frac{D_{1,0}}{V_{\mathrm{ref}1,0}}. \quad \text{(B.8)}$$

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