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Analysis of Input Current Ripple and Optimum Filter Capacitor for Fuel-Cell-Based Single-Phase Inverter

Most single-phase inverters, being sourced by fuel cell stacks (FCSs), subject the stacks to reflected low-frequency (120 Hz) current ripples that ride on average dc currents. The ripple current impacts the sizing and efficiency of the FCS. As such and typically, a passive or active filter is required at the input of the inverter (or output of the FCS) to mitigate the ripple current. Toward that end, this paper outlines a guideline to choose the optimum size of a passive input-filter capacitor for a fuel-cell-based power system from the standpoints of the overall system energy density and cost. Detailed case-specific simulation results, based on an analytical approach, are provided to illustrate key issues for both unity power factor as well as harmonic loads. [DOI: 10.1115/1.4032040]

1 Introduction

An issue of importance for fuel cell (FC)-based inverter is the selection of the rating of the FCS. High cost of a cell and enhanced probability of failure of an FCS with increasing number of cells renders the inverter to be typically low-voltage and high-current systems [1]. For a single-phase inverter, which produces a significant 120 Hz current ripple at the input of the inverter [2], a large average current rating implies a large current ripple, which is detrimental to the life and performance of the FCS [3]. Further, to handle the large ripple current (producing zero average power), the FCS has to be oversized which increases the cost of the overall power system. As shown in Fig. 1, to mitigate the current ripple from the FCS current, a typical and low-cost solution is to place a filter capacitor at the input (or output) of the inverter (or of the FCS). Similar power decoupling method is also used in the photovoltaic (PV) systems [4]. A detailed review of active power decoupling methods has been presented in Ref. [5]. However, this paper focuses on the passive capacitor stack based approach only and outlines a guideline to choose the optimum size of a passive input-filter capacitor from the standpoints of the overall system energy density and cost.

Analysis shows that there exists a negative-current zone for a FCS connected to a single-phase inverter producing line-frequency sinusoidal voltage for any power factor other than unity. A suitable input-filter capacitor can be chosen to prevent negative FCS current. Dependence of the magnitude of the FCS current ripple on load power factor, load harmonics, and size of input-filter capacitor is illustrated. It is also shown that the magnitude of the FCS ripple current varies with stack parameters such as voltage and current ratings, for a given value of the input-filter capacitance. Finally, it is demonstrated how the FCS efficiency, which varies with the magnitude of the current ripple, varies with stack and load parameters (such as power factor and harmonics). It is shown that an optimum value of the input-filter capacitor (for a given voltage and current rating of the stack or for a given load profile) from stack efficiency and cost points of view can be derived.

2 Analysis of the Input Ripple Current

FCS current ripple is caused by the reflection of the current on the output of the modulated inverter to the input side. Before moving forward, we assume the following in our analysis:

- Impact of switching-ripple dynamics is assumed to be negligible due to very low magnitude and large-scale separation (i.e., 60 Hz line and 200 kHz switching frequencies) [6];
- The switching converter does not store any average energy; i.e., all the parasitic capacitances and inductances of the switching converter can be treated as negligible [6].
- Voltage drop in the output filter is negligible compared to the output voltage value.

We start with the average power-balance equation *in the absence of the input-filter capacitor*

$$V_{\mathrm{FC}} I_{\mathrm{FC}} = \frac{V_o I_o}{\eta} \tag{1}$$

where η represents the inverter efficiency, and V_o and I_o are the rms output voltage and current, respectively. Modeling the FCS as a current-controlled dc voltage source with area-specific-resistance (R_{ASR}) [7], we obtain

$$(V_{\mathrm{oc}} - I_{\mathrm{FC}} R_{\mathrm{ASR}}) I_{\mathrm{FC}} = \frac{V_o I_o}{\eta} \tag{2}$$

where V_{OC} is the stack open-circuit voltage and I_{FC} is the stack current. Assuming a load with a power factor of $\cos(\varphi)$ along with sinusoidal output voltage and current (having peak values of V_m and I_m, respectively, and a periodic frequency of ω), we obtain

$$(V_{\mathrm{oc}} - I_{\mathrm{FC}} R_{\mathrm{ASR}}) I_{\mathrm{FC}} = \frac{V_m \sin(\omega t) I_m \sin(\omega t + \varphi)}{\eta}$$

$$\Rightarrow (V_{\mathrm{oc}} - I_{\mathrm{FC}} R_{\mathrm{ASR}}) I_{\mathrm{FC}} = \frac{V_m I_m}{2\eta} \left[\cos(\varphi) - \cos(2\omega t + \varphi)\right] \tag{3}$$

Equation (3) leads to a quadratic equation in I_{FC}

$$I_{\mathrm{FC}}^2 R_{\mathrm{ASR}} - I_{\mathrm{FC}} V_{\mathrm{OC}} + \frac{V_m I_m}{2\eta} \left[\cos(\varphi) - \cos(2\omega t + \varphi)\right] = 0 \tag{4}$$

which yields

$$I_{\mathrm{FC}} = \frac{V_{\mathrm{OC}}}{2R_{\mathrm{ASR}}} \pm \frac{\sqrt{V_{\mathrm{OC}}^2 - 4R_{\mathrm{ASR}} \frac{V_m I_m}{2\eta} \left[\cos(\varphi) - \cos(2\omega t + \varphi)\right]}}{2R_{\mathrm{ASR}}} \tag{5}$$

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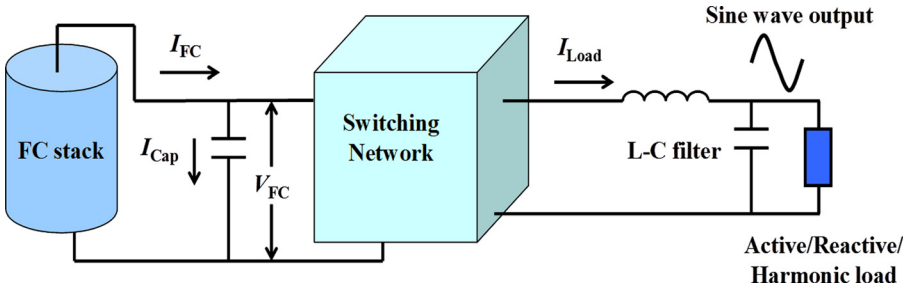

Fig. 1 Current distribution in an FCS-based single-phase single-stage inverter. A typical illustration of such a topology is shown in Ref. [2], which achieves voltage amplification using an embedded step-up high-frequency transformer. It is noted that such a single-stage inverter can be nonisolated as well even though it is normally less practical due to the cost of the stack to support a high voltage. Symbols I_{Out}, I_{FCS}, and I_{Cap} represent, respectively, the inverter-output, FCS-output, and filter-capacitor currents. I_{Out}, devoid of high-frequency components (which is absorbed by the output capacitor), represents the load current. The sinusoidal modulation of the inverter results in an inverter input current that has a dc- and a strong ripple-current component.

We show in Fig. 2 that, for any power factor other than unity, I_{FC} will be negative and the maximum negative value increases with the load power factor.

For preventing this negative current, a filter capacitor is typically placed at the input to the inverter, as shown in Fig. 1. Therefore, next, the power-balance equation (1) is rewritten *taking into account the contributions of the FCS and the input-filter capacitor currents*

$$V_{FC}(I_{FC} - I_{cap}) = \frac{V_m \sin(\omega t) I_m \sin(\omega t + \phi)}{\eta} \tag{6}$$

Now, using the current–voltage relation of the FCS, I_{FC} is given by

$$I_{FC} = \frac{V_{OC} - V_{FC}}{R_{ASR}} \tag{7}$$

Capacitor current is given by

$$I_{cap} = C\frac{dV_{FC}}{dt} \tag{8}$$

Using Eqs. (6)–(8), we obtain

$$V_{FC}\left(\frac{V_{OC} - V_{FC}}{R_{ASR}} - C\frac{dV_{FC}}{dt}\right) = \frac{V_m \sin(\omega t) I_m \sin(\omega t + \varphi)}{\eta}$$
$$\Rightarrow V_{FC}\left(\frac{V_{OC} - V_{FC}}{R_{ASR}} - C\frac{dV_{FC}}{dt}\right) = \frac{V_m I_m}{2\eta}\left[\cos(\varphi) - \cos(2\omega t + \varphi)\right] \tag{9}$$

Therefore, the nonlinear differential equation governing the input voltage is given by

$$-V_{FC}\frac{dV_{FC}}{dt} - \frac{V_{FC}^2}{CR_{ASR}} + \frac{V_{FC}V_{OC}}{CR_{ASR}} - \frac{V_m I_m}{2\eta}\left[\cos(\varphi) - \cos(2\omega t + \varphi)\right] = 0 \tag{10}$$

Using the solution of Eqs. (10) (i.e., V_{FC}) and (6), one can calculate I_{FC}, its sign, and the percentage ripple. It is noted that, for a load drawing harmonic currents, Eq. (10) can be generalized to

$$-V_{FC}\frac{dV_{FC}}{dt} - \frac{V_{FC}^2}{CR_{ASR}} + \frac{V_{FC}V_{OC}}{CR_{ASR}} - \frac{V_m \sin(\omega t)}{C\eta}$$
$$\left[I_{m1}\sin(\omega t + \varphi_1) + I_{m2}\sin(2\omega t + \varphi_2) + I_{m3}\sin(3\omega t + \varphi_3) + \ldots\right] = 0 \tag{11}$$

where I_{m1}, I_{m2}, I_{m3} are the peak values of the harmonic components and φ_1, φ_2, φ_3 are the corresponding phase angles. Rewriting Eq. (10) as

$$V_{FC}\frac{dV_{FC}}{dt} = -\frac{V_{FC}^2}{CR_{ASR}} + \left(\frac{V_{OC}}{CR_{ASR}}\right)V_{FC} - \frac{V_m I_m}{2\eta}\left[\cos(\varphi) - \cos(2\omega t + \varphi)\right] \tag{12}$$

one can recognize that Eq. (12) represents Abel's differential equation of the second kind. Using two new variables w and z given by

$$V_{FC} = e^{-t/CR_{ASR}}.w(t) \tag{13}$$

$$z = \left(\frac{V_{OC}}{CR_{ASR}}\right).\int e^{t/CR_{ASR}}dt \tag{14}$$

Equation (12) is transformed to the following differential equation:

$$w.\frac{dw}{dz} - w = -z\left(\frac{CR_{ASR}}{V_{OC}^2}\right)\left(\frac{V_m I_m}{2C\eta}\left[\cos(\varphi) - \cos\left(2\omega\left(CR_{ASR}\ln\left\{\frac{z}{V_{OC}}\right\}\right) + \varphi\right)\right]\right) \tag{15}$$

Generalized solution for the equation of type (15) is found in Ref. [8] as the implicit solution of a set of simultaneous integral and algebraic equations. Due to the presence of transcendental functions in the right-hand side of Eq. (15), closed-form analytical solution cannot be derived in the present case. Therefore, a fourth-order Runge–Kutta numerical algorithm is used to solve Eq. (10) or (11) for calculating FCS current ripple. Then, the FCS current is given by

$$I_{FC} = \frac{V_{OC} - V_{FC}}{R_{ASR}} \tag{16}$$

Therefore, the peak-to-peak ripple (R_{PP}) of the FCS current is given by

$$R_{PP} = \frac{\max(I_{FC}) - \min(I_{FC})}{\text{avg}(I_{FC})} \tag{17}$$

where $\max(I_{FC})$, $\min(I_{FC})$, and $\text{avg}(I_{FC})$ represent maximum, minimum, and average values of I_{FC}.

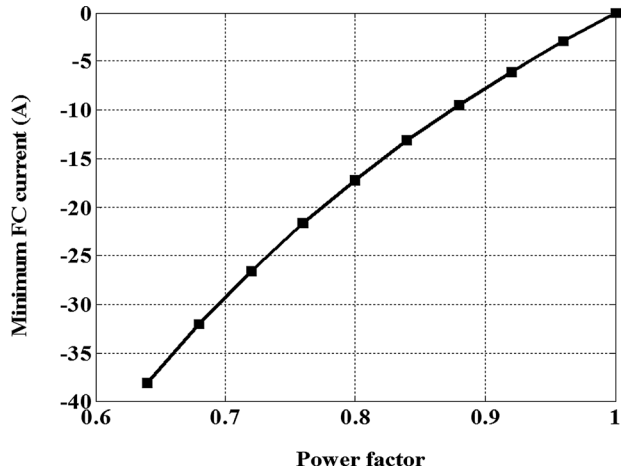

Fig. 2 Peak negative FCS current with non-unity power factor load without input-filter capacitor

3 Simulation Results and Discussion

To carry out the simulation-based analysis, an experimentally validated planar solid oxide FC model, as reported in Ref. [9], is used to set V_{OC} (=23.75 V) and R_{ASR} (=20.17 mΩ). Parameter V_m represents the peak value of the single-phase utility voltage (i.e., $120 \cdot \sqrt{2} = 169.7$ V). Parameters I_m or I_{mn} (where n represents the harmonic number for the harmonic load) represent the peak value(s) of the fundamental (nth-harmonic) component of the output current. For initial analysis, a 3 kW unity power factor load is assumed. An inverter efficiency of 90% is assumed (i.e., $\eta = 0.9$). Using V_{OC}, R_{ASR}, V_m, I_m, η, cos(φ), and input-filter capacitance C, V_{FC} can be solved using Eq. (12) using the fourth-order *Runge–Kutta* numerical algorithm as mentioned in Sec. 2. Subsequently, I_{FC} and R_{PP} are determined using Eqs. (16) and (17).

First, we show how the FCS current behaves with and without the input-filter capacitor. Figure 3 shows that the current has a sinusoidal ripple riding on a dc current. It is seen that, without the filter capacitor, the current becomes negative when the load power factor is less than unity. It also suggests that, for a given power factor, a minimum value of input capacitance is required to maintain positive FC current. Therefore, in Fig. 4, variation of the FCS current ripple with varying load power factor and input capacitance is demonstrated.

Next, we demonstrate in Fig. 5 that, for a small value of input-filter capacitance, increasing the FCS nominal voltage (i.e., by

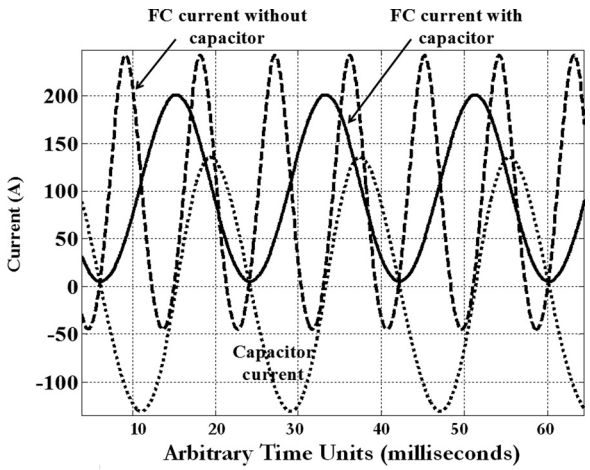

Fig. 3 FCS current at 0.6 load power factor, with and without a 50 mF input-filter capacitor

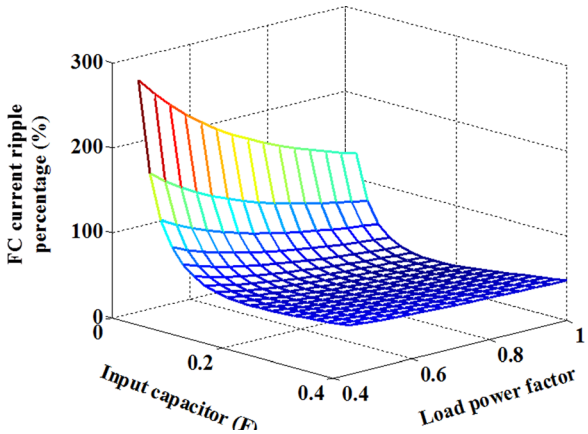

Fig. 4 FCS current ripple as a function of input-filter capacitor size and load power factor

increasing the number of cells in series) may reduce the FCS current ripple for a given load power factor and output power. But the percentage reduction is quite small as compared to what one can achieve using a larger capacitance. Therefore, a rational choice must be made between selecting a large input-filter capacitor and large number of cells in a stack based on the comparative cost of these two options.

Next, the effects of the load-current harmonics on the FCS input-current ripple are investigated. FCS voltage and current are calculated using Eqs. (11) and (16) and assuming the existence of third, fifth, and seventh harmonics, which is a typical scenario. The input-filter capacitance is set at 100 mF and the magnitudes

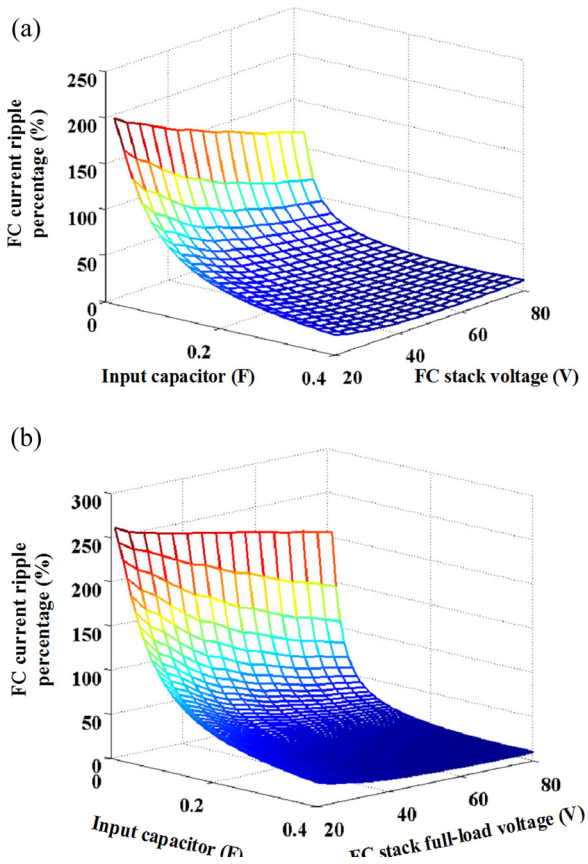

Fig. 5 Input-filter capacitor size versus FCS current ripple for different stack nominal voltages at load power factors of (*a*) 1.0 and (*b*) 0.8, respectively

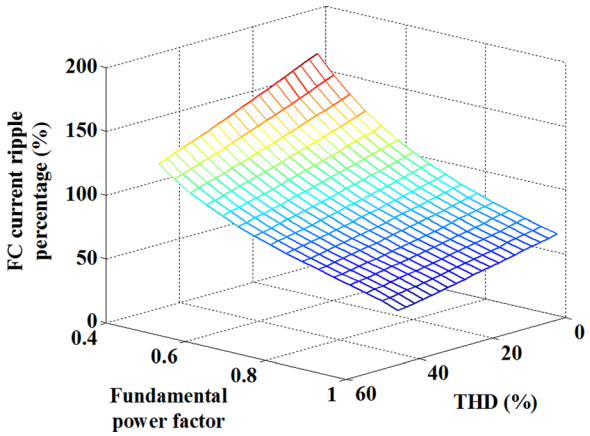

Fig. 6 THD versus peak-to-peak FCS current ripple for varying fundamental power factor

of the harmonic currents are varied. Total harmonic distortion (THD) of the load current is calculated using

$$\text{THD} = \frac{\sqrt{I_{m3}^2 + I_{m5}^2 + I_{m7}^2}}{I_{m1}} \tag{18}$$

while the phase angles of the fundamental and harmonic components are given by

$$\varphi_k = \tan^{-1}\left(\frac{n\omega L}{R}\right) \quad \text{where } n = 1, 3, 5, 7, \ldots \tag{19}$$

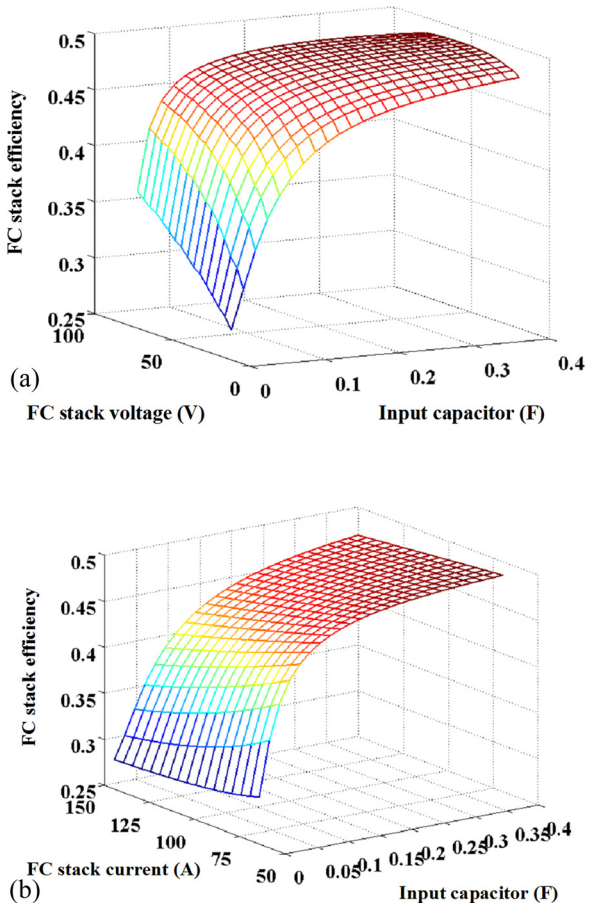

Fig. 7 FCS efficiency as a function of input-filter capacitor size and (*a*) stack voltage and (*b*) stack current ratings

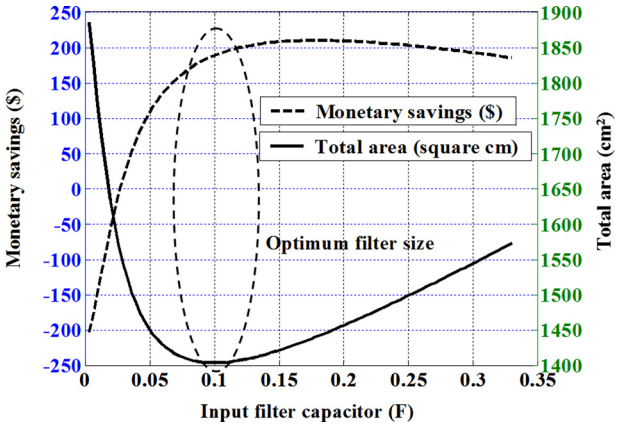

Fig. 8 Input-filter capacitor size versus monetary savings (due to increased FCS efficiency) and total footprint area of the inverter. The zone of optimality is illustrated by dotted ellipse. A curve-fitted equation was used to plot this, however, the nature and coefficients of the equation will vary greatly with FC stack and capacitor technology choice, and therefore, it should not be perceived as a generic equation.

Figure 6 shows the dependence of FCS peak-to-peak current ripple on the THD of the load current with varying fundamental power factor (i.e., $\cos(\phi_1)$). The phase angle of the fundamental component is varied and for each value, the FCS current ripple is calculated with varying THD. Figure 7 indicates that FCS peak-to-peak current ripple decreases with increasing THD and increases with decreasing fundamental power factor.

Next, we investigate the effect of large current ripple on the FCS efficiency. Figure 7 plots the stack efficiency as a function of stack voltage and current ratings and filter capacitor size. This gives the FC power-system designer and the FC manufacturer choice of selecting the optimum ripple-mitigating capacitor for achieving the balance between stack efficiency, voltage and current ratings of the stack, and combined cost of input capacitor and the stack.

However, the enhanced stack efficiency comes at the price of increasing the footprint area and cost of the power electronics. Based on the Department of Energy specification of solid oxide FC stack cost [10], the monetary gain that can be achieved by increasing capacitor size and the total footprint area (sum of FC stack and converter areas) to determine the optimum range of the input-filter size. For calculating the input-filter capacitor cost, a particular class of capacitor (electrolytic) is chosen and a base unit price is obtained from the retailer. Total required capacitance was divided by the base unit capacitance to obtain the number of capacitors and that number is multiplied by the base unit price to obtain the total capacitor cost. In all calculations, bulk production pricing is assumed. Choice of voltage rating of the capacitor is important because it influences the base price significantly for electrolytic capacitors. For instance, an 80 V electrolytic capacitor of 5.6 mF is priced at $2.60 whereas a 100 V electrolytic capacitor of 5.6 mF is priced at $4.93. A base unit of 3.3 mF (large quantity price $1.57) is chosen for this calculation. The actual part number is KMG50VB332M18X35LL from United-Chemi Con. Figure 8 illustrates the monetary savings and total footprint area of power electronics as a function of the input-filter capacitor size.

4 Summary and Conclusions

We describe an analysis technique for the input-current-ripple calculation for a single-phase inverter fed by a FCS. The analysis shows that, for any power factor other than unity, the reflected current ripple on the FCS output will cause the absolute value of the stack current to go negative. Because FCS typically does not support negative current, this must be handled by a passive or active filter placed at the output of the FCS (i.e., at the input of the

inverter). For a passive input-filter capacitor, the analysis can further determine the percentage ripple as a function of capacitor value. Moreover, the voltage and current ratings of the FCS also feature in this analytical framework and hence the effect of input-filter capacitor sizing on the ripple-current reduction can be examined as a function of FCS size. Because ripple-current magnitude has been shown to affect the FCS efficiency, it is further possible to examine how the stack efficiency varies with the input-filter capacitor size. From a practical consideration, however, the cost and footprint space of a capacitor increase as the capacitance increases. On the other hand, increased stack efficiency effectively results in cost savings on the part of the FC-system developer. Therefore, an optimization study is also performed to determine the net monetary savings as the input-filter size is increased and it is found that, a maximum savings point can be realized for a particular type of the capacitor. Although this study does not guarantee existence of such an optimized cost for all situations, it establishes the need for such a practice while choosing an input capacitor for a single-phase inverter system.

References

[1] Mazumder, S. K., Sarkar, T., and Acharya, K., 2009, "A DirectFET^{tm} Based High-Frequency Fuel-Cell Inverter," 24th IEEE Applied Power Electronics Conference (APEC 2009), Washington, DC, Feb. 15–19, pp. 1805–1812.

[2] Mazumder, S. K., Burra, R. K., and Acharya, K., 2007, "A Ripple-Mitigating and Energy-Efficient Fuel Cell Power-Conditioning System," IEEE Trans. Power Electron., **22**(4), pp. 1437–1452.

[3] Mazumder, S. K., Acharya, K., Haynes, C., Williams, R., von Spakovsky, M. R., Nelson, D., Rancruel, D., Hartvigsen, J., and Gemmen, R., 2004, "Solid-Oxide-Fuel-Cell Performance and Durability: Resolution of the Effects of Power-Conditioning Systems and Application Loads," IEEE Trans. Power Electron., **19**(5), pp. 1263–1278.

[4] Haibing, H., Harb, S., Kutkut, N., Batarseh, I., and Shen, Z. J., 2013, "A Review of Power Decoupling Techniques for Microinverters With Three Different Decoupling Capacitor Locations in PV Systems," IEEE Trans. Power Electron., **28**(6), pp. 2711–2726.

[5] Sun, Y., Liu, Y., Su, M., Xiong, W., and Yang, J., 2015, "Review of Active Power Decoupling Topologies in Single-Phase Systems," IEEE Trans. Power Electron. (in press).

[6] Kassakian, J. G., Schlecht, M. F., and Verghese, G. C., 1991, *Principles of Power Electronics*, Addison Wesley, Washington, DC.

[7] Singhall, S. C., and Kendall, K., 2003, *High-Temperature Solid Oxide Fuel Cells: Fundamentals, Design and Applications*, Elsevier, Atlanta, GA.

[8] Panayotounakos, D. E., Sotiropoulos, N. B., Sotiropoulou, A. B., and Panayotounakou, N. D., 2005, "Exact Analytic Solutions of Nonlinear Boundary Value Problems in Fluid Mechanics (Blasius Equations)," J. Math. Phys., **46**(3), p. 033101.

[9] Pradhan, S., Mazumder, S. K., Hartvigsen, J., and Hollist, M., 2007, "Effects of Electrical Feedbacks on Planar Solid-Oxide Fuel Cell," ASME J. Fuel Cell Sci. Technol., **4**(2), pp. 154–166.

[10] Battelle Memorial Institute, 2014, "Manufacturing Cost Analysis of 1 kW and 5 kW Solid Oxide Fuel Cell (SOFC) for Auxiliary Power Applications," U.S. Department of Energy, Golden, CO, Report No. DE-EE0005250.