Novel Zero-Current-Switching Current-Fed Half-Bridge Isolated DC/DC Converter for Fuel-Cell-Based Applications

Udupi R. Prasanna, *Member, IEEE*, Akshay K. Rathore, *Senior Member, IEEE*, and Sudip K. Mazumder, *Senior Member, IEEE*

***Abstract*—A novel zero-current-switching (ZCS) current-fed half-bridge isolated dc/dc converter has been proposed in this paper. The proposed converter has potential applications such as front-end dc/dc power conversion for fuel cell and photovoltaic inverters, bidirectional converters for fuel cell vehicles, energy storage, etc. This proposed converter provides a simple solution to the switch turn-off voltage spike problem without any additional components or snubber. It leads to reduced size, lower cost, compactness, and higher conversion efficiency. In addition, the proposed converter has reduced peak current through the components (semiconductor devices and transformer) that reduces their volt-ampere rating and size compared to active-clamped zero-voltage-switching (ZVS) current-fed converters. Voltage across the primary switches is naturally clamped without an additional active clamp or snubber circuit. In addition, voltage across the switch is independent of the duty cycle. ZCS of the primary switches, natural commutation of secondary diodes, and zero-current turn-on of secondary switches are achieved. Therefore, switching transition losses are significantly reduced. Steady-state analysis, operation with the proposed novel ZCS concept, and design of the converter are reported. A 200-W laboratory converter prototype has been built. Experimental results as well as simulation results are presented to validate the analysis and design. A comparison with existing active-clamped ZVS current-fed half-bridge converters has been discussed. The effect of device parasitic is investigated and explained by simulation and experimental results.**

***Index Terms*—Bidirectional converter, current fed, dc/dc converter, fuel cells, renewable energy sources, soft switching.**

I. Introduction

GREEN ENERGY and clean transportation has potentially attracted the attention of researchers, industries, and common men in recent years. With the concept of smart grid, smart metering, smart buildings, alternative energy sources, transportation electrification, hybrid microgrid, etc., efficient, economical, and compact power conversion is getting increasing importance, and power electronics industries are revoking. Alternative energy sources (photovoltaic (PV), wind, etc.) cannot be used as such since their output is unregulated and discontinuous in nature. Therefore, a power condition link is needed to convert their output into regulated and usable form for given application. Maximum power from these sources is extracted and supplied to low-voltage dc grid for local loads as well as interfaced to standard ac grid (utility) with a point of common coupling with local ac loads. A typical smart grid has hybrid microgrid (low-voltage dc and standard ac grid), and zero-emission vehicles are part of it. Fuel cells have been accepted as an important part because their output is continuous and secure as long as the fuel supply is maintained unlike PV and wind. In addition, fuel cell vehicles are assumed to be taking over once commercialized as they are true zero-emission vehicles. Energy storage in gas (H_2 and O_2) form relieves from issues like disposal, lifetime, leakage, deep discharging, overcharging, and capacity variations with season in case of battery storage. Therefore, fuel cell systems will dominate in future smart grid.

To improve the fuel utilization and efficiency or, in other words, for the energy-efficient operation of fuel cells, the current ripple of the fuel cell stack must be minimized [1]. This is applicable to any fuel cell applications and true for any kind of source.

Front-end dc/dc conversion is important in fuel cell/PV inverters because its efficiency dominates the overall system efficiency. Since it is directly interfaced to the source, its functionality decides the performance of the source [1], source/fuel utilization for example. Hence, selection of efficient and high-performance converters is important.

Several converter topologies have been reported [2]–[24]. A comparison of soft-switching converters has been studied in [18] and [19] and has justified current-fed half-bridge topology as a suitable topology for fuel cell applications [2]–[4], [16]–[20]. The same is true for applications of low voltage high current, higher voltage conversion ratio, and wide source voltage and power transfer capacity variations. It draws a low ripple dc current from fuel cell stack and has been widely reported recently [2]–[4], [15]–[17], [22]–[24]. An active-clamp helps in achieving soft switching of devices and absorbs the

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U. R. Prasanna is with the Department of Electrical Engineering, The University of Texas at Dallas, Richardson, TX 75080 USA (e-mail: prasanna.ur@utdallas.edu).

A. K. Rathore is with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117576 (e-mail: eleakr@nus.edu.sg).

S. K. Mazumder is with the Department of Electrical and Computer Engineering, University of Illinois at Chicago, Chicago, IL 60607 USA (e-mail: mazumder@ece.uic.edu).

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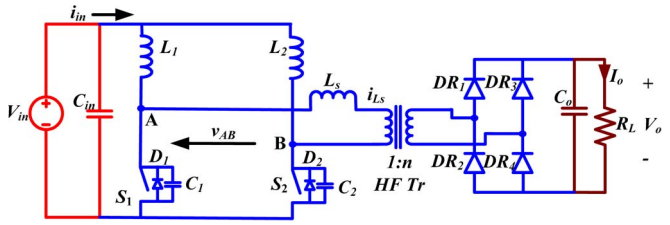

Fig. 1. Conventional hard-switched current-fed half-bridge isolated dc/dc converter [8].

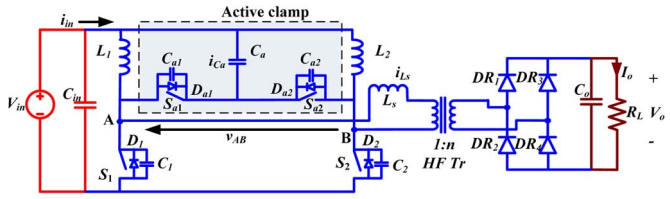

Fig. 2. Active-clamped ZVS current-fed half-bridge isolated dc/dc converter [2]–[4].

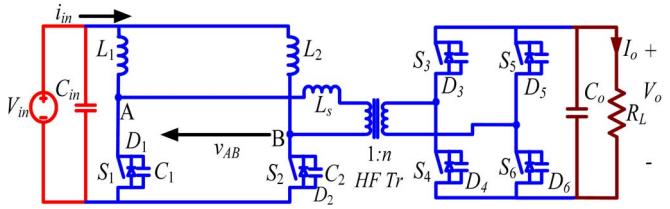

Fig. 3. Proposed ZCS current-fed half-bridge dc/dc converter with full bridge on secondary.

turn-off voltage spike across the switches. However, an active clamp dissipates around 1% of the output power. In addition, it increases the current stresses across the components and introduces circulating current that leads to higher switch rms current. Moreover, it requires two additional active switches, two snubber capacitors, and one high-frequency (HF) capacitor of large value, which increases the component count and converter complexity.

A novel and simple zero-current-switching (ZCS) current-fed half-bridge dc/dc converter is proposed by the authors [25]. Voltage across the switches is clamped without an active clamp or passive snubber. It makes a reduction in size and cost. It improves the converter efficiency by ZCS of primary devices, zero-current turn-on of all devices, and natural commutation of secondary diodes and body diodes of primary devices. Switching transition losses are significantly reduced. It has negligible circulating current and lower conduction losses and, therefore, is expected to show better light load efficiency than hard switching (Fig. 1) and active-clamped circuits (Fig. 2). The proposed converter, as shown in Fig. 3, has bidirectional ability and can be used for battery storage, fuel cell vehicles, and hybrid electric vehicles. This paper demonstrates experimental results and presents complete design and effect of device parasitics on converter operation.

The layout of this paper is as follows. Steady-state operation and analysis of the proposed converter have been explained in Section II. Section III presents a detailed converter design. Effect of parasitics, i.e., device capacitance, has been described in Section IV. The proposed converter analysis and design are verified by simulation results using PSIM 9.0 in Section V. Comparison with active-clamped zero-voltage-switching (ZVS) topology has been reported. Experimental results for a 200-W laboratory prototype have been demonstrated in Section V.

II. Steady-State Operation and Analysis

In this section, steady-state operation and analysis with the ZCS concept have been explained. In the instant before removing the gating signal of the primary-side switch, two diagonal switches on the secondary side are turned on, and the reflected output voltage V_o/n appears across the transformer primary. This diverts the current from the primary switch into the transformer, causing the transformer current to increase and the primary switch current to decrease to zero. Once current decreases below zero, the body diode across the switch starts conducting, and the gating signal is removed, causing its ZCS turn-off. Fixed-frequency duty-cycle modulation is used for control of power transfer and output voltage regulation.

The following assumptions are made for converter analysis: 1) Inductors L_1 and L_2 are large enough to maintain constant current through them; 2) the magnetizing inductance of the transformer is infinitely large; 3) all the components are ideal; and 4) L_s is the leakage inductance of the transformer or a series inductor that includes the transformer leakage inductance.

The steady-state operating waveforms are shown in Fig. 4. The primary-side switches (S_1 and S_2) are operated with gating signals which are phase shifted by 180° with an overlap. The overlap varies with duty cycle that depends on the input voltage and load conditions. The duty cycles of the primary and secondary switches are denoted by d and d_r, respectively. Here, d is always greater than 50%, while d_r is always less than 50%. Switches S_3 and S_6 are operated with a duty ratio of d_r and switched off in synchronous with the switch S_2, as shown in Fig. 4. Similarly, the turn-off of S_4 and S_5 is synchronized with the turn-off of switch S_1. The converter operation during different intervals in a half HF cycle is explained using the equivalent circuits shown in Fig. 5.

Interval 1 (Fig. 5(a); $\boldsymbol{t_o < t < t_1}$): During this interval, both the primary-side switches S_1 and S_2 are conducting and sharing 50% each of the input current. Power is fed to the load by the output capacitor. $i_{L1} = i_{L2} = i_{S1} = i_{S2} = I_{\text{in}}/2$.

Interval 2 (Fig. 5(b); $\boldsymbol{t_1 < t < t_2}$): In this interval, secondary-side switches S_4 and S_5 are turned on at $t = t_1$. It causes voltage V_o/n to appear across the primary of the transformer, and its current i_{Ls} starts building up; hence, the inductor current i_{L1}, which was earlier flowing through switch S_1, is diverted to the transformer primary. Therefore, current i_{S1} through switch S_1 starts decreasing linearly, and current i_{Ls} starts increasing. The currents through the several components are given by

$$i_{Ls} = \frac{V_o}{n \cdot L_S}(t - t_1) \tag{1}$$

$$i_{S1} = \frac{I_{\text{in}}}{2} - \frac{V_o}{n \cdot L_S}(t - t_1) \tag{2}$$

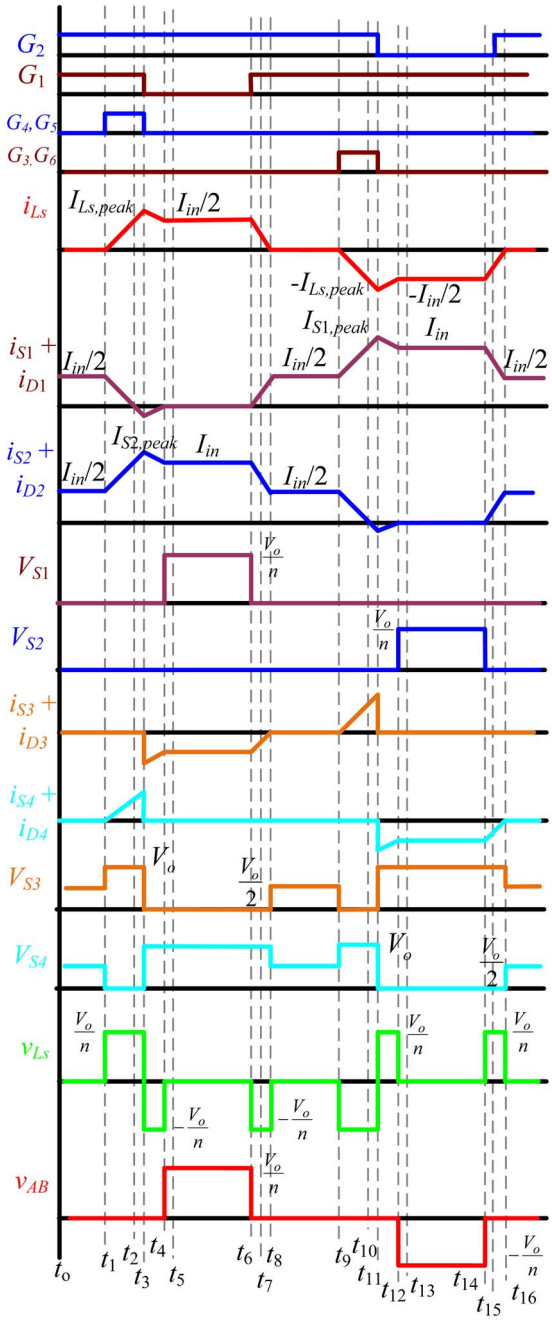

Fig. 4. Operating waveforms of proposed ZCS two-inductor current-fed half-bridge isolated dc/dc converter shown in Fig. 3.

$$i_{S2} = \frac{I_{\text{in}}}{2} + \frac{V_o}{n \cdot L_S}(t - t_1) \tag{3}$$

$$i_{S4} = i_{S5} = \frac{V_o}{n^2 \cdot L_S}(t - t_1). \tag{4}$$

At the end of this interval, switch S_1 current reduces to zero, causing its ZCS turn-off since the gating signal has not been removed yet. Currents i_{Ls} and i_{S2} reach $I_{\text{in}}/2$ and I_{in}, respectively.

Interval 3 (Fig. 5(c); $t_2 < t < t_3$): In this interval, antiparallel diode D_1 of the switch S_1 starts conducting at $t = t_2$. The currents through the transformer and the switches S_2, S_4, and S_5 are increasing with the same slope. At the end of this interval

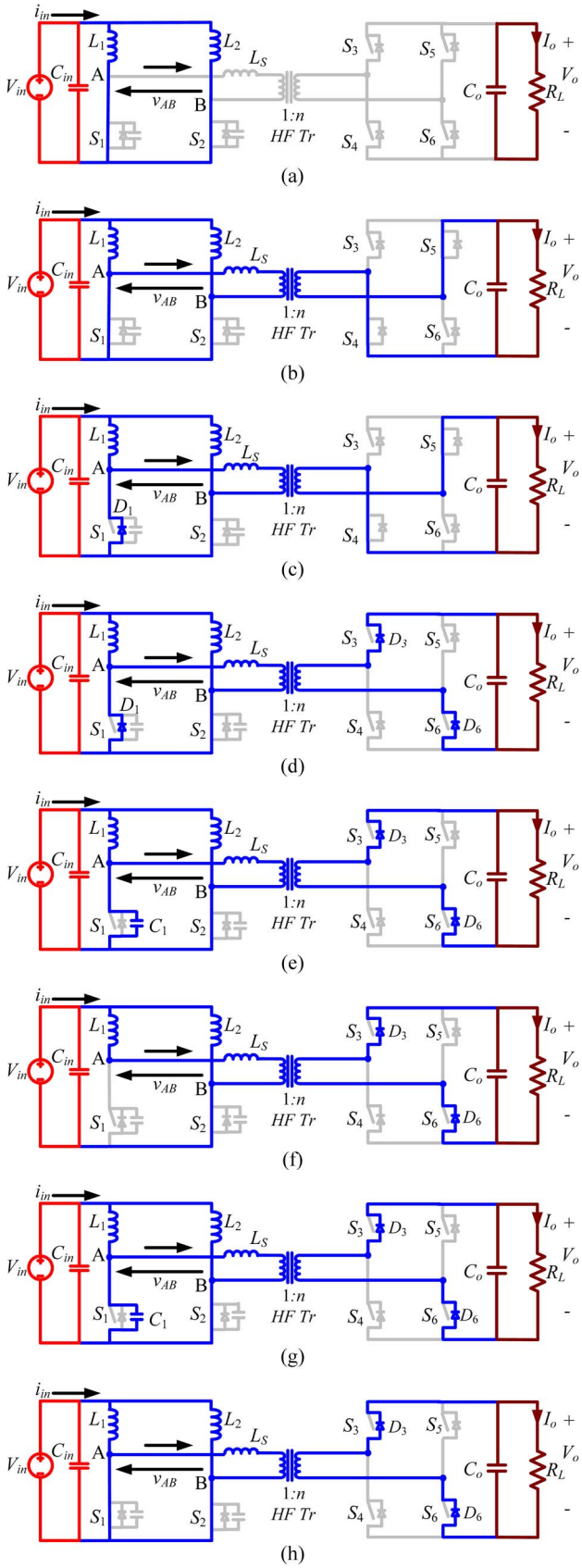

Fig. 5. Equivalent circuits during different intervals of the operation of the proposed converter (Fig. 4) for the steady-state operating waveforms illustrated in Fig. 4. (a) Interval 1. (b) Interval 2. (c) Interval 3. (d) Interval 4. (e) Interval 5. (f) Interval 6. (g) Interval 7. (h) Interval 8.

at $t = t_3$, currents I_{Ls} and i_{S2} reach their peak values. The peak value depends upon the pulsewidth of the gating signal (G_4 and G_5 shown in Fig. 5) applied to secondary switches.

Interval 4 (Fig. 5(d); $t_3 < t < t_4$): Secondary switches S_4 and S_5 are turned off at $t = t_3$. The current on the secondary side is taken over by antiparallel diodes D_3 and D_6 across secondary switches S_3 and S_6, respectively. A negative voltage of $-V_o/n$ appears across the transformer primary, and its current i_{Ls} starts decreasing from its peak value

$$i_{Ls} = I_{Ls,\text{peak}} - \frac{V_o}{n \cdot L_S}(t - t_3) \tag{5}$$

$$i_{S2} = I_{S2,\text{peak}} - \frac{V_o}{n \cdot L_S}(t - t_3). \tag{6}$$

At $t = t_4$, the current through diode D_1 naturally reaches zero. Currents i_{Ls} and i_{S2} reach $I_{\text{in}}/2$ and I_{in}, respectively.

Interval 5 (Fig. 5(e); $t_4 < t < t_5$): During this interval, the snubber capacitor across the primary switch S_1 charges to voltage V_o/n. This interval is very short. Series snubber resistance controls the charging rate.

Interval 6 (Fig. 5(f); $t_5 < t < t_6$): In this interval, the transformer primary voltage is zero; therefore, a constant current $I_{\text{in}}/2$ flows through its primary. Switch S_2 conducts full input current I_{in}. Output capacitor C_o is charged by constant current $I_{\text{in}}/2n$ through the antiparallel diodes D_3 and D_6. G_1–G_6 *are the gating signals for the switches* S_1–S_6, respectively.

Interval 7 (Fig. 5(g); $t_6 < t < t_7$): At $t = t_6$, primary switch S_1 is turned on. The snubber capacitor across it discharges through the series snubber resistance, and switch voltage reduces to zero at the end of this interval. This interval is very short.

Interval 8 (Fig. 5(h); $t_7 < t < t_8$): During this interval, a negative voltage $-V_o/n$ appears across the transformer primary, and its primary current starts falling from $I_{\text{in}}/2$.

Switch S_1 current starts increasing, i.e., current i_{Ls} is transferred to switch S_1. It is the zero-current turn-on of switch S_1. At the end of this interval at $t = t_8$, current i_{Ls} reduces to zero, and switch current I_{S1} increases to $I_{\text{in}}/2$. Their mathematical expressions are given as follows:

$$i_{S1} = \frac{V_o}{n \cdot L_S}(t - t_7) \tag{7}$$

$$i_{Ls} = \frac{I_{\text{in}}}{2} - \frac{V_o}{n \cdot L_S}(t - t_7). \tag{8}$$

A half HF switching cycle terminates at the end of this interval. For the next half HF cycle, the intervals are repeated in a similar sequence with other symmetrical devices conducting to complete the full HF cycle.

III. Design of the Converter

In this section, the converter design procedure is explained by a design example for the following specifications chosen for fuel cell inverter application: input voltage $V_{\text{in}} = 22$–41 V, output voltage $V_o = 350$ V, output power $P_o = 200$ W, and switching frequency $f_s = 100$ kHz.

1) The average input current is $I_{\text{in}} = P_O/(\eta V_{\text{in}})$. Assuming an ideal efficiency η of 100%, $I_{\text{in}} = 9.09$ A.

2) The maximum voltage across the primary switches is

$$V_{\text{SW}} = \frac{V_o}{n}. \tag{9}$$

3) Input and output voltages are related as

$$V_o = \frac{n \cdot V_{\text{in}}}{(1 - d)}. \tag{10}$$

4) Series inductance L_s is calculated using

$$L_s = \frac{2 \cdot V_o \cdot d_r}{n \cdot I_{\text{in}} \cdot f_s}. \tag{11}$$

5) The rms current through the primary switches is given by

$$I_{\text{sw,rms}} = I_{\text{in}} \sqrt{\frac{9 + 4d_r - 6d}{12}}. \tag{12}$$

6) High-frequency transformer design: The transformer turn ratio is selected to achieve low conduction losses in primary switches because converter efficiency primarily depends upon losses in primary switches due to conduction of higher current compared to other components in the converter. Losses in the HF transformer like core loss and copper loss in windings are also considered while selecting the turn ratio. Selecting a transformer with a higher turn ratio requires lower voltage switches [using (9)] featuring low ON-state resistance introducing lower conduction loss. On the contrary, a higher transformer turn ratio results in higher switch rms current and enforces a duty ratio of primary switches below 0.5 to regulate output voltage at higher input voltage values [using (10) and (12)].

Based on the appearing maximum voltage, switches are selected and given in Table I. The maximum duty ratio corresponding to an input voltage of 22 V is calculated using (10) for several values of transformer turn ratio, keeping the secondary duty ratio d_r to 0.05. Next, conduction losses in primary switches using corresponding ON-state resistance of the selected devices are determined.

The number of turns on the primary and secondary of the transformer is calculated for various turn ratios, keeping the maximum flux density in the core identical for all cases. Based on the primary and secondary winding currents, gauge of windings is chosen, and winding resistances are calculated. Individual copper and core losses in the transformer are estimated, and the total is tabulated in Table I.

The plot of combined conduction loss in primary switches and transformer losses with respect to various turn ratios is shown in Fig. 6. Small values of the transformer turn ratio, i.e., $n \leq 3.5$, result in high values of the primary switch duty ratio $d > 0.8$. For a larger value of duty ratio, power has to be transferred to the secondary in a shorter time of $(1 - D)T_s$, resulting in higher peak current. At low values of turn ratios of $n \leq 3.5$, the voltage across the switch is higher, and the ON-state resistance $R_{\text{ds,on}}$ of corresponding switches

TABLE I
CALCULATED CONVERTER PARAMETERS AS A DESIGN EXAMPLE

n	V_{sw} (V)	d_r	L_s (μH)	Selected switch	Conduction loss (W)	Transformer Loss (W)	Remarks
2.5	140	0.84	15.4	IRFB4229GPbF 250 V, 46 A, 38 mΩ	3.795	2.92	Large secondary peak current i.e. low power transfer time (1-*D*), and higher conduction losses
3	116.7	0.81	12.8	IRFB4127GPbF 200 V, 54 A, 20 mΩ	2.088	3.09	Large secondary peak current, i.e. low power transfer time (1-*D*)
3.5	100	0.78	11.0	IRFB4127GPbF 200 V, 54 A, 20 mΩ	2.179	3.25	Large secondary peak current, i.e. low power transfer time (1-*D*)
4	87.5	0.75	9.6	IRFB4115GPbF 150 V, 74 A, 11 mΩ	1.248	3.4	Suitable
4.5	77.8	0.72	8.6	IRFB4115GPbF 150 V, 74 A, 11 mΩ	1.298	3.54	Suitable
5	70.0	0.69	7.7	IRFB4115GPbF 150 V, 74 A, 11 mΩ	1.348	3.67	Voltage Regulation issue
5.5	63.6	0.65	7.0	IRFB4115GPbF 150 V, 74 A, 11 mΩ	1.398	3.80	Voltage Regulation issue
6	58.3	0.62	6.4	IRFB4110GPbF 100V, 120A, 4.5mΩ	0.593	3.92	Voltage Regulation issue

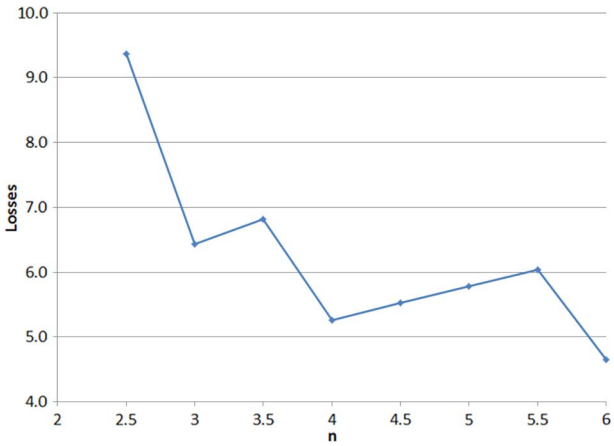

Fig. 6. Losses including conduction loss in primary switches and transformer losses with respect to turn ratio n.

is higher, resulting in higher conduction loss. The cost of the device increases with the voltage rating. On the other hand, when $n > 4.5$, duty ratio d goes below 0.75. Although this works at $V_{\rm in} = 22$ V, the duty ratio has to go below 0.5 to regulate output voltage at higher values of $V_{\rm in} = 41$ V. However, the duty ratio has to be maintained always above 0.5 to provide a current path to pass or circulate the input boost inductor currents, i.e., both the primary switches cannot be turned off at a time. From the aforementioned discussion, designs with $n = 4$ and 4.5 are competitive. However, with low switch rms current, i.e., low losses and better duty cycle range for voltage regulation over wide fuel cell voltage range, $n = 4$ is selected for this application. A designer can follow the same procedure with its own selected switches based on the requirements. Here, low-cost devices of similar values are selected based on voltage rating. Here, d_r is set to 0.05. Using (11), the leakage inductance of the transformer is calculated to be $L_s = 9.6$ μH. The maximum voltage across the secondary switches is equal to output voltage V_o. Switches of 600 V are used on the secondary side.

Peak and rms values of the transformer primary current are

$$I_{Ls,\rm peak} = \frac{V_o \cdot d_r}{n \cdot f_s \cdot L_S} \tag{13}$$

$$I_{Ls,\rm rms} = I_{\rm in}\sqrt{\left[\frac{(1-d)}{2} + \frac{d_r}{3}\right]}. \tag{14}$$

7) The necessary condition of ZCS of primary switches is

$$d_r \geq \frac{I_{\rm in} \cdot n \cdot L_s \cdot f_s}{2 \cdot V_o}. \tag{15}$$

For ensuring ZCS, the value of d_r is kept a little higher than the critical value given by (15). For this additional time, the antiparallel diode of the switch conducts. However, in order to limit the peak and circulating current through the components, d_r should not be too high than its critical value.

8) Boost inductors: The values of the boost inductor are given by

$$L_1 = L_2 = (V_{\rm in})(D)/\left[(\Delta I_{\rm in})(f_s)\right] \tag{16}$$

where $\Delta I_{\rm in}$ is the boost inductor ripple current.

For $\Delta I_{\rm in} = 1$ A, $L = 176$ μH. The maximum voltage across the inductors is equal to $V_o/n - V_{\rm in} = 53$ V.

9) Secondary switches: The peak current through the secondary switches is

$$I_{\rm sw,sec,peak} = \frac{I_{\rm in}}{2 \cdot n}. \tag{17}$$

10) Output capacitor: The value of output filter capacitor C_o is

$$C_o = \frac{(I_0) \cdot (D - 0.5)}{\Delta V_o \cdot f_S} \tag{18}$$

where ΔV_o is the allowable ripple in output voltage and $C_o = 4.2$ μF for $\Delta V_o = 0.5$ V. Its voltage rating is equal to $V_o = 350$ V.

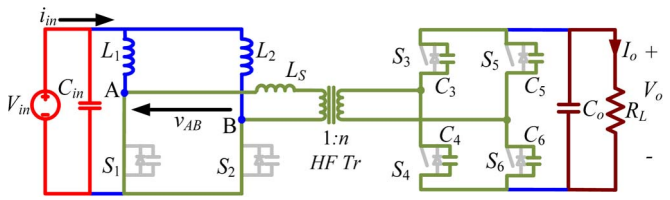

Fig. 7. Equivalent circuit during intervals 1 and 9, considering device capacitance of the secondary switches.

IV. Effect of Device Parasitic

Steady-state analysis of the converter explained in Section II assumes ideal devices. The devices used in a practical converter system have parasitic. Although the performance of the converter does not change considerably due to output capacitance, it slightly modifies the operating waveforms during a few intervals.

The effect of the output capacitance of the secondary switches is prominent in intervals 1 and 9. At the end of interval 8 at $t = t_8$, the secondary current of the transformer reduces to zero. The voltage across the switch capacitances C_4 and C_5 is charged to output voltage V_o. The equivalent circuit during this interval is as shown in Fig. 7. Series inductance L_S resonates with the device capacitances C_3–C_6. The resonant frequency is given by

$$\omega_r = \frac{1}{\sqrt{n^2 \cdot L_S \cdot C_{\text{eq}}}} \tag{19}$$

where C_{eq} is the equivalent capacitance across the transformer secondary. Considering all device capacitances to be equal, C_{eq} is obtained as

$$C_{\text{eq}} = C_3 = C_4 = C_5 = C_6. \tag{20}$$

The respective voltages across the switch capacitances during interval 9 are given by

$$V_{S3} = V_{S6} = \frac{V_o}{2} + \frac{V_o}{2}\cos\left[\omega_r(t - t_8)\right] \tag{21}$$

$$V_{S4} = V_{S5} = \frac{V_o}{2} - \frac{V_o}{2}\cos\left[\omega_r(t - t_8)\right]. \tag{22}$$

Currents through the secondary i_{sec} and primary of the transformer i_{Ls} are given as follows:

$$i_{\text{sec}} = -\frac{V_o}{\omega_r \cdot n^2 \cdot L_S}\sin\left[\omega_r(t - t_8)\right] \tag{23}$$

$$i_{Ls} = -\frac{V_o}{\omega_r \cdot n \cdot L_S}\sin\left[\omega_r(t - t_8)\right]. \tag{24}$$

Similar oscillations at identical resonant frequency ω_r are observed during interval 1, $t_o < t < t_1$.

V. Simulation and Experimental Results

In this section, simulations and experimental results for a 200-W converter design are presented. Simulation was performed on PSIM 9.0 to verify the converter analysis and design. Simulation results are shown in Figs. 8–11 and closely match with the theoretical waveforms given in Fig. 4.

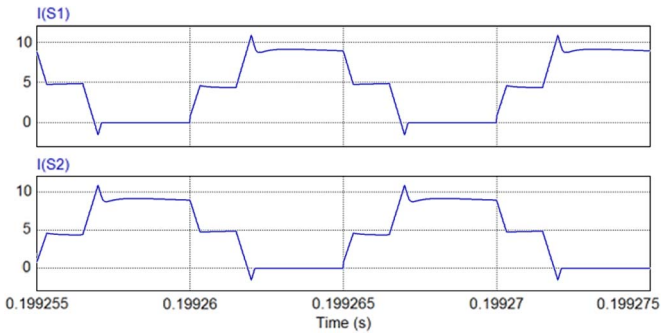

Fig. 8. Current in the primary-side switches showing ZCS turn-off.

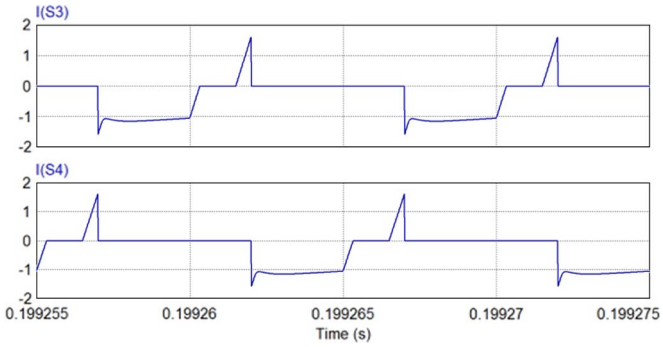

Fig. 9. Current flowing through the secondary-side switches.

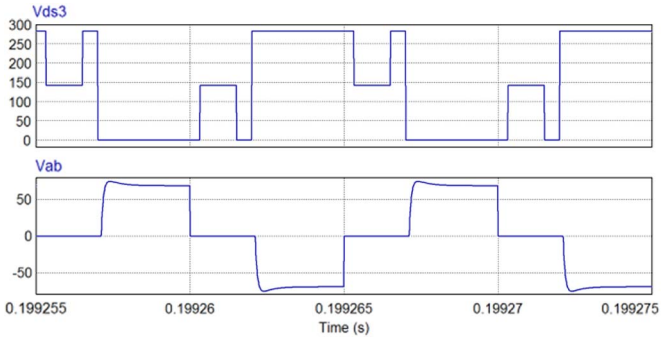

Fig. 10. Waveforms showing voltage across the secondary switch and voltage across the primary of the HF transformer.

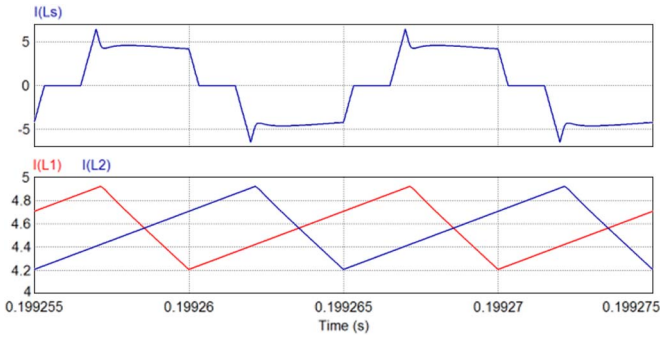

Fig. 11. Current through the primary of the transformer and current in the boost inductors.

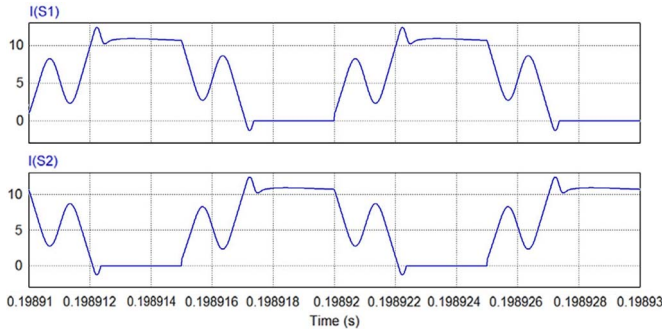

Fig. 12. Current waveforms through primary switches i_{S1} and i_{S2}.

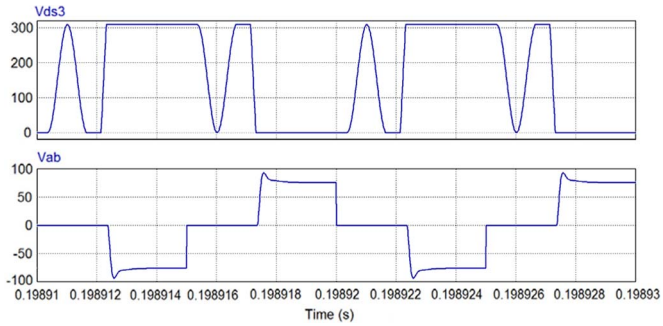

Fig. 13. Voltages across the secondary switch and primary of the transformer.

Figs. 8–11 show simulation results with ideal components for $V_{\rm in} = 22$ V at 200 W. Fig. 8 presents ZCS turn-off of the primary switches. It is clear that each switch current reaches zero naturally and the antiparallel body diode conducts, causing a zero voltage across it. Therefore, a switch turn-off snubber is not needed, and the gate signal is removed. In addition, the currents through the switches build up with a slope resulting in their zero-current turn-on.

Fig. 9 shows the current through the secondary switches, including the current through their body diodes. It shows the zero-current turn-on of secondary switches as the current starts conducting from zero and builds up with a slope that depends upon the reflected value of L_s. The voltage across the secondary device is shown in Fig. 10. Voltage becomes zero when either the diode conducts or the switch is turned on. When switches S_4 and S_5 are conducting, the voltage across switch S_3 is V_o. Voltages across all the switches become $V_o/2$, when current through the antiparallel diode reaches zero. Fig. 10 also shows the voltage across the primary of the transformer. Whenever one of the primary switches is turned off, output voltage is reflected across the primary of the transformer. Voltage $V_{\rm AB}$ is zero during conduction of both the primary switches.

Fig. 11 shows the transformer primary current (i_{Ls}) and the current through input inductors (i_{Ls} and i_{L2}). The simulation waveform of current i_{Ls} matches with that of the analysis performed in Section II. The ripple frequency of i_{L1} and i_{L2} is the same as switching frequency $f_s = 100$ kHz. Since these two currents are phase shifted by 180°, the ripple frequency of input current $I_{\rm in}$ is 200 kHz, which is twice the switching frequency f_s.

Additional simulation is performed considering device capacitance of the secondary switches for $V_{\rm in} = 22$ V and $P_o = 200$ W. Figs. 12 and 13 show simulation waveforms to compare with the analytical description given in Section IV.

Fig. 12 shows ZCS turn-off of the primary switches. Their currents reach zero naturally, and antiparallel body diodes conduct, causing a zero voltage across them. However, clear difference can be noticed compared with Fig. 8, where device capacitance is neglected. When current reaches $I_{\rm in}/2$, it starts oscillating due to resonance between transformer series inductance and device capacitance of the secondary switches. Similarly, oscillations are observed in waveforms showing the voltage across the secondary switch in Fig. 13. Transformer primary voltage is unaffected by the device capacitance which is similar to the waveform shown in Fig. 10.

TABLE II
COMPARISON OF PARAMETERS BETWEEN ACTIVE-CLAMPED ZVS AND PROPOSED ZCS CURRENT-FED HALF-BRIDGE TOPOLOGIES

Parameters	Active-clamped ZVS	Proposed ZCS
Peak current through transformer $I_{Ls,peak}$ (A)	9.1	4.55
RMS current through transformer $I_{Ls,rms}$ (A)	3.8	3.4
Peak current through primary switches $I_{S1,peak}$ (A)	13.6	9.1
RMS current through primary switches $I_{S1,rms}$ (A)	6.3	5.7
Peak current through secondary switches/diodes (A)	2.3	1.14
RMS current through secondary switches/diodes (A)	0.66	0.55
Voltage across primary switches V_{s1} (V)	110	87.5
Rating of primary switches (VA)	693	498.75
Transformer rating (VA)	334	238

A comparison between active-clamped ZVS and proposed ZCS current-fed half-bridge topologies has been illustrated in Tables II and III. It is clear from Table II that the proposed ZCS converter has reduced voltage and peak current stresses across the switches and transformer. Also, it requires transformer and switches of lower volt-ampere rating. Therefore, it results in small size and low cost.

Higher efficiency is obtained due to saving in losses in active-clamp circuit and reduced circulating current through the switches, as shown in Table III. All these advantages come without any added components and cost but with reduced components and cost. This makes this contribution novel.

The total losses in equivalent series resistance (ESR) of the capacitor and the Q losses in inductors are assumed equal to 0.5% of the rated power. Improvement in efficiency by 3.1% enhances the source utilization and saving in fuel cells. Also, the reduced components (absence of an active clamp) result in low cost and reduced size.

Fig. 14 shows the picture of a 200-W laboratory prototype of the experimental converter. Its details are as follows.

TABLE III
COMPARISON OF LOSSES AND EFFICIENCY BETWEEN ACTIVE-CLAMPED ZVS AND PROPOSED ZCS CURRENT-FED HALF-BRIDGE TOPOLOGIES

Parameters	Active-clamped ZVS	Proposed ZCS
Conduction losses in primary switches (W)	2.8	1.2
Conduction losses in auxiliary switches (W)	1.4	-
Conduction losses in secondary switches/diodes (W)	2.4	2.34
Primary switches turn-off losses (W)	1.65	ZCS
Primary switches turn-on losses (W)	ZVS	2.53
Auxiliary switches turn-off losses (W)	1.1	-
Turn-off losses in secondary switches (W)	-	0.53
Transformer losses	3.72	2.93
Extra losses (W): (ESR of filters + parasitics etc.)	1	1
Total losses (W)	14	10.5
% Losses	7	5.25

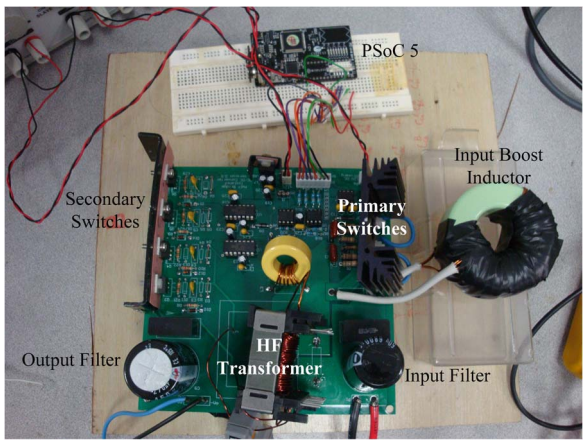

Fig. 14. Experimental prototype showing various components.

The input boost inductors have a T250-40 magnetics molypermalloy powder (MPP) core, $N = 26$, $L_1 = L_2 = 195\ \mu$H, and four strands of SWG19.

The input filter capacitors are a 6800-μF 100-V electrolytic capacitor and a 1-μF 275-V HF film capacitor.

The primary switches S_1 and S_2 are IRFB4115PBF, with 150 V, 100 A, and $R_{\mathrm{ds,on}} = 9.3\ \mathrm{m}\Omega$.

The HF transformer has a PC40ETD44-Z ferrite core, primary turns of 20, secondary turns of 80, and a leakage inductance (reflected to the primary side) equal to 1.54 μH. The HF transformer is designed by limiting the maximum flux density to 0.05 T, and a core that avoids saturation is selected accordingly. Litz wires are used.

The external series inductance is T106-26, with $N = 5$ turns and four strands of SWG19.

The secondary switches S_3–S_6 are FGP5N60LS 600-V 10-A discrete insulated-gate bipolar transistors (IGBTs) with an IDD05SG60C external Schottky diode in parallel. Since reverse recovery of the body diode of MOSFET is more than 250 ns, a discrete IGBT with an external SiC Schottky diode is used in the converter.

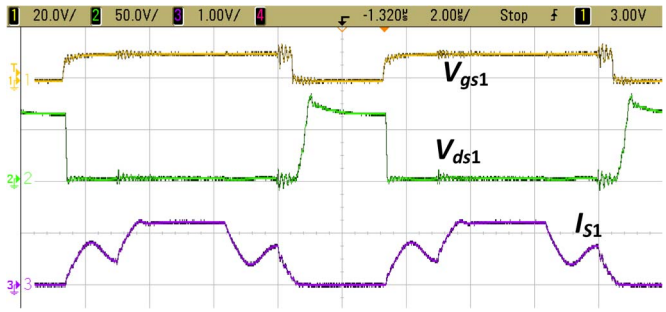

Fig. 15. Experimental results: Primary switch gate voltage V_{gs1} (20 V/div), switch voltage V_{ds1} (50 V/div), and current I_{S1} (10 A/div).

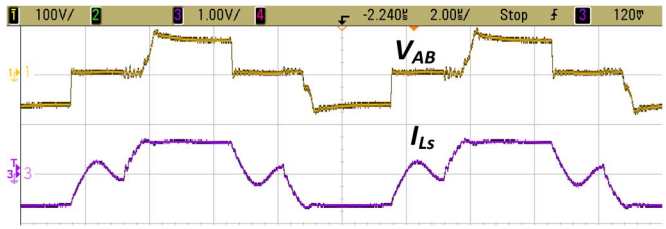

Fig. 16. Experimental results for voltage V_{AB} (100 V/div) across and current I_{LS} (10 A/div) through primary of the transformer.

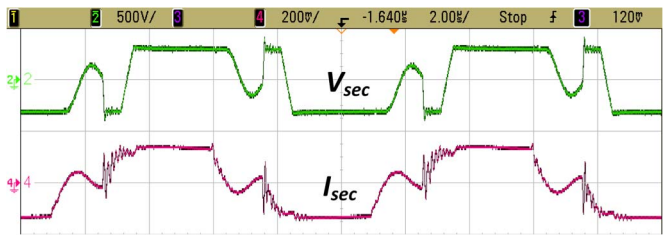

Fig. 17. Experimental results for voltage V_{sec} (500 V/div) across and current I_{sec} (2 A/div) through secondary of the transformer.

The output filter capacitors are a 270-μF 450-V electrolytic capacitor and 0.68-μF 450-V HF film capacitors.

For the gate drivers, IR2181 is used to drive primary-side MOSFETs, and IR21834 is used for secondary-side IGBTs.

For the gating signal generation, gating signals for the devices are generated on Cypress Programmable System-on-Chip 5. It is more economical, user friendly, easy to program, and simple to use. It is of smaller volume and size compared to DSP and field-programmable gate array (FPGA) kits of similar functionality.

Figs. 15–19 show the experimental results for $V_{\mathrm{in}} = 22$ V and $P_o = 200$ W. ZCS of the primary can be clearly observed from the waveform given in Fig. 15. Current in the primary device I_{S1} reaches zero naturally before the gate signal V_{gs1} is removed. The voltage across the switch V_{ds1} rises only after gate voltage V_{gs1} is removed. Switch voltage V_{ds1} is clamped at reflected output voltage. Clamping of the device voltage is achieved simply by modulation of secondary switches without any additional active clamp or snubber circuit.

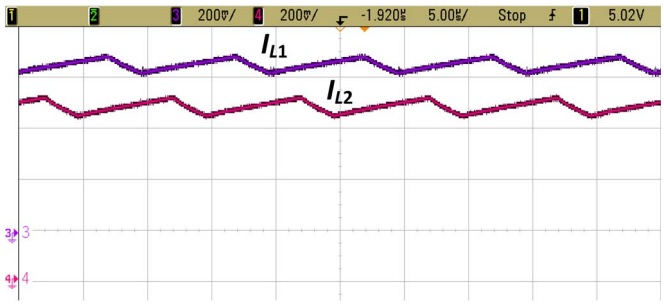

Fig. 18. Experimental result showing current through the boost inductors I_{L1} and I_{L2} (2 A/div).

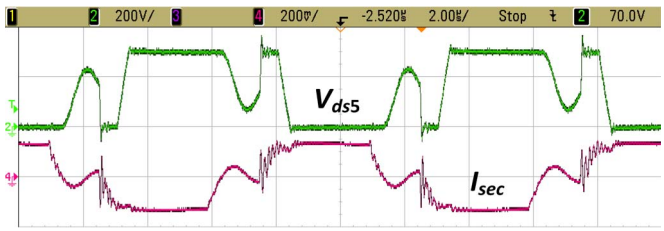

Fig. 19. Voltages across the secondary switch V_{ds5} (200 V/div) and current through the secondary switch $I_{\rm sec}$ (2 A/div).

Fig. 16 shows the voltage across the primary of the transformer $V_{\rm AB}$ and the primary current I_{LS}. The voltage across the primary $V_{\rm AB}$ is zero when both the primary switches are turned on and equal to voltage V_o/n when one of the switches is turned off. This shows the clamping of voltage appearing across the primary devices without any external clamping circuit. Oscillation in current through the transformer primary I_{LS} shown in Fig. 16 validates the effect of device capacitance. These results match very well with the simulation results and the analytically predicted waveforms, as shown in Fig. 4.

The voltage across the secondary of the transformer $V_{\rm sec}$ and the secondary current $I_{\rm sec}$ are shown in Fig. 17. Oscillation due to resonance between transformer secondary and secondary device capacitances can be observed when current in the transformer secondary reaches zero. Due to parasitics in the board, current has oscillations when the secondary switches are turned on, i.e., when voltage $V_{\rm sec}$ becomes zero.

Fig. 18 shows the current waveforms I_{L1} and I_{L2} through the boost inductors which are phase shifted by 180° due to the phase shift in gating signals of the two primary switches. This phase shift results in 200-kHz ripple frequency at input current, achieving reduced input current ripple.

The experimental voltage waveform across the secondary switch V_{ds5} is shown in Fig. 19 along with secondary current $I_{\rm sec}$. The voltage across the device is zero when either switch or antiparallel diode is conducting. Discrete IGBT with a Schottky diode in parallel is used to avoid reverse recovery losses as compared to 600-V MOSFET because its body diode has a reverse recovery time of $>$ 250 ns. It is a concern on the secondary side because, for majority of the time, the diode conducts. Figs. 20 and 21 show experimental results for $V_{\rm in} =$ 30 V and $P_o = 150$ W, indicating ZCS and voltage clamping of primary devices along with low peak currents.

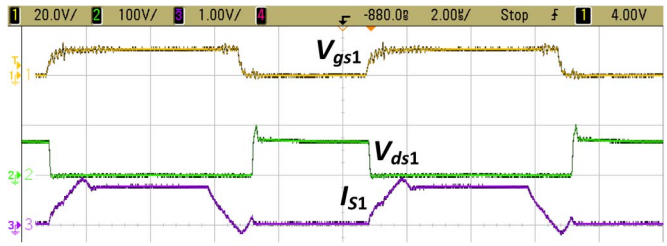

Fig. 20. Experimental results: Primary switch gate voltage V_{gs1} (20 V/div), switch voltage V_{ds1} (100 V/div), and current I_{S1} (10 A/div).

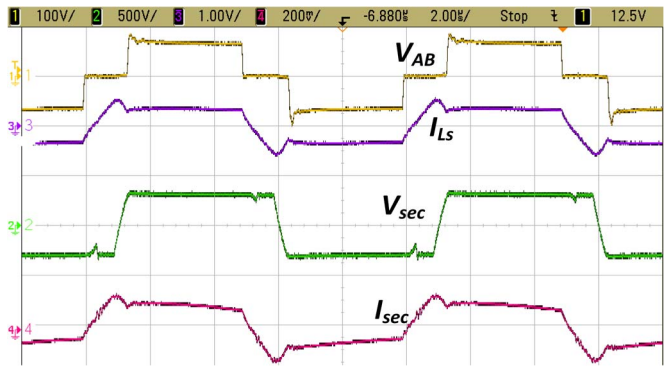

Fig. 21. Experimental results for voltage $V_{\rm AB}$ (100 V/div) across and current I_{LS} (10 A/div) through primary of the transformer and voltage $V_{\rm sec}$ (500 V/div) across and current $I_{\rm sec}$ (2 A/div) through secondary of the transformer.

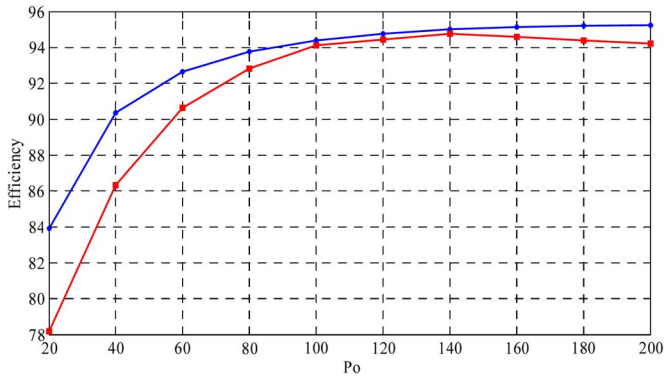

Fig. 22. Plot of efficiency versus output power obtained for different load conditions at $V_{\rm in} = 22$ V; circles (blue) for proposed ZCS converter and square (red) for active-clamped ZVS converter.

Converter efficiency (blue circles) is compared with the efficiency of an active-clamped ZVS half-bridge converter (red squares) under varying load conditions for $V_{\rm in} = 22$ V and is plotted as shown in Fig. 22. The maximum efficiency of 95% is obtained at full load. Efficiency can be improved by accurate design of printed circuit board (PCB), reducing the losses due to parasitics.

VI. Summary and Conclusion

This paper has proposed a novel current-fed converter that provides a secondary-side-modulation-based solution to the switch turn-off voltage spike problem. It relieves the need of extra snubber circuit, making the proposed concept novel and

snubberless. This reduces component count and peak current through the primary switches, and the transformer has been reduced. Voltage of the primary-side switches is clamped at reflected output voltage. Therefore, a design with selection of low-voltage devices is possible. Low-voltage and low-current devices are less costly and result in compact converters. In addition, such devices have low ON-state resistance, resulting in low conduction losses, and enhance converter efficiency. It maintains soft switching of all the devices as well as natural or zero-current commutation of body diodes of primary devices as well as secondary diodes, resulting in low switching losses.

Steady-state operation, analysis, and design of the proposed converter have been presented. An experimental low-power laboratory prototype of the converter was developed and tested. Experimental results demonstrate the accuracy of the proposed analysis and design. This converter topology is suitable for low-voltage high-current applications such as fuel cell, PV, and battery source applications. The proposed converter has bidirectional power flow ability.

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Udupi R. Prasanna (M'11) received the B.E. degree in electrical and electronics engineering from the National Institute of Technology Karnataka, Surathkal, India, in 2006 and the Ph.D. degree in power electronics and alternate energy conversion from the Indian Institute of Science, Bangalore, India in 2011.

He was a Postdoctoral Research Fellow in the Department of Electrical and Computer Engineering, National University of Singapore, from July 2011 to January 2013. Currently, he is working at The University of Texas at Dallas, Richardson, TX, USA, as a Research Scholar. His research interests mainly include high-frequency soft-switching power converters, hybrid energy management in the field of alternate energy sources, hybrid electric vehicles, fuel cell vehicles, and modeling of multi-disciplinary energy systems using bondgraph technique. He is a Reviewer for IEEE TRANSACTIONS, and IET, Elsevier, and Inderscience journals.

Akshay K. Rathore (M'05–SM'12) received the B.E. degree in electrical engineering from the Maharana Pratap University of Agriculture and Technology, Udaipur, India, in 2001, the M.Tech. degree in electrical machines and drives from the Indian Institute of Technology (Banaras Hindu University) Varanasi, Varanasi, India, in 2003, and the Ph.D. degree in power electronics from the University of Victoria, Victoria, BC, Canada, in 2008.

He was a Lecturer with the College of Technology and Engineering, Udaipur, from February 2003 to August 2004 and with the Mody Institute of Technology and Science, Lakshamangarh, India. From May to December 2007, he was a Sessional Lecturer with the Department of Electrical and Computer Engineering, University of Victoria. From September 2008 to August 2009, he was a Postdoctoral Research Fellow with the Electrical Machines and Drives Laboratory, University of Wuppertal, Wuppertal, Germany. Subsequently, from September 2009 to September 2010, he was a Postdoctoral Research Associate with the University of Illinois, Chicago, IL, USA. Since November 2010, he has been with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore, where he is currently an Assistant Professor. He is a Reviewer of IET and Elsevier journals and an Associate Editor of the *International Journal of Power Electronics*. He is also an Editor of *Electric Power Components and Systems*. He has contributed to nearly 70 research papers and delivered three tutorials on current-fed soft-switching converters. His research interests include soft-switching techniques, high-frequency power conversion for distribution generation and renewable energy sources (fuel cells and photovoltaic), current-fed topologies, modulation techniques, electric and fuel cell vehicles, energy storage, and high-performance control of motor drives and power converters.

Dr. Rathore was listed in Marquis Who's Who in Science and Engineering in 2006, Who's Who in the World, and Who's Who in America in 2008. He is also a Reviewer of IEEE TRANSACTIONS. He is an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, IEEE TRANSACTIONS ON POWER ELECTRONICS, and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He was a guest Associate Editor for a special issue on transportation electrification and vehicle systems in the IEEE TRANSACTIONS ON POWER ELECTRONICS to appear in January 2014 and is a guest Associate Editor for a special issue on transportation electrification in the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is a Technical Track Chair for the IEEE Industrial Electronics Conference (IECON) 2013 to be held in Vienna, Austria, was a Technical Track Chair for the IEEE Power Electronics and Drive Systems (PEDS) Conference 2013 held in Kitakyushu, Japan, and IECON 2012 held in Montreal, Canada, and was a Tutorial Chair for the IEEE PEDS Conference 2011 held in Singapore. He was a recipient of the University Ph.D. Fellowship, the Thouvennelle Graduate Scholarship, and the Natural Sciences and Engineering Research Council of Canada Research Assistantship during his Ph.D. studies.

Sudip K. Mazumder (SM'02) received the B.E. degree from the University of Delhi, Delhi, India, in 1989, the M.S. degree from Rensselaer Polytechnic Institute, Troy, NY, USA, in 1993, and the Ph.D. degree from Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, in 2001.

He is currently a Professor with the Department of Electrical and Computer Engineering, University of Illinois, Chicago, IL, USA, where he is also the Director of the Laboratory for Energy and Switching Electronics Systems. He has more than 15 years of professional experience. He has held R&D and design positions in leading industrial organizations. He was the first Editor-in-Chief of the *International Journal of Power Management Electronics* (currently called *Advances in Power Electronics*) between 2006 and 2009. His current research interests include interactive power electronics/power networks, renewable and alternative energy systems, photonically triggered and wide-bandgap-based power semiconductor devices, and applied technologies.

Dr. Mazumder has been an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON AEROSPACE AND ELECTRONIC SYSTEMS, and IEEE TRANSACTIONS ON POWER ELECTRONICS since 2003, 2008, and 2009, respectively. He was the Cochair of the IEEE Power Electronics Technical Committee on Sustainable Energy Systems. He was the Vice Chair of the Technical Program Committee of the 2010 IEEE Energy Conversion Conference and Exposition. He was the Chair of the Student/Industry Coordination Activities for the 2009 and 2010 IEEE Energy Conversion Congress and Exposition. He was also the Technical Program Committee Cochair of the 2010 IEEE International Symposium on Power Electronics for Distributed Generation Systems. He has been invited by the IEEE and the American Society of Mechanical Engineers, as well as multiple industries, federal agencies, national laboratories, and universities, for several keynote, plenary, and invited lectures and presentations. He was a recipient of the prestigious 2011 Teaching Recognition Program Award, the prestigious 2008 Faculty Research Award, the 2006 Diamond Award from the University of Illinois for outstanding research performance, the Office of Naval Research Young Investigator Award, National Science Foundation CAREER Awards in 2005 and 2002, and the IEEE TRANSACTIONS ON POWER ELECTRONICS Prize Paper Award in 2002. He was also a corecipient of the 2007 IEEE Outstanding Student Paper Award at the IEEE International Conference on Advanced Information Networking and Applications.