A Soft-Switched Hybrid-Modulation Scheme for a Capacitor-Less Three-Phase Pulsating-DC-Link Inverter

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***Abstract*—A soft-switched hybrid-modulation (HM) scheme is outlined for a dc-link-capacitor-less three-phase high-frequency (HF) pulsating-dc link (PDCL) isolated multistage inverter. The overall inverter comprises a front-end isolated dc/pulsating-dc converter followed by a pulsating-dc/ac converter. Because the two stages are directly connected without a dc-link capacitor, the intermediate link is a PDCL instead of a fixed-dc link as in conventional HF-link inverters. The HM modulates the pulsating-dc/ac converter such that, two of its converter legs are line-switched, while the third leg of the pulsating-dc/ac converter is switched under zero-voltage-switching condition. This is achieved by first modulating the dc/pulsating-dc converter to achieve a specific encoding of the PDCL signal, which in turn, is exploited by the modulation scheme of the pulsating-dc/ac converter to mitigate its switching loss without requiring any auxiliary circuit. Operation of the pulsating-dc/ac converter using the soft-switched HM scheme is validated using a prototype 1 kW, 72-V (dc)/208-V (ac) HF inverter.**

***Index Terms*—Capacitor-less, high-frequency (HF) link, hybrid modulation, inverter, pulsating-dc link (PDCL), soft switching, three phase.**

I. Introduction

A pulsating-dc link (PDCL) high-frequency (HF) inverter topology is suitable for multiple applications including solar energy, fuel-cell energy, wind energy, energy storage, electrical vehicles, and power quality. It yields high power density due to elimination of line-frequency (LF) transformers with HF transformers and elimination of dc-link. Fig. 1 shows a simplified structure of a PDCL HF inverter that consists of two conversion stages: 1) a dc/pulsating-dc converter that comprises dc/ac converters, HF transformers, and an ac/pulsating-dc converter; and 2) a pulsating-dc/ac converter that generates the desired LF output ac voltages. Well-known sine-wave pulse-width modulation or space-vector modulation schemes can be used to derive the LF output ac voltages for single-phase and three-phase inverters [1]–[13]. However, multistage power conversion of the PDCL inverter requires a carefully designed switching scheme to reduce device losses of the inverter and ensure the synthesis of the inverter output waveforms with acceptable harmonic distortion.

One such modulation scheme is described in [14] that uses a square-wave modulation scheme. It uses the square-wave modulation for the dc/ac converter. Using such a modulation, the dc/ac converter generates a stream of pulses with fixed on-time width on the PDCL. As such, a sine-wave modulation technique must be applied to the pulsating-dc/ac converter to generate the line-frequency ac output voltages. Therefore, all the legs of the pulsating-dc/ac converter operate at HF under hard-switching condition. Discontinuous-modulation schemes [15]–[19] can reduce the switching loss of the pulsating-dc/ac converter by allowing no switching of one of the legs of the three-leg converter. Therefore, these schemes yield no commutation of a leg for a specific angular duration (e.g., 30° or 60°) of any line cycle. However, this still incurs HF switching of the remaining legs of the converter under hard-switching condition.

The originally proposed HM scheme (referred to as the conventional HM in this paper), described in [20]–[23], can be applied to the pulsating-dc/ac converter to decrease the switching requirements of the converter. Unlike the discontinuous-modulation schemes, the conventional HM scheme requires no HF commutation on two of the legs of the pulsating-dc/ac converter. Therefore, only one of the three legs operates under HF hard-switching condition. This additional reduction in switching is achieved by recognizing that, if the dc/ac converter switches are sinusoidally modulated (emulating the inverter output), the PDCL signal, representing the maximum (dc/ac-converter) phase-to-phase voltage, is also encoded with this sinusoidal information, which is exploited by the HM to reduce switching need for the pulsating-dc/ac converter. Because the maximum phase-to-phase voltage of the dc/ac converter changes every 60° of the line cycle, the HM of the pulsating-dc/ac converter appropriately selects the two converter legs that are not switched in this 60° interval. Notwithstanding, switching loss incurred in the remaining converter leg that is hard-switched needs to be addressed.

As such, in this paper, a soft-switched HM scheme is developed to provide soft-switching condition for the pulsating-dc/ac converter. A novel and fundamentally different modulation scheme must be applied to the dc/ac converter to enable soft-switched HM of the pulsating-dc/ac-converter switches. Using this scheme, the two predetermined legs of the pulsating-dc/ac

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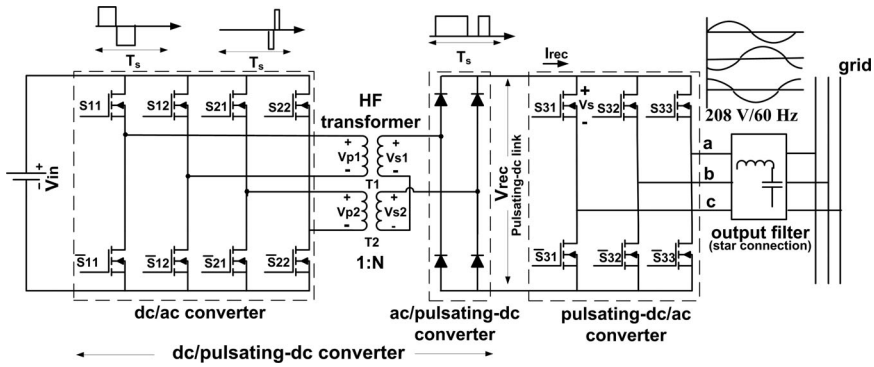

Fig. 1. Schematic of the PDCL HF inverter which operates using the soft-switched HM scheme.

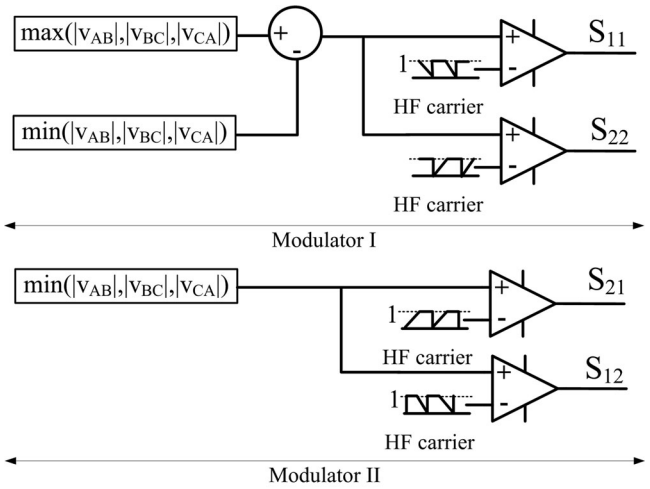

Fig. 2. Switching signal generation for the dc/ac converter (dc/ac modulator).

converter are not switched in every 60° of the line cycle while the other leg works at HF but under soft-switching condition. Therefore, soft-switched HM scheme proposes unique modulation mechanism for the dc/ac and the pulsating-dc/ac converters.

This paper consists of four additional sections. The principle of operation of the soft-switched HM scheme is outlined in Section II. Section III describes the modes of operation of the PDCL HF inverter (as shown in Fig. 1) using the soft-switched HM scheme. In Section III, key simulation and experimental results, obtained using a 1-kW prototype PDCL HF inverter, are presented to validate the performance of the soft-switched HM scheme. Finally, conclusions based on the novel HM scheme are outlined in Section IV.

II. Principle of Operation

PDCL HF inverter consists of two active stages, which are the front-end dc/ac and pulsating-dc/ac converters. The dc/ac converter generates width modulated bipolar pulses for HF transformers. The modulated voltage pulses across the secondary sides of the HF transformers are rectified by the ac/pulsating-dc converter to generate the PDCL waveform. An RCD snubber [24] is used to limit the voltage spikes on the PDCL waveform due to the leakage inductances of the HF transformers and parasitic output capacitors of the ac/pulsating-dc converter.

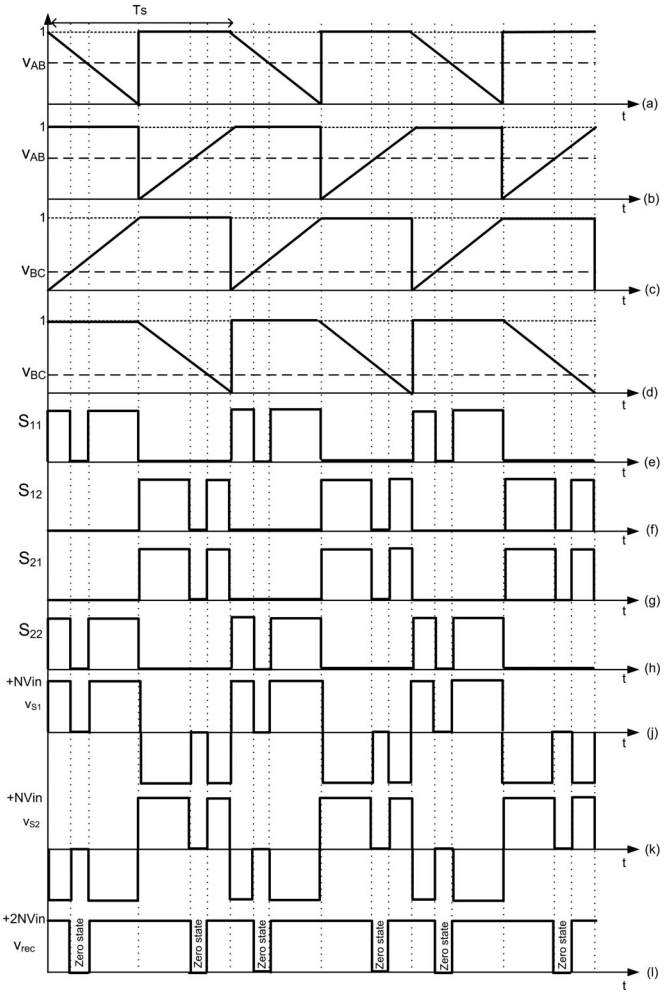

Fig. 3. Pulse placement on the PDCL using the dc/ac converter to provide zero states: (a)–(d) the HF carriers and references of the full-bridge modules of the dc/ac converter to generate bipolar pulses for HF transformers, (e)–(h) the synthesized gate signals of S_{11}, S_{21}, S_{21}, and S_{22}, (j)–(k) the secondary voltages of the HF transformer, and (l) the generated PDCL waveform.

Finally, the pulsating-dc/ac converter generates the LF output sine-waves using the pulses on the PDCL waveform. Therefore, the PDCL waveform is synthesized by the dc/ac converter and the pulsating-dc/ac converter uses the synthesized pulses on the PDCL waveform to generate LF output sine-wave pulses. The soft-switched HM scheme decreases the switching losses

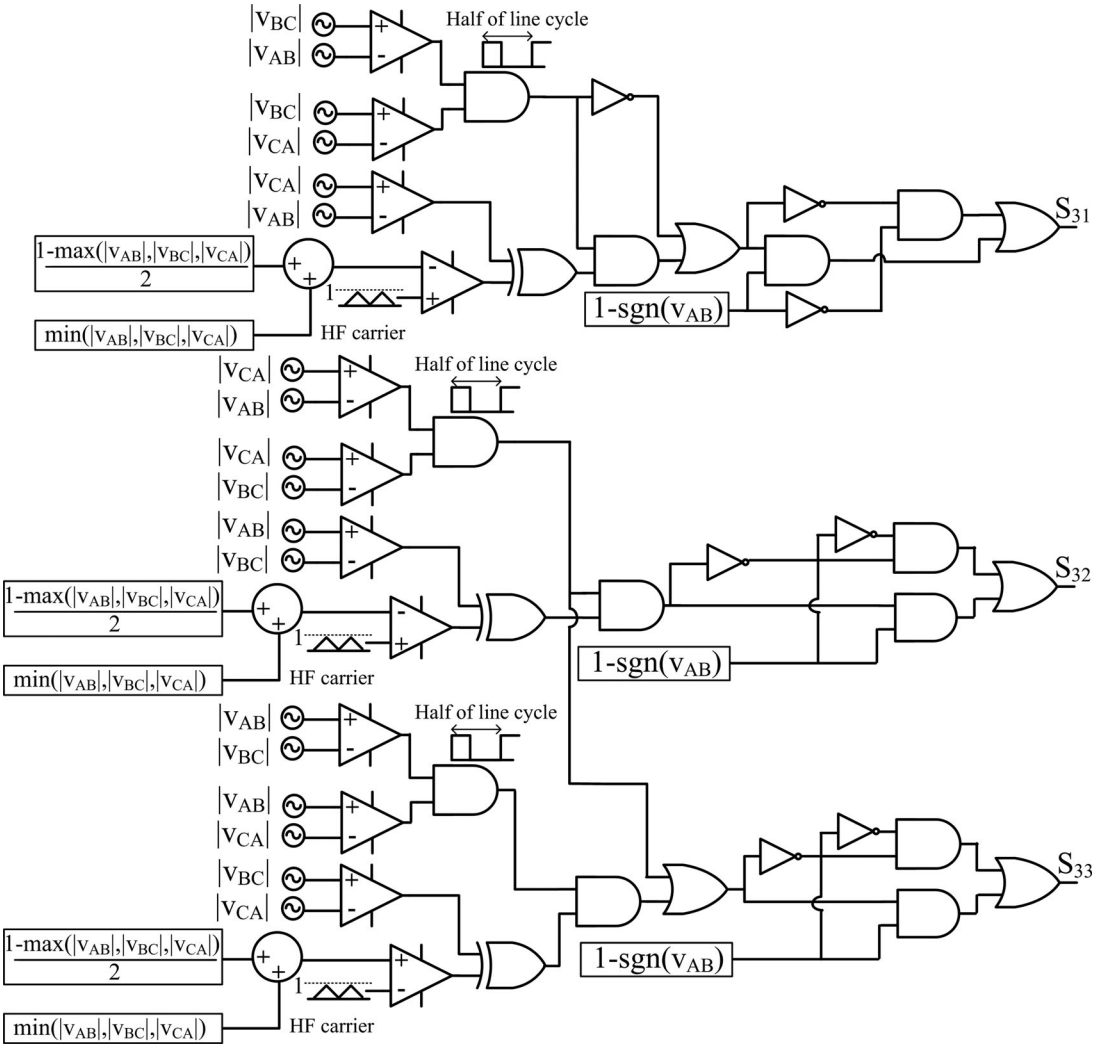

Fig. 4. Switching signals generation for the pulsating-dc/ac converter.

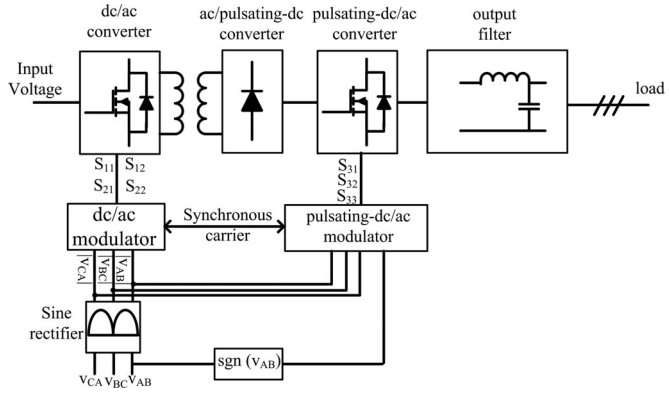

Fig. 5. Simplified operation overview of the PDCL HF inverter using the soft-switched HM.

of the pulsating-dc/ac converter by decreasing the switching requirement and ZVS operation of the pulsating–dc/ac converter. This section explains the modulation scheme to synthesize the PDCL waveform, then; the soft-switched HM for pulsating-dc/ac converter to yield the desired LF output sine-waves.

A. Synthesis of the PDCL Waveform

The dc/ac converter generates two sets of bipolar pulses for the HF transformers to avoid core saturation. The PDCL HF inverter has two full-bridge modules operating as a dc/ac converter. The first full-bridge module includes $S_{11}, \bar{S}_{11}, S_{12}$, and $\bar{S}_{12}$. The second full-bridge module (using modulator II) includes $S_{21}, \bar{S}_{21}, S_{22}$, and $\bar{S}_{22}$. Each full-bridge module generates a set of bipolar pulses for a HF transformer. Two switches of each leg operate complementary and a proper dead-time is considered to avoid short-circuit of the input dc bus. Fig. 2 shows the modulation scheme for switching signal generation of the dc/ac converter. A set of normalized three-phase sine-wave references are defined as (1)

$$\begin{aligned} v_{AB} &= m * \sin(\omega t) \\ v_{BC} &= m * \sin\left(\omega t + \frac{2\pi}{3}\right) \\ v_{CA} &= m * \sin\left(\omega t + \frac{4\pi}{3}\right) \end{aligned} \tag{1}$$

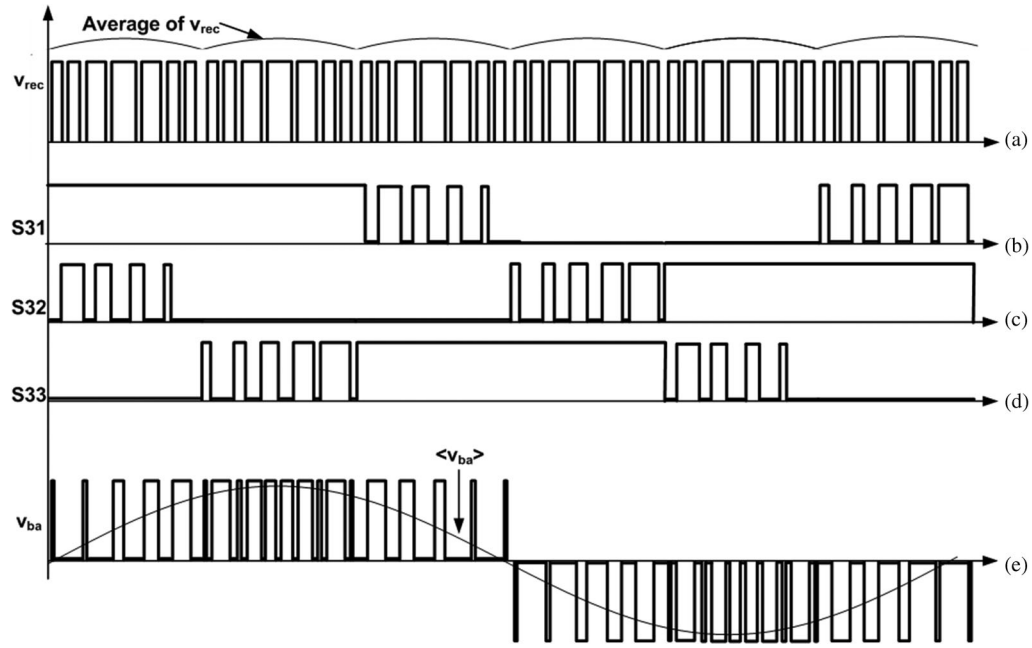

Fig. 6. Switching functions and waveforms of the soft-switched HM pulsating-dc/ac converter: (a) PDCL, (b)–(d) gate signals of pulsating-dc/ac converter switches, and (e) resulting phase-to-phase voltage before and after the output filters.

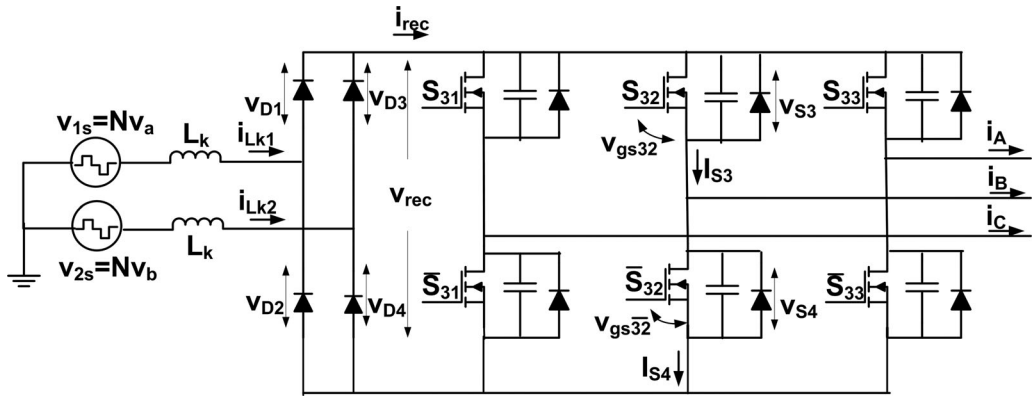

Fig. 7. Equivalent circuit of the ac/pulsating-dc converter, HF transformers, and the front-end pulsating-dc/ac converter to study topological modes of operation.

where m is modulation index and ω is output line angular frequency of the LF output sine-waves. We also obtain the following relationships for a balanced system:

$$\begin{aligned} v_{ij} + v_{jk} + v_{ki} &= 0 \\ v_{ij} &= -\left(v_{jk} + v_{ki}\right) \end{aligned} \tag{2}$$

where $i, j, k \underbrace{\in}_{i \neq j \neq k} \{A, B, C\}$. One can conclude

$$v_{ij} = |v_{jk} + v_{ki}|\,. \tag{3}$$

Then, following equation are obtained for different 60° sectors of the output line cycle:

$$|v_{CA}| = |v_{AB}| + |v_{BC}| \quad 0 < \omega t < \frac{\pi}{3} \text{ or for } \pi < \omega t < \frac{4\pi}{3} \tag{4}$$

$$|v_{AB}| = |v_{BC}| + |v_{CA}| \quad \frac{\pi}{3} < \omega t < \frac{2\pi}{3} \text{ or for } \frac{4\pi}{3} < \omega t < \frac{5\pi}{3} \tag{5}$$

$$|v_{BC}| = |v_{CA}| + |v_{AB}| \quad \frac{2\pi}{3} < \omega t < \pi \text{ or for } \frac{5\pi}{3} < \omega t < 2\pi. \tag{6}$$

Therefore, the PDCL waveform is required to be compartmentalized in six distinct sectors; that is PI: 0–60°, PII: 60°–120°, PIII: 120°–180°, PIV: 180°–240°, PV: 240°–300°, and PVI: 300°–360°. During each sector, the dc/ac converter generates two sets of pulses representing the rectified signals v_{AB}, v_{BC}, and v_{CA}. In each sector, the nonmaximum voltage reference signal is synthesized by two pulses representing two other nonmaximum reference signals as shown in (4)–(6). Therefore, the voltage reference signals of the dc/ac modulator change in every

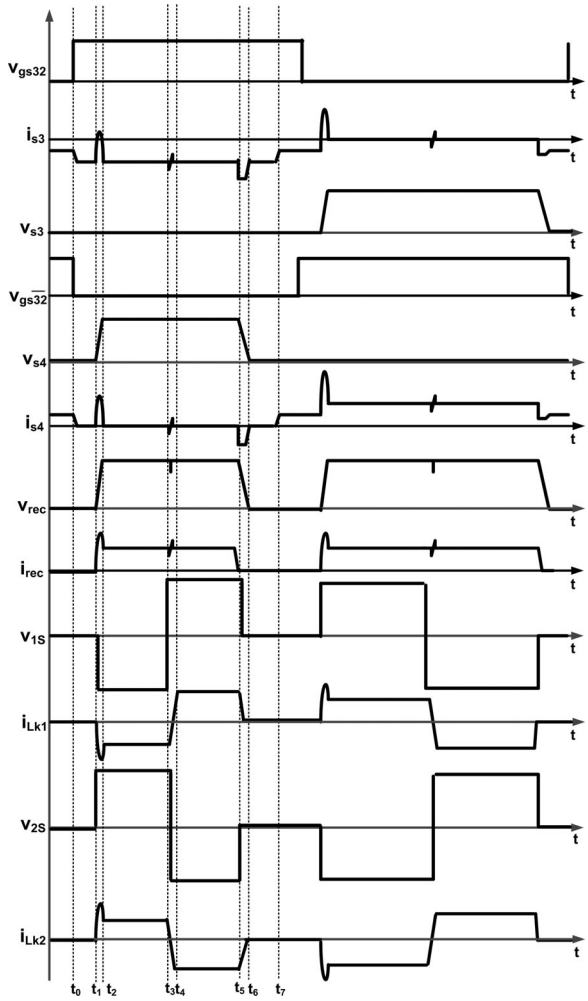

Fig. 8. Key waveforms of the equivalent circuit shown in Fig. 7 to study the soft-switching operation of the pulsating-dc/ac converter.

60° of the line cycle. In sectors PI and PIV, $|v_{CA}|$ is synthesized on the PDCL waveform using two sets of pulses synthesized by $|v_{AB}|$ and $|v_{BC}|$ as the voltage reference signals. These two sets of pulses are generated by the two-full-bridge modules of the dc/ac converter. In sectors PII and PV, $|v_{AB}|$ is synthesized on the PDCL waveform using $|v_{BC}|$ and $|v_{CA}|$ as the voltage reference signals of the full-bridge modules of the dc/ac converter. Finally, in sectors PIII and PVI, $|v_{BC}|$ is synthesized using two sets of pulses synthesized by $|v_{AB}|$ and $|v_{CA}|$ as the voltage reference signals of the full-bridge modules of the dc/ac converter.

Equations (4)–(6) can be rewritten as

$$|v_{BC}| = \max(|v_{AB}|, |v_{BC}|, |v_{CA}|) - \min(|v_{AB}|, |v_{BC}|, |v_{CA}|) \quad 0 < \omega t < \frac{\pi}{6} \text{ or for } \frac{\pi}{2} < \omega t < \frac{2\pi}{3} \tag{7}$$

$$|v_{CA}| = \max(|v_{AB}|, |v_{BC}|, |v_{CA}|) - \min(|v_{AB}|, |v_{BC}|, |v_{CA}|) \quad \frac{\pi}{3} < \omega t < \frac{\pi}{2} \text{ or for } \frac{5\pi}{6} < \omega t < \pi \tag{8}$$

$$|v_{AB}| = \max(|v_{AB}|, |v_{BC}|, |v_{CA}|) - \min(|v_{AB}|, |v_{BC}|, |v_{CA}|) \quad \frac{\pi}{6} < \omega t < \frac{\pi}{3} \text{ or for } \frac{2\pi}{3} < \omega t < \frac{5\pi}{6}. \tag{9}$$

Using (7)–(9), Modulator I of the dc/ac modulator can be implemented using the maximum and minimum signals of $|v_{AB}|$, $|v_{BC}|$, and $|v_{CA}|$. This approach makes the implementation of the dc/ac modulator just based on the maximum and minimum function of the voltage reference signals.

For example, when ωt is between 0 and π/6, $|v_{CA}|$ is the maximum of the rectified signals v_{AB}, v_{BC}, and v_{CA} and $|v_{AB}|$ is the minimum of the rectified signals v_{AB}, v_{BC}, and v_{CA}. Therefore, the voltage reference signal of Modulator I is $|v_{CA}|$ minus $|v_{AB}|$, which is equal to $|v_{BC}|$. Modulator II uses $|v_{AB}|$ (the minimum reference signal) as its voltage reference signal. Therefore, a set of pulses are synthesized by $|v_{AB}|$ and the other set of the pulses are synthesized by $|v_{BC}|$ on the PDCL waveform. Then, the average of two resulting consecutive pulses on the PDCL waveform over the switching cycle is equal to $|v_{CA}|$ (the maximum reference signal). The duration of the synthesized zero states between these two sets of pulses on the PDCL waveform are calculated as follows:

$$z(t) = 1 - \max(|v_{AB}|, |v_{BC}|, |v_{CA}|). \tag{10}$$

These zero states on the PDCL waveform are used to achieve ZVS operation for the switches of the pulsating-dc/ac converter. Therefore, $|v_{AB}|$ and $|v_{BC}|$ are directly synthesized on the PDCL waveform by two full-bridge modules of the dc/ac converter. Also, $|v_{CA}|$ is indirectly synthesized on the PDCL waveform as two consecutive pulses. Therefore, all the required voltage reference signals are synthesized on the PDCL waveform. As a result, two legs of the pulsating-dc/ac converter do not switch while the other leg switches at middle of the provided zero states on the PDCL waveform to achieve ZVS condition. The soft-switched HM scheme for the pulsating-dc/ac converter is explained in the following section.

As shown in Fig. 2, the HF carrier of Modulator I has 180° phase shift with respect to the HF carrier of Modulator II of the dc/ac converter. Therefore, the dc/ac converter generates a set of bipolar pulses at the end and beginning of the switching cycle. But, it also generates a set of bipolar pulses at the middle of the switching cycle. Consequently, two sets of the generated pulses by the full-bridge modules of the dc/ac converter have 180° phase shift with respect to each other.

Fig. 3 shows the HF carriers, references, signal-waveforms of Modulator I and Modulator II of the dc/ac converter, bipolar pulses for the HF transformers, and the resulting PDCL voltage waveform. As shown in Fig. 3, two sets of pulses with 180° phase shift are generated on the PDCL waveform with enough zero states to enable ZVS condition for the pulsating-dc/ac converter. As a result, the average of two consecutive pulses on the PDCL waveform over the switching cycle is equal to the maximum of the rectified signals v_{AB}, v_{BC}, and v_{CA}.

B. Soft-Switched Hybrid Modulation for the Pulsating-DC/AC Converter

The modulation scheme to generate the required PDCL waveform for pulsating-dc/ac converter is described in the previous section. The two sets of generated pulses by the full-bridge modules of the dc/ac converter are used to decrease the switching requirement of the pulsating-dc/ac converter. Also, the zero

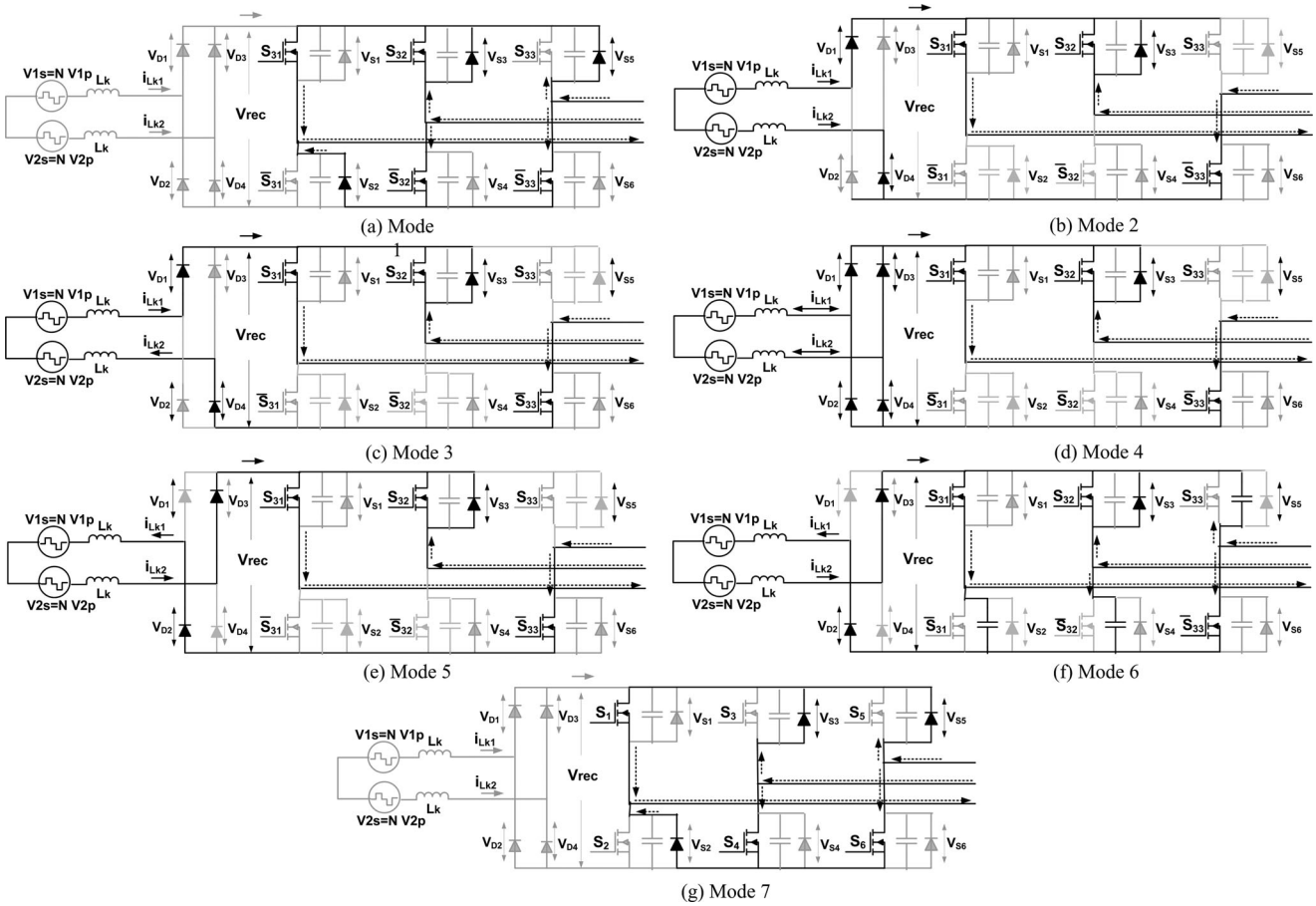

Fig. 9. Topological modes of the equivalent circuit shown in Fig. 7 to study the soft-switching operation of the pulsating-dc/ac converter.

TABLE I
SPECIFICATIONS AND MAIN COMPONENTS OF THE IMPLEMENTED PDCL HF INVERTER

Frequency	**Input voltage**	**Output phase-to-phase voltage**	**Output power**	**Transformer turns ratio**
21.6 kHz	40 V	208 V	1 kW	1:4.2
Name	**Components**			
dc/ac converter	IRF3808; MOSFET, 75 V, 140 A, 7 mΩ			
ac/pulsating-dc converter	D06S60; 600 V, 6A			
pulsating-dc/ac converter	IPW60R045CP; 650V, 60A, 45 mΩ			
transformers	Nano-crystalline core			

states on the PDCL waveform are used to provide ZVS condition for the pulsating-dc/ac converter. The modulation scheme to generate switching signals for three legs of the pulsating-dc/ac converter is shown in Fig. 4. The sign of v_{AB} (as represented by sgn(v_{AB})) is used to generate the complementary pulses for the second half of the line cycle. Each leg of the pulsating-dc/ac converter does not switch for two-thirds of the line cycle. For instance, the first leg of the pulsating-dc/ac converter operates only at HF when $|v_{BC}|$ is greater than $|v_{AB}|$ and $|v_{CA}|$. The available zero states on the PDCL waveform are calculated using (10). Therefore, the term z(t)/2 is added to the reference signals of the comparators to operate at middle of the zeros states on the PDCL waveform. As a result, the switches of the pulsating-dc/ac converter turn OFF/ON when the voltage across the PDCL waveform is zero.

Fig. 5 shows a simplified operation overview of the soft-switched HM. The dc/ac and pulsating-dc/ac modulators are respectively described in Figs. 3 and 4. A sine-wave rectifier is used to provide rectified sine-wave voltage reference signals (v_{AB}, v_{BC}, and v_{CA}) for the dc/ac and pulsating-dc/ac modulators. These modulators have synchronous carriers to achieve ZVS condition for the pulsating-dc/ac converter. The generated pulses for the pulsating-dc/ac converter are inverted when the sign of signal v_{AB} changes. Therefore, the sign of v_{AB} is provided for the pulsating-dc/ac modulator. The signals v_{AB}, v_{BC}, and v_{CA} are the output of the controller for close loop of the PDCL HF inverter.

Fig. 6 illustrates the switching scheme of the pulsating-dc/ac converter and the zero states on the PDCL over a line cycle. Fig. 6(b)–(d) shows the required gate signals to extract the

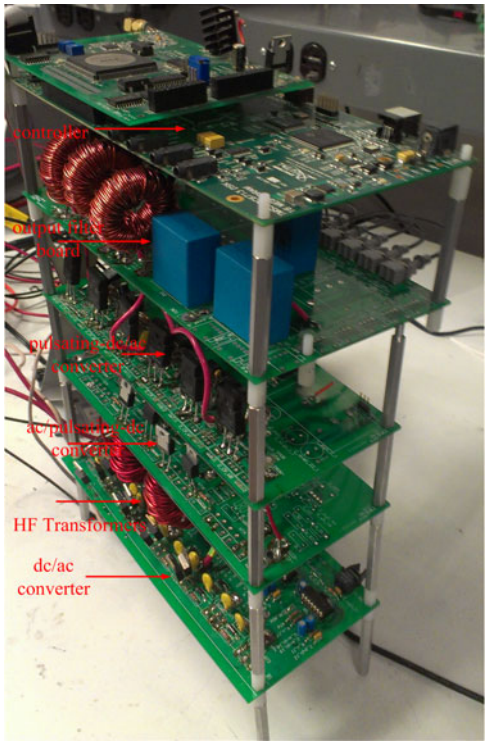

Fig. 10. Implemented prototype to validate the soft-switched hybrid modulation.

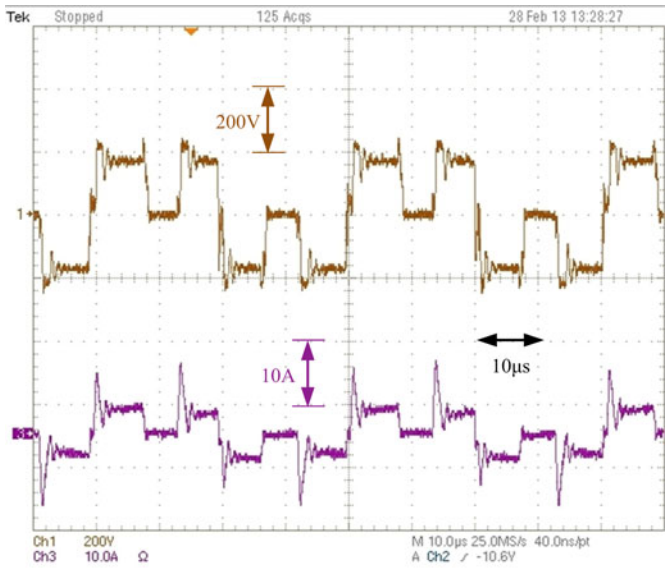

Fig. 11. Secondary-side voltage and current of a HF transformer of the PDCL HF inverter.

desired phase-to-phase output voltages using the soft-switched HM. The resulting output voltage v_{ba} is depicted in Fig. 6(e) before and after the output filter stage. Topological modes of operation are thoroughly presented in the next section.

In order to study the topological modes of operation of the PDCL HF inverter using the soft-switch HM, an equivalent circuit is derived as shown in Fig. 7. It is obtained by eliminating the HF transformers and simplifying the dc/ac converter to analyze the soft-switching operation of the soft-switched HM. The voltage supplies (v_{1s} and v_{2s}) represent the secondary reflected voltages of transformers T_1 and T_2, while the inductors are the secondary-side leakage inductances. The capacitors across the switches of the pulsating-dc/ac converter represent the parasitic capacitors of the switches.

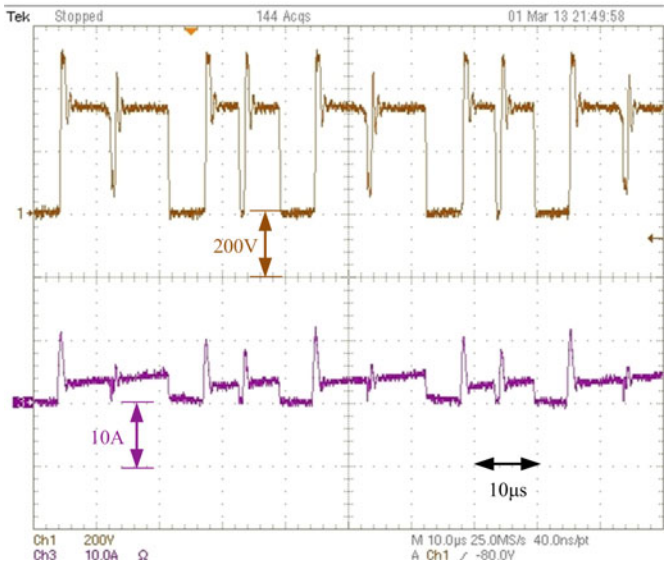

Fig. 12. PDCL voltage and current waveform of the PDCL HF inverter using the soft-switched HM. Each switching cycle contains two pulses that represent different output sine-wave reference voltage signals as explained in Section II.

III. Modes of Operation

To analyze the modes of operation, the following assumptions are made:

1) the voltage drops of the diodes and conduction losses of the switches are neglected;
2) the dead time considered for the complementary switches of the pulsating-dc/ac converter is disregarded (it should be noted that switches of the pulsating-dc/ac converter operate at zero states, therefore; no dead time is necessary for complementary switches of the converter);
3) the currents are considered to be constant during switching cycle;
4) the currents and voltages are assumed to be balanced three-phase sinusoidal waveforms; that is

$$\begin{aligned} i_A &= I_m \sin(\omega t + \gamma) \\ i_B &= I_m \sin\left(\omega t + \gamma + \frac{2\pi}{3}\right) \\ i_C &= I_m \sin\left(\omega t + \gamma + \frac{4\pi}{3}\right) \end{aligned} \tag{11}$$

where I_m is the peak value of the line output currents and γ represents the power factor of the output load, which is negative for inductive load. A PDCL HF inverter with diode rectifier supports a power factor up to 30° according to [14]. Due to symmetry, the soft-switching operation of a leg of the pulsating-dc/ac converter is analyzed, which operates at HF.

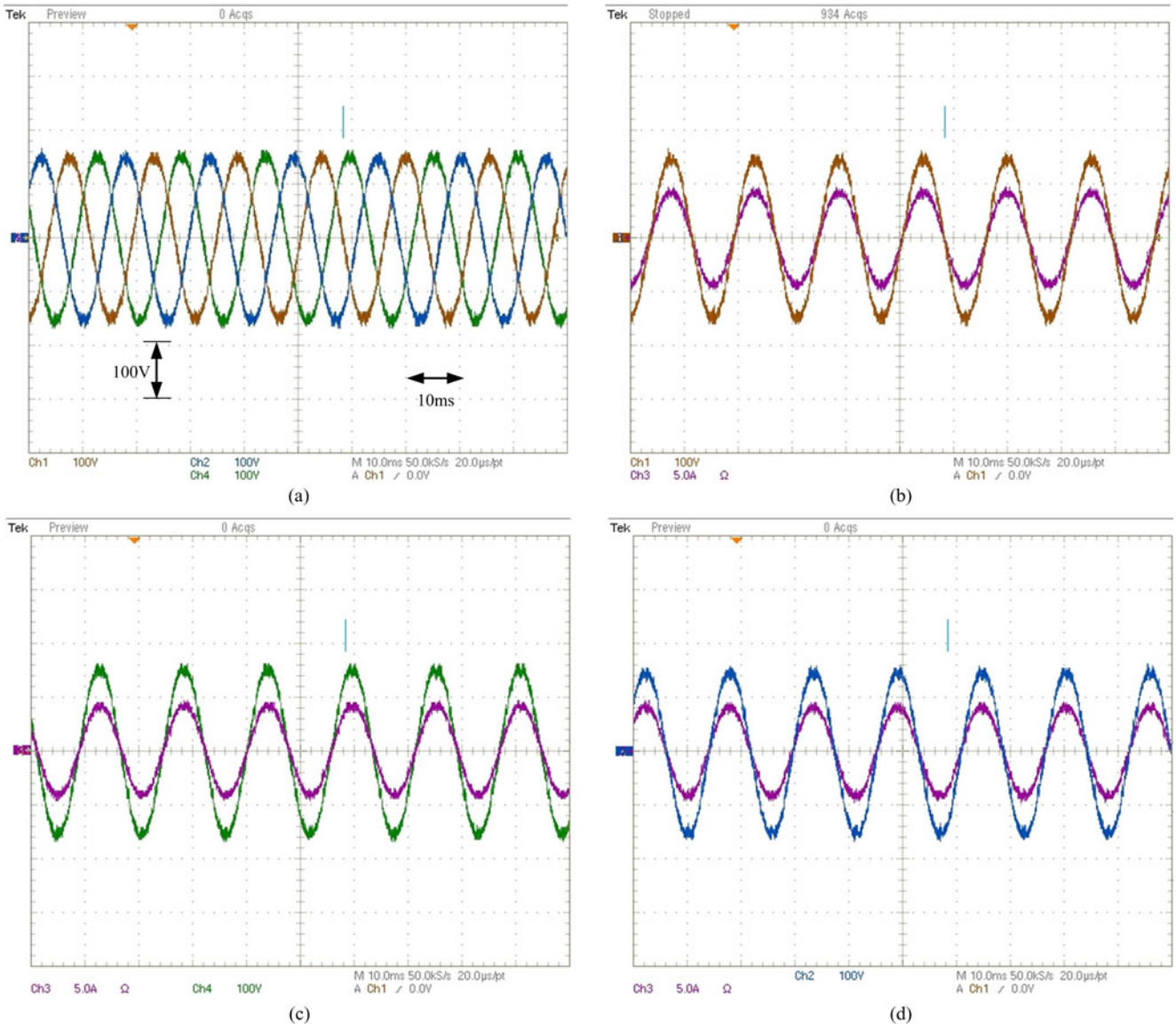

Fig. 13. Output phase voltages and currents for a 1-kW resistive load: (a) three-phase output voltage, (b) voltage and current of phase A, (c) voltage and current of phase B, and (d) voltage and current of phase C.

In this section, $|v_{CA}|$ is greater than $|v_{AB}|$ and $|v_{BC}|$ and the sign of v_{AB} is negative. Therefore, switches S_{31}, $\bar{S}_{31}$, S_{33}, and $\bar{S}_{33}$ do not switch. However, the second leg of the pulsating-dc/ac converter consisting of S_{32} and $\bar{S}_{32}$ operates at HF. Currents i_A and i_C are positive, but i_B is negative. The topological modes of operation and the key waveforms are respectively shown in Figs. 8 and 9.

Mode 1 ($t_0 < t < t_1$): Before t_0,S_{32} is OFF and i_B is shared between $\bar{S}_{32}$ and the body diode of S_{32}. Therefore, all the diodes of the ac/pulsating-dc converter are OFF and the currents freewheel in the legs of the pulsating-dc/ac converter. Therefore, the PDCL voltage $v_{\rm rec}$ and current $i_{\rm rec}$ are zero. Hence, the second leg (S_{32} and $\bar{S}_{32}$) is switched under ZVS turn-on/off condition. This mode ends when $v_{\rm rec}$ starts to rise from zero.

Mode 2 ($t_1 < t < t_2$): At $t = t_1$, the voltage of the PDCL waveform starts to rise from zero. Before this instant, the voltage across parasitic capacitors of the switches is zero. Thus, D_1 and D_4 start to conduct to supply the required current for charging the parasitic capacitors of $\bar{S}_{31}$, $\bar{S}_{32}$, and S_{33}.

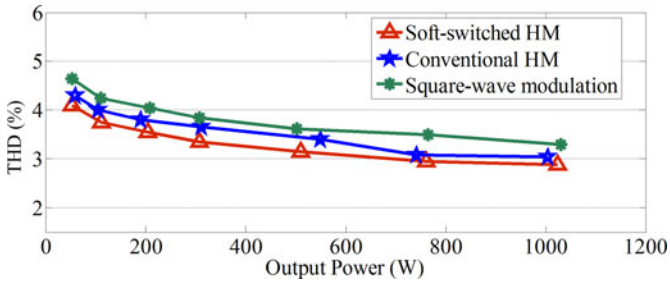

Fig. 14. Output current THD versus output power of the inverter.

Voltage supplies v_{1s} and v_{2s} are respectively equal to $-NV_{\rm in}$ and $+NV_{\rm in}$. The current i_A is positive and S_{31} is ON. Consequently, the required current to charge the parasitic capacitor of

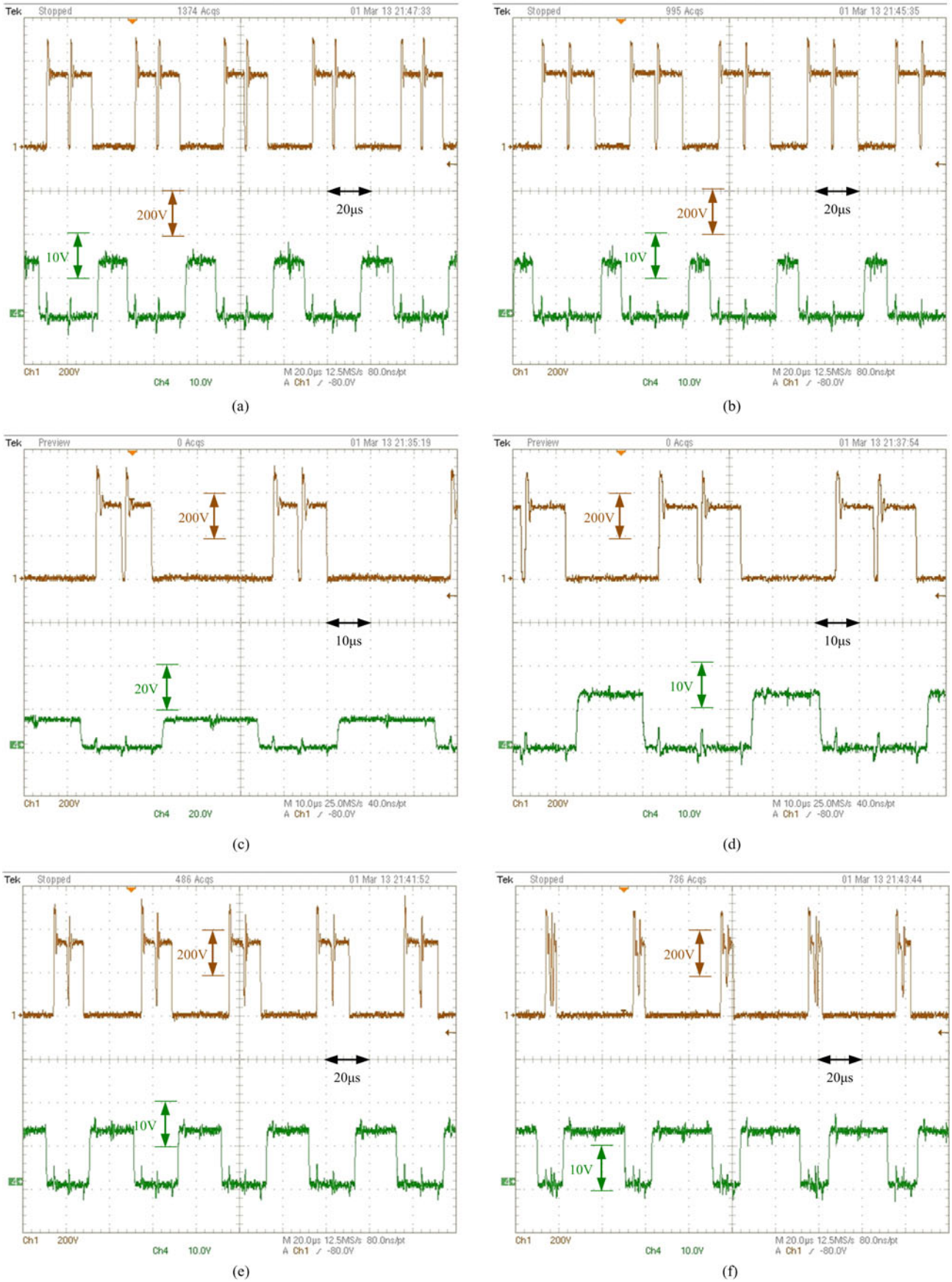

Fig. 15. Soft-switching operation of all switches of the pulsating-dc/ac converter: (a) S_{31}, (b) $\bar{S}_{31}$,(c) S_{32}, (d) $\bar{S}_{32}$, (e) S_{33}, and (f) $\bar{S}_{33}$ (Ch1: drain-to-source voltage, and CH4: gate voltage).

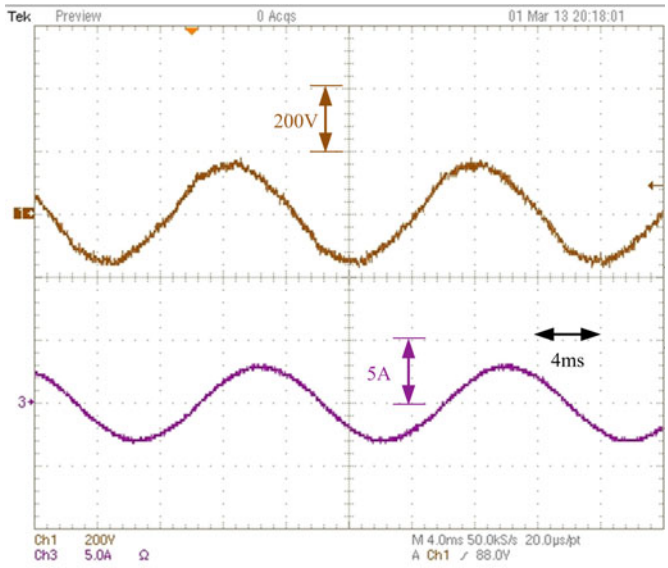

Fig. 16. Output phase voltage and current of a phase of the PDCL HF inverter when it supplies an induction motor.

$\bar{S}_{31}$ is supplied by a path through S_{31}. The voltage across the parasitic capacitors is calculated as follows:

$$v_{s2} = v_{s4} = v_{s5} = v_c$$
$$2\mathrm{NV_{in}} = 2L_k \frac{di_{Lk2}}{dt} + v_c$$
$$i_{c2} = i_{c4} = i_{c5} = C\frac{dv_c}{dt}. \tag{12}$$

We can rewrite (10) as follows:

$$2\mathrm{NV_{in}} = 2L_k C\frac{d^2 v_c}{dt^2} + v_c. \tag{13}$$

According to (12), the resonant paths between the parasitic capacitors and the leakage inductances of the HF transformers build up the voltage of $\bar{S}_{31}, \bar{S}_{32}$, and S_{33}. This mode ends at $t = t_2$ when the voltage of the parasitic capacitors reaches their final value, which is equal to $2\mathrm{NV_{in}}$.

Mode 3 ($t_2 < t < t_3$): At the beginning of this mode, the PDCL voltage waveform reached its final value. The currents are supplied by the PDCL. The current of the leakage inductances remains constant because their voltages are zero. At the end of this mode, v_{1S} and v_{2S} change their polarity.

Mode 4 ($t_3 < t < t_4$): In this mode, v_{1s} and v_{2s} are constant and respectively equal to $\mathrm{NV_{in}}$ and $-\mathrm{NV_{in}}$. There are two commutations in the ac/pulsating-dc converter to change the current directions of the leakage inductances. As a result, D_1 commutes with D_2 and D_3 takes over the current of D_4. The commutation times of the diodes are neglected here. Therefore, all the diodes conduct in this mode of operation. The leakage currents are taken over by D_3 and D_2 at the end of this mode. Therefore, the leakage inductance currents are equal and calculated as

$$2L_k \frac{di_{Lk1}}{dt} = +2\mathrm{NV_{in}}$$
$$i_{Lk1}(t) = i_{Lk1(t_3)} + \frac{\mathrm{NV_{in}}}{L_k}(t - t_3). \tag{14}$$

Finally, the currents of leakage inductance are equal to the PDCL current.

Mode 5 ($t_4 < t < t_5$): This mode of operation starts when the currents of leakage inductances reached their final value to support the balanced output currents. Similar to Mode 3, the voltages across the leakage inductances are zero, consequently; the leakage currents are constant. At the end of this mode, v_{1s} and v_{2s} become zero and the leakage currents start to decrease.

Mode 6 ($t_5 < t < t_6$): The PDCL voltage waveform tends to decrease, because the secondary winding voltages are zero. As a result, the body capacitors of $\bar{S}_{31}, \bar{S}_{32}$, and S_{33} are being discharged by output load currents. This mode ends when the leakage currents become zero and load currents start to freewheel again in the pulsating-dc/ac converter. In this mode of operation, S_{32} turns OFF under zero voltage turn-off condition because the voltage of the PDCL waveform is zero.

Mode 7 ($t_6 < t < t_7$): $\bar{S}_{32}$ is OFF and i_B must pass through the S_{32} and its body diode. $\bar{S}_{32}$ turns ON under zero-voltage turn-on condition. Similar to Mode 1, the load current shares between S_{32} and $\bar{S}_{32}$. Therefore, the load currents again freewheel in the pulsating-dc/ac converter. The ZVS operation of the other switches has the same principle of operation during other operation conditions.

IV. Experimental Results

The specifications and main components of the implemented PDCL HF inverter for validating the operation of the soft-switched HM scheme are summarized in Table I. Fig. 10 shows the implemented prototype of the PDCL HF inverter to validate the soft-switched HM. The output filter capacitors and inductors are respectively 5 μF and 1 mH. The secondary-side voltage and current of a HF transformer of the PDCL HF inverter are shown in Fig. 11. The secondary-side voltage waveforms of the HF transformers are rectified by the ac/pulsating-dc converter to generate the PDCL waveform. The Fig. 12 shows the resulting PDCL waveform using the explained modulation scheme in Section II for the dc/ac converter. The resulting zero states on the PDCL waveform provide ZVS turn-on/off condition for the pulsating-dc/ac converter. These two pulses with different widths are related to different output sine-wave reference voltage signals.

Fig. 13(a) shows the three-phase output sine-wave voltages using soft-switched HM modulation for a 1 kW resistive load. The respective output phase voltages and currents of the PDCL HF inverter are shown in Figs. 13(b)–(d). The THD of the HF PDCL inverter for the soft-switched HM, the conventional HM, and square-wave modulation is shown in Fig. 14. The soft-switched HM shows a more promising THD because of soft-switching of the pulsating-dc/ac converter. The resulting THD of the PDCL HF inverter is well below 5% for a wide range of the output powers for the soft-switched HM.

The ZVS soft-switching operation of the pulsating-dc/ac converter is shown in Fig. 15. All of the switches turn ON/OFF in the zero states available on the PDCL voltage waveform. The ZVS operation and performance of the PDCL HF inverter using soft-switched HM scheme is evaluated when the inverter

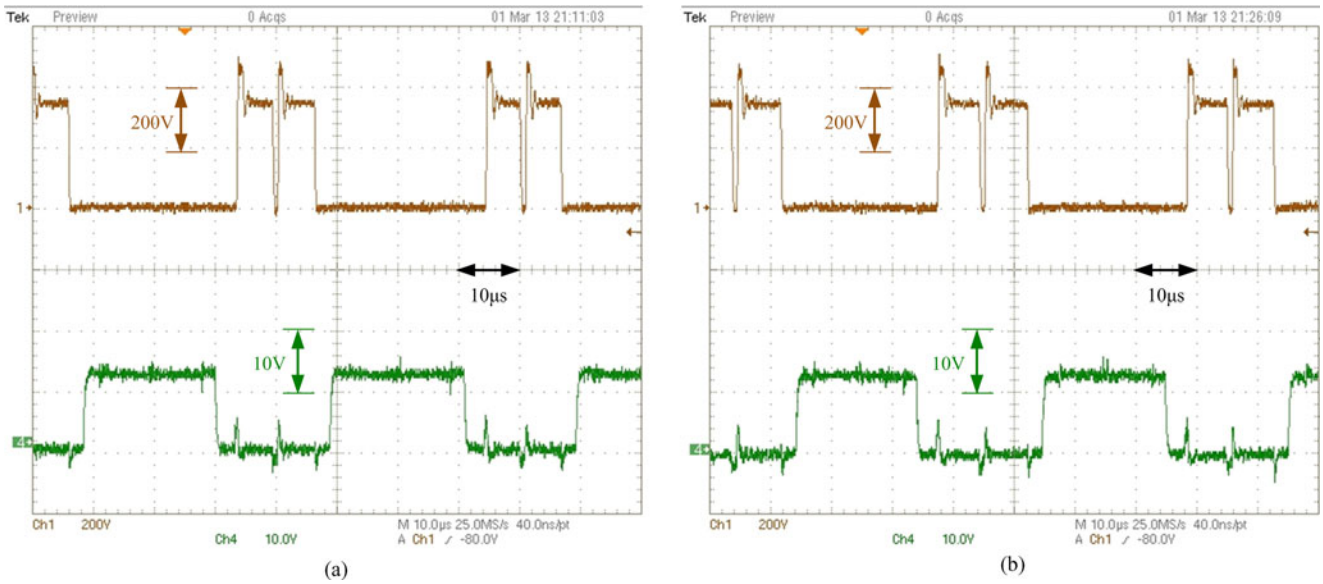

Fig. 17. Soft-switching operation of the first leg of the pulsating-dc/ac converter when it supplies an induction load: (a) S_{31}, (b) $\bar{S}_{31}$ (Ch1: drain to source voltage, and CH4: gate voltage).

supplies an induction motor. The power factor of the motor is about 30°. The obtained output voltage and current of a phase of the PDCL HF inverter is shown in Fig. 16. The THD of the output voltage of the inverter is 4.7% for this inductive load. Fig. 17 shows the ZVS operation of the PDCL HF inverter for the first leg of the pulsating-dc/ac converter when the PDCL HF inverter supplies the induction motor. A three-phase diode rectifier is used as a nonlinear load for the implemented PDCL HF inverter. Fig 18 shows the output voltage and current waveforms of the inverter when it supplies a nonlinear load. The THD of the output voltage is 4.85% when the output power is 1 kW. The soft-switching operation of the inverter for the first leg of the inverter is shown in Fig. 19.

The efficiency of the soft-switched HM scheme, the conventional HM, and the square-wave modulation scheme in [9] for PDCL HF inverters are compared using the implemented inverter. The achieved efficiencies for the PDCL HF inverter using the mentioned schemes are shown in Fig. 20. The efficiency of the pulsating-dc/ac converter is increased using the soft-switched HM compared to other modulation schemes. The efficiency of the three stage of the PDCL HF inverter is depicted in Fig. 21. The conduction loss of the dc/ac converter is dominant because of high current rating of the front-end stage. However, the ac/pulsating-dc and pulsating-dc/ac converters have considerably lower conduction loss. Therefore, switching loss is dominant at the stages after the secondaryside of the HF transformers. European weighted efficiency and The California Energy Commission (CEC) weighted efficiencies are calculated and recorded in Figs. 21 and 22.

The operation of the soft-switched HM is reviewed for the light load conditions. As explained in Section III, load currents charge and discharge the parasitic capacitors of the switches of the pulsating-dc/ac converter. Therefore, enough load currents is required to provide the zero states for the ZVS operation of

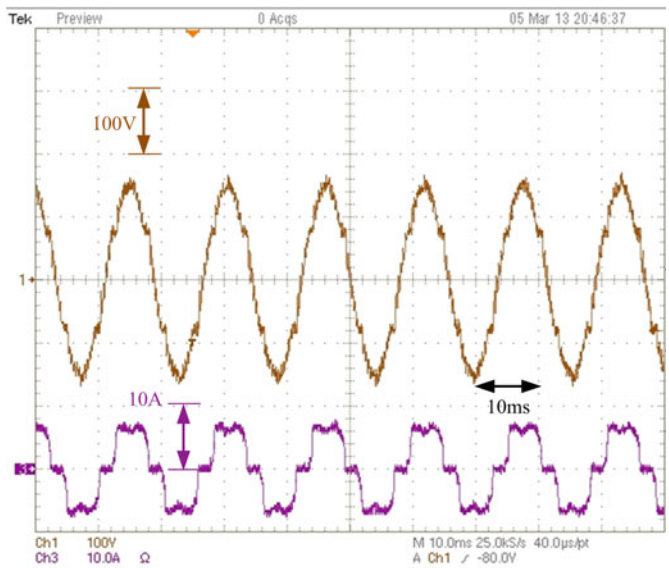

Fig. 18. Output voltage and current of a phase of the PDCL HF inverter when it supplies a nonlinear load.

the pulsating-dc/ac converter. Fig. 22 shows the soft-switching operation of switch S_{31} when the output power is 50 W. Because parasitic capacitors of the switches are typically small (320 pF for IPW60R045CP MosFets), enough zero states are generated on the PDCL waveform. Therefore, the soft switching is achieved for light load although it takes more time to discharge the parasitic capacitors. The Fig. 23 shows the drain–source voltage and the gate signal of switch S_{31} when the output power is 40 W. The ZVS operation is lost due to lack of enough load currents. But, the switch still commutate at lower voltages compared to the conventional HM.

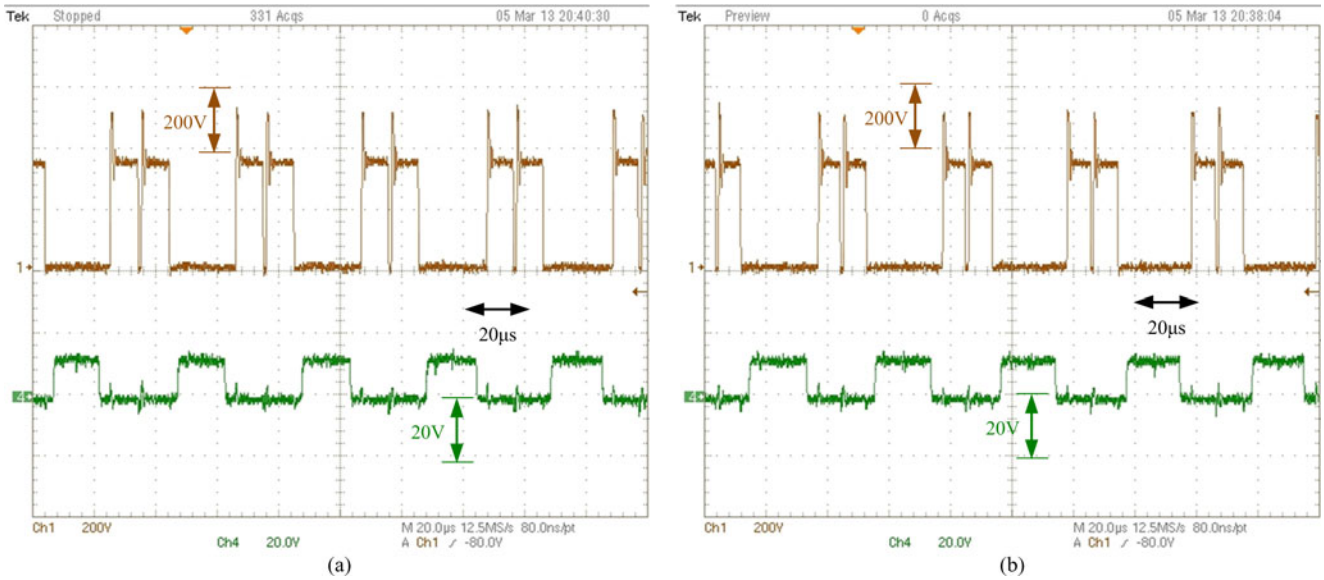

Fig. 19. Soft-switching operation of the first leg of the pulsating-dc/ac converter when it supplies a nonlinear load: (a) S_{31}, (b) $\bar{S}_{31}$ (Ch1: drain to source voltage, and CH4: gate voltage).

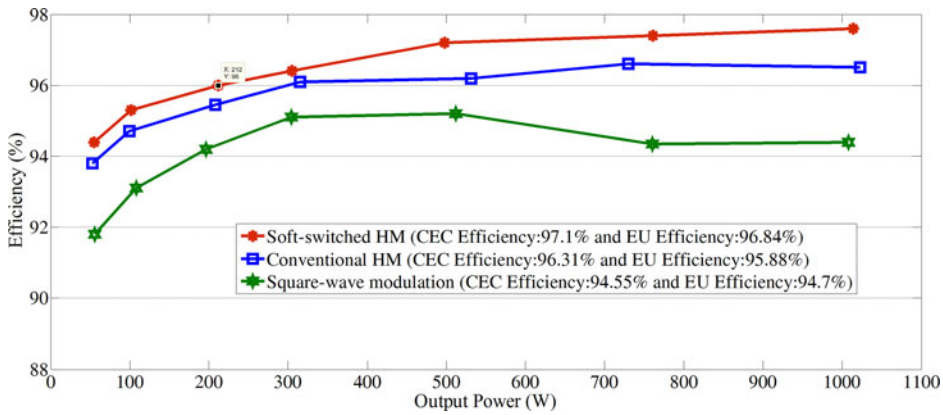

Fig. 20. Efficiency of the pulsating-dc/ac converter.

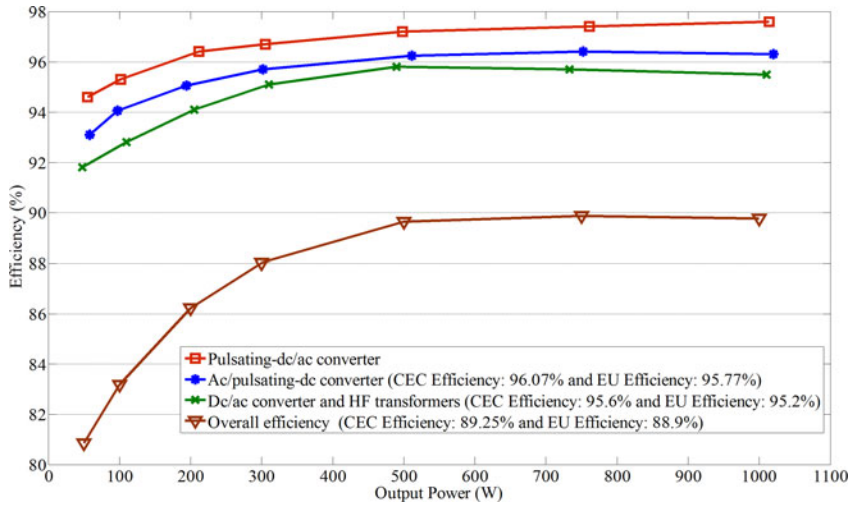

Fig. 21. Efficiency of the different stages of the PDCL HF inverter.

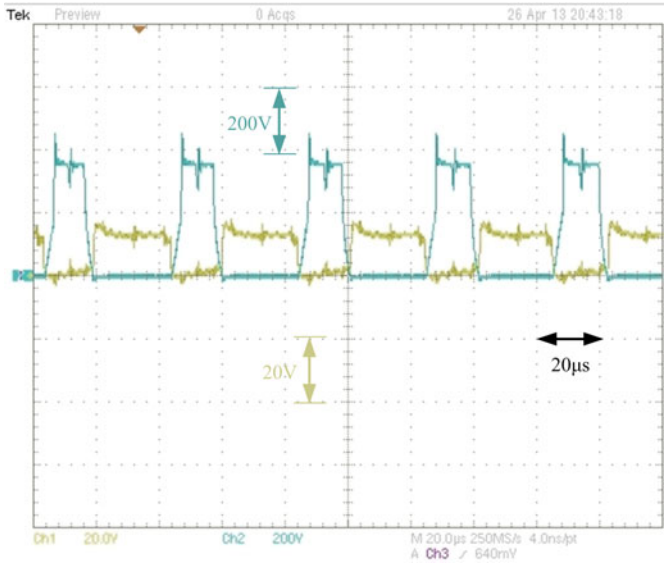

Fig. 22. Soft-switching operation of S_{31}.

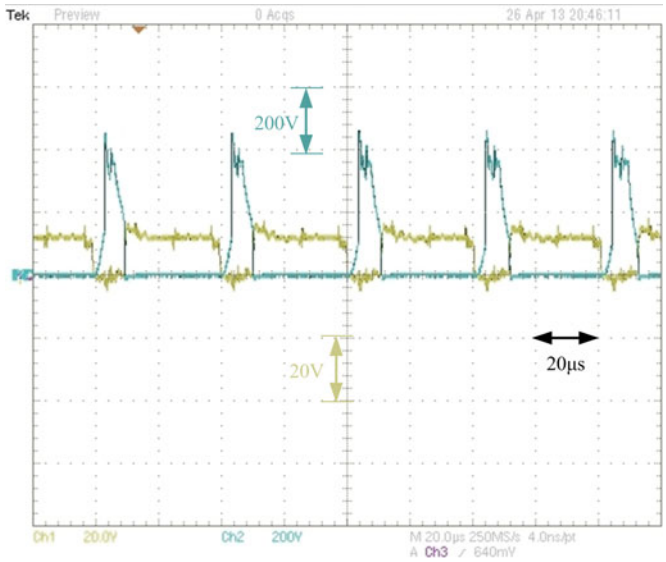

Fig. 23. Operation of the S_{31} when the output power is 40 W.

V. Conclusion

Lossless mitigation of the pulsating-dc/ac converter is achieved using the soft-switched hybrid modulation due to switching transition during the zero states. The pulsating-dc link waveform has two different phase-to-phase representations that lead to soft-switching operation of the pulsating-dc/ac converter. The soft-switching operation of the pulsating-dc/ac converter can be extended to the ac/pulsating-dc converter when full controlled switches are used for the ac/pulsating-dc converter. The soft-switching operation of the pulsating-dc/ac converter is independent of the load type. Its operation is validated for resistive, inductive, and nonlinear loads.

VI. Disclaimer

The hybrid modulation mechanism outlined in this paper is covered by the following patent:

S.K. Mazumder and R. Huang, "Multiphase converter apparatus and method," USPTO Patent# 7,768,800 B2, awarded on August 3, 2010.

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