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Switching Transition Control to Improve Efficiency of a DC/DC Power Electronic System

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ABSTRACT Increasing the switching frequency of the power semiconductor devices (PSDs) reduces the size and cost of the passive elements, thereby positively affecting the power density of a high-frequency (HF) power electronic system (PES). To achieve a higher switching frequency of a PES, yet low switching losses, the speed of switching transitions of PSDs need to be increased. However, such fast transitions adversely affect PES performance in terms of electromagnetic interference (EMI) and device stress. Hence, a switching transition control (STC) scheme is developed to create optimality between switching PSDs with higher transitions yet maintaining safe levels of parasitic oscillations, that result from reducing the transition time of these devices. The switching transition control (STC) framework helps the HF PES achieve a target efficiency improvement by controlling the high di/dt and dv/dt regions of a PSD on the fly. Results are shown to validate that this improvement of efficiency is not feasible with a passive gate drive. An HF Cuk PES using a Cree SiC MOSFET half-bridge module is fabricated for the testing purpose of the STC framework. The STC network is based on a simple switched resistor network, synthesized using high-speed GaN-FETs and built across two generations, Gen-1, and Gen-2. Practical operational issues of the STC network with fast switching GaN-FET in the Gen-1 board are analyzed and are overcome with design modification in Gen-2. The work has ramifications in meeting a system-level goal of an HF WBG PES, like a target efficiency increment, while not deteriorating the EMI performance and PSD stress levels that result due to parasitic oscillations in such PES.

INDEX TERMS Switching transition control (STC), PSD, EMI, half-bridge, GaN FET, target efficiency.

I. INTRODUCTION

To reduce PES losses while increasing power densities (by increasing switching frequencies), the switching transitions of the PSDs need to be significantly improved as is evident from the recently used WBG PSDs like GaN-FETs and SiC FETs [1]–[7]. These new-generation devices facilitate miniature chip design leading to small parasitic capacitances. This enables higher frequency operation at increased power. However, increasing the switching transitions of these new generation devices to decrease the switching losses using fixed gate drive results in non-optimal performance resulting in excessive device stress and electro-magnetic interference (EMI). As an illustrative example, if we consider SiC FET

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based high power half-bridge modules [8] that are fabricated to aid higher frequency operation at higher power ratings, reducing the on-time resistance of the low-side FET to reduce switching losses, results in reverse recovery induced oscillations [9] due to the body diode of the high-side FET.

So, instead of reduced switching losses, these oscillations increase the V-I overlap at the turn-on switching transition even further, resulting in decreased PES efficiency. Over and above, these oscillations lead to unstable PES gate drive operation, which does not let the PES operate across a wide operating range. In such HF PES, where there is a need of optimality between switching losses (by using lower gate resistances) and device stress/ oscillations (that results due to the use of lower gate resistances), a switching transition control scheme, as shown in Figure 1, can be synthesized. Depending on a particular topology and an online operating



FIGURE 1. Figure showing how STC scheme can meet system-level goals for an HF PES. t_r and t_f are the rise and fall times of the devices.

point, with the device physics under consideration, it can create rise and fall times of the devices (t_r and t_f , respectively) of the HF PES to meet a specific goal (η) for the topology. The specific goal (η) can range from efficiency increment to common mode EMI reduction for the PES.

Passive gate circuits cannot achieve this feat. They use fixed gate resistances which decrease transition times at the cost of increased power loop and gate loop oscillations and hence, optimized switching performance is not achievable over wide power levels. Active and passive snubbers, as well as active clamp circuits, are then used to reach optimality between switching loss EMI and device stress of a PES [3], [10]. This introduces additional components in the power stage in form of semiconductor switches, and passive elements which add to the PES losses. Also, the snubber values are difficult to optimize, and a desirable trade-off is seldom obtained.

A good strategy in attaining a tradeoff is to design an active gate drive that controls the switching transitions of a PES. The STC scheme in Figure 1 uses such an active gate drive. Active gate circuits were first used to dynamically adjust the turn-on/turn-off transition of slower transition IGBTs [2], [11], [12] for the series connection of such devices. It helped replace the conventional voltage-sharing snubbers, as well as reduce switching losses while maintaining admissible voltage/current stresses of the devices. References [12]–[17] extend the use of active gate drive circuits for WBG SiC MOSFET applications. The literature [13], [15] propose switched resistor-based gate drive modulation to improve the current and voltage transitions of SiC PSDs and achieve controllability and performance optimization in terms of EMI and switching losses. However, both the references encompass limited transitions of the switched resistor network, resulting in lower flexibility to affect different regions of the switching transition in a single turn on/turn-off event. Moreover, the switched resistor-based gate drive synthesis is not touched upon in detail in the abovementioned literature. Also, reference [15] uses the switched resistor approach to decrease turn-off losses only of the SiC FET, while during turn-on, EMI issues and device stress due to body-diode reverse recovery is focused upon. Contrary to [13], [15], references [14], [16] could achieve higher granularity in active gate voltage control using an advanced mixed-signal design approach. But the approach suffers from higher complexity compared to [13], [15], and the design parameters are not easy to replicate. Also, [14][16] does not consider WBG SiC devices with strong diode reverse recovery effects. References [17], [18] talk about controlling the switching transitions of optically triggered devices. Although the references give some thoughtful insights on resolving practical challenges encountered with optical device active gating, the complex analog based techniques used reduce design flexibility.

Recently, active gate circuits are used for high-speed GaN-FETs with less than 10 *ns* switching transients [19] which is one of the most impressive work in the field of active gate control. Although the gate driver altered multiple drive parameters per switching event, however, the gate current peaks are significantly less than that needed for SiC MOSFETs having large gate to source capacitances. Thus, it needs to be seen whether the techniques used in [19] to achieve high granularity of active gate drive are scalable to the applications in [15]. Also, [19] fabricated an integrated ASIC which is understandable since the switching transition of GaN-FETs is very fast. The complexity of the approach, and the need of an ASIC to realize active gate control, may preclude the approach in low-cost industrial applications.

Another important point is that most of the abovementioned literature studies the active gate control using a double pulse test set-up, thus creating a cause/effect relationship mainly. How these schemes can be extended to improve converter level performance, or meet a system-level goal, as shown in Figure 1 concerning a converter, is not clearly studied.

Contrary to the prevalent approaches, which either use complicated mixed-signal schemes or performs a less granular operation, this manuscript delineates a switching transition control (STC) framework using a simple switched resistive based active gate drive. Depending on modes of operation (CCM/DCM) of a Cuk WBG PES set-up using Cree SiC MOSFET half-bridge module (having high input capacitance that results in higher peak gate currents), the STC network shapes the turn-on/turn-off of the HF PES using an online processor. It does so to help the PES achieve target efficiency increment across wide operating conditions while precluding excessive device stress. The approach is scalable/replicable because it uses a switched resistor scheme for the STC circuit. It is the simplest form of active gate drive. Contrary to approaches in [13], [15] which requires multiple gate resistors in the switched resistor drive to achieve granularity, the proposed approach makes use of a single resistor with an HF GaN switch in parallel. The pulses to the GaN device are selected to create an averaged gate resistance



FIGURE 2. Figure showing the difference between conventional [13], [15] vs modified switched resistor-based gate drive approach.

during a transition event. The conventional [13], [15] vs proposed approach is compared in Figure 2 and detailed more in [20]. Recently accepted [20] describes succinctly how the approach dramatically reduces the gate footprint and complexity of the drive, along with describing the basic approach of the STC scheme. However, [20] does not cover the following topics: detailed description of the STC scheme, detailed DSP implementation details, detailed hardware description of the switched resistor scheme built across two generations, Gen-1 and Gen-2; detailed experimental validation of the proposed approach. The present manuscript delineates the above-mentioned points in detail.

Moreover, the STC scheme uses discrete components that are easy to procure. The scheme is easy to synthesize with the increased reliability of high-speed GaN devices and their drive techniques that can switch a resistor with enormous speed without the need for integrated ASICs [19] or complicated mixed-signal schemes [14], [16]. Also, it uses the most common industrial-scale processor, F28379D, to realize the circuit without any significant computational burden or complex control [14], [16].

The manuscript is organized as follows: Section II delineates the STC framework and its application to the Ćuk based PES. Section III describes the hardware set-up synthesized to perform STC, along with experimental results. Some appendices are incorporated to ease comprehension.

II. SWITCHING TRANSITION BEHAVIOR AND CONTROL

A. MOTIVATION BEHIND STC FOR THE ĆUK PES

In this section, the motivation behind the switching transition control framework for a Ćuk PES is delineated. Figure 3a shows the schematic of the Ćuk PES. The Cree SiC MOSFET half-bridge module (the details of the module are protected by a Non-Disclosure Agreement) used for the PES constitutes of two HF SiC switches denoted by M_1 and M_2 in Figure 3a. According to the modes of operation of the Ćuk PES in CCM operation (shown in Appendix II), the body-diode of MOSFET M_1 operates during both turn-on/turn-off transitions in deadtime and leads to near zero-voltage switching of



FIGURE 3. (a) Figure showing a Ćuk PES. (b) Figure showing the loss breakdown of a Ćuk PES at $V_{ds_{M2}} = V_{ds_{M1}} = 500 \text{ V}$, $I_{ds_{M2}} = I_{ds_{M1}} = 20 \text{ A}$, $P_{in} = 5 \text{ kW}$.

MOSFET M_1 . So, the switching losses of the PES are mainly associated with the hard-switched transition of switch M_2 . Operating the Ćuk PES at 5 kW for $V_{ds_{M2}} = V_{ds_{M1}} = 500 \text{ V}$ results in the power loss distribution shown in Figure 3b, which is dominated by the switching loss of the switch M_2 of the SiC module. (Of the total switching losses of switch M_2 , more than 70% is the turn-on switching loss). The Cree SiC MOSFET half-bridge module is usually driven by an industrial Cree gate driver with fixed gate resistances and two isolated channels for each of the SiC MOSFETs M_1 and M_2 . Each of the gate-loop channels being a 2nd order LC system, the total gate resistance should be large enough to damp any resonance arising in the gate loop. The net required gate resistance, from a damped gate-loop perspective (or the minimum external gate resistance that serves to damp the gate resonance), can be calculated from the equation [21]:

$$R_{init} + R_{ext} \ge 2\rho_{SiC} \sqrt{\frac{L_{int} + L_{ext}}{C_{iss}}}$$
(1)

In (1), R_{init} denotes the internal gate resistance, and R_{ext} denotes the external gate resistance in the driver circuit of each of the MOSFETs M_1 and M_2 (of the SiC module). Also L_{int} and L_{ext} denote the parasitic inductance internal to the SiC module, and external to the module in the gate drive loop, respectively. C_{iss} denotes the input capacitance of the MOSFETs M_1/M_2 . For avoiding any resonance in the gate loop, ρ_{SiC} should be greater than unity. For the Cree SiC half-bridge modules chosen for hardware validation, with available values of L_{int} and L_{ext} , R_{init} is set at 1 Ω (internal to the SiC module and fixed) to avoid oscillations for zero R_{ext} . After that, R_{ext} should be set accordingly to limit switching losses of MOSFET M_2 while taking into consideration the stress on the devices because of high di/dt and dv/dt due to faster turn-on of MOSFET M_2 .



FIGURE 4. (a) Figure showing the schematic of the SiC half-bridge module with the passive gate drive circuit. (b) Figure showing spurious turn-on of the high side switch M_1 due to diode reverse recovery induced oscillations.

Notwithstanding, using a fixed $R_{ext} = R_{on_1}$ at turn-on, as shown in Figure 4a, admissible power loop and gate driver performance is achieved only for higher values of the gate resistance R_{on_1} . When a lower R_{on_1} is applied to decrease the switching losses in a half-bridge set-up like Figure 4a two noticeable problems arise at turn-on of MOSFET M_2 :

1) due to higher dv/dt across switch M_1 when the lower MOSFET M_2 is turning on, the rapid charging current (i_{gd_1}) of the Miller capacitance can lead to spurious turn-on of the high-side switch M_1 leading to a shoot-through event [22].

2) due to higher dv/dt at the onset of the Miller region in the lower MOSFET M₂, the body diode of MOSFET M₁ reverse recovers at a very high rate, leading to higher di/dt rates. This results in a voltage drop across the common source inductance $\Delta v = L_{cs_1} \frac{di}{dt}$ across the gate of the upper MOSFET which may also lead to spurious turn-on and oscillations. Scenario (2) is illustrated in Figure 4b.

Traditionally (1) is taken care of by decreasing the turn-off gate resistance of switch M_1 . However, this reduces damping in the gate path and the voltage drop due to Δv (point 2) causes considerable current flow in the gate loop path which is undesirable. Hence to take care of (2), a larger gate

resistance is desired to limit the circulating current due to Δv . However, the increase in gate resistance exacerbates (1). Hence, this optimality between (1) and (2) is difficult to reach for modules with have large common source inductance [23].

Also, for boosting the efficiency of the HF Cuk PES by decreasing the switching losses on lower MOSFET M_2 (since switching loss of M_2 accounts for the majority of losses of the PES as shown in Figure 3a) the turn-on resistance needs to be decreased which will lead to the problems delineated in points (1) and (2).

Hence, an STC method is adopted here to explore whether using variable gate resistance use during the SiC MOSFET transition can help the Ćuk PES meet a target efficiency improvement by reducing the switching losses while precluding excessive parasitic oscillations that result due to reduced turn-on resistance.

B. STC FOR TURN-ON TRANSITION OF ĆUK PES

Figure 5a shows the switched resistor-based circuit synthesis for STC network, and Figure 5a shows the STC circuit when applied to the Ćuk PES.

The external resistance of the turn-on path for MOSFET M_2 (Figure 5a/b) can be expressed as:

$$R_{ext} = R_{on_1} + \overline{S_{L1}}R_{on_2} \tag{2}$$

The turn-off path resistance for MOSFET M_2 can be expressed as:

$$R_{ext} = \overline{S_{L3}}R_{off} || (\overline{S_{L1}}R_{on_2} + R_{on_1})$$
(3)

In (2) and (3), R_{on_1} is a fixed gate resistor in the gate drive path, while $\overline{S_{L1}}R_{on_2}$ and $\overline{S_{L3}}R_{off}$ are the dynamic values of the turn-on and turn-off gate resistances. As such, S_{L1} and S_{L3} switch at extremely high frequencies and are 1000-fold faster than the Cree SiC module switching frequency. The pulse-widths of S_{L1} and S_{L3} can be controlled to create an affective gate resistance in a transition region.

The STC network is also built for the turn-on and turn-off paths of the SiC module for MOSFET M_1 . ($\overline{S_{H1}}R_{on_2}$ and $\overline{S_{H3}}R_{off}$ are the dynamic values of the turn-on and turn-off gate resistances for MOSFET M_1). This is primarily because:

1) Since the Ćuk modules (Figure 3a) are purely bi-directional [1], the roles of switches M_1/M_2 can be reversed in some cases.

2) The Cuk modules are recently used in differential-mode topologies [3], and depending on modulation strategies, the switches M_1/M_2 change roles. However, (1) and (2) are not explored in the present manuscript.

FOLLOWING A PRE-DEFINED TURN-ON TRAJECTORY

For turn-on control, the STC network modulates the switching sequence of the HF switch S_{L_1} (both duty cycle and period), as shown in Figure 6 (as an illustrative example), to create an average gate resistance in between $R_{ext} = R_{on_1} + R_{on_2}$ and R_{on_1} . This is done to follow a pre-defined V_{ds} trajectory. R_{on_1} is a smaller value of gate resistance that is chosen





to create optimal gate damping [21]. R_{on_2} is a higher value of the gate resistance that is chosen in a way to give higher controllability to the turn-on STC scheme. For the SiC module under consideration, due to higher value of transconductance (the term is explained in [7]), the time from V_{th} to start of the Miller region is very small and the device current reaches steady state very fast. The main switching loss, as shown in Figure 6, is thus dominated by the Miller region due to the higher parasitic capacitances of the SiC module under consideration. Optimally shaping this region leads to efficiency improvement. Again, the MOSFET capacitance that controls the Miller Region [7] is non-linear. Due to this non-linear nature, at the onset of $V_{ds_{M_2}}$, the dv/dt slope is very high



FIGURE 6. Figure showing the turn-on Vds trajectory control using STC.

and the slope progressively decreases with decreasing value of $V_{ds_{M_2}}$. As shown by the varying pulse-widths in Figure 6, the switching sequence of S_{L_1} can be chosen in a way to create higher resistances during the onset of $V_{ds_{M_2}}$ fall to reduce dv/dt, while progressively applying lower resistances as the voltage gradient reduces to save switching losses.



FIGURE 7. Waveforms for MOSFET turn-on and STC scheme for the switch S_{L_1} .

2) REDUCING DIODE REVERSE RECOVERY-BASED OSCILLATIONS TO BOOST PES EFFICIENCY

Figure 7 further highlights the SiC MOSFET M_2 turn-on waveforms and the STC scheme for the switch S_{L1} . The three control variables T_{w_1} , T_{w_2} and T_{w_3} for the switch S_{L1} during

the turn-on transition control the voltage and current overshoot, along with the switching losses of the SiC MOSFET.

During turn-on of the SiC MOSFET M_2 , the reverse recovery of the diode of SiC MOSFET M_1 is of importance as it affects the turn-on loss of M_2 . Before the onset of Mode 2 in the Cuk PES (shown in Appendix II), during Mode 1 the body diode of M_1 was conducting during deadtime. It was carrying a net current of $I_{L_a} + I_{L_b}$ (See Figure 3a). As the gate to source voltage of M_2 rises above the V_{th} , (shown by the point t_1 in Figure 7 the current $I_{L_a} + I_{L_b}$ flowing through the body diode of M_1 starts shifting to M_2 . During the onset of the Miller region at t_2 , the current overshoot increases from $I_{L_a} + I_{L_b}$ to $I_{L_a} + I_{L_b} + I_{dsrr}$ at t_3 , where I_{rr} is the reverse recovery current of the diode, and $\Delta i_L = I_{dsrr}$ as shown in Figure 7. Due to high $\frac{dV_{ds_{M_2}}}{dt}$ during $t_3 - t_4$, the stored charge in the body diode increases at an enhanced rate, leading to the diode current falling to zero at high $\frac{di}{dt}$. This $\frac{di}{dt}$ rate is several fold higher than the rate at which the device current of M_2 , $I_{ds_{M_2}}$ reaches $I_{L_a} + I_{L_b}$ from zero [7], [15]. This high $\frac{di}{dt}$ results in voltage drop across the common source inductance L_{CS_1} (as shown in Figure 5b) which may lead to spurious turn-on of the high side device (Section II, A1). Moreover, the high $\frac{di}{dt}$ may lead to voltage drops across the drain to source inductance of M_1/M_2 , which may lead to additional oscillations that result in excess common mode EMI and device conduction losses.

Appendix III derives the analytical equations for the MOSFET M_2 turn-on (Figure 7). The analytical equations are guided by references [7], [14], [15], [24]. As such, these analytical timings are close to the experimental timings for SiC MOSFETs, as shown in [7], [24].

To perform STC for this turn-on transition, a unique switching scheme for the switch S_{L1} is followed, which is shown in Figure 7. Post V_{th} , and before the onset of the Miller region at t_2 , the STC scheme sets the external gate resistance for a period T_{w_1} as:

$$R_{ext} = R_{on_1} + \overline{S_{L1}}R_{on_2} = R_{on_1} \tag{4}$$

This is the region $t_1 - t_2$ (Appendix III). From SiC device dynamics [7], [21], [24], decreasing the region $t_1 - t_2$ causes $I_{L_a} + I_{L_b}$ to rise faster. This results in decreased switching losses for the PES by reducing the V-I overlap.

After the onset of the Miller region, a higher gate resistance is applied by STC by giving a low duty cycle to S_{L1} . The gate resistance is given by:

$$R_{ext} = R_{on_1} + \overline{S_{L1}}R_{on_2} = R_{on_1} + (50 - 100\%)R_{on_2}$$
(5)

This is done for a period T_{w_2} to decrease the $\frac{dV_{ds_{M_2}}}{dt}$ fall rate to cause slower diode reverse recovery, which in turn will lead to less $\frac{di}{dt}$ induced oscillations by the reverse recovery current. After the pre-calculated period T_{w_2} in the Miller region when the diode reverse recovery has ended (Appendix III and [7], [24] derives the timings), STC applies a lower gate resistance by modulating the duty cycle of S_{L1} . The lower gate resistance is given by:

$$R_{ext} = R_{on_1} + \overline{S_{L1}}R_{on_2} = R_{on_1} + (0 - 50\%)R_{on_2}$$
(6)

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STC applies this lower gate resistance for a period T_{w_3} as shown in Figure 7 until the end of the Miller Region. This results in an enhanced rate of $\frac{dV_{ds_{M_1}}}{dt}$ fall, thereby decreasing the transition region post t_4 which leads to switching loss reduction. If a constant gate drive resistance R_{on_1} (that gives optimal damping, (1) and reference [21], [24]) is used throughout the transition region, the diode reverse recovery-based oscillations lead to high current overshoot rates, which leads to the issues discussed in Section II.A1.

Hence, the STC scheme helps achieve optimality of Ćuk PES operation. For any operating point, depending on a particular desired dv/dt profile, STC can shape the $V_{ds_{M_2}}$ trajectory that can optimize switching losses and parasitic oscillations that result from decreasing switching transitions.

C. STC FOR TURN-OFF TRANSITION OF ĆUK PES

Contrary to the turn-on transition, the turn-off transition for the SiC module under consideration is not plagued by any diode reverse recovery effects. Also, the turn-off losses of the SiC MOSFETs are much smaller than the turn-on losses [25]. For the current PES behavioral dynamics and the test scenario, an STC scheme is not required for efficiency improvement during device turn-off mainly because of these reasons:

1) keeping a low value of the passive gate resistance results in very low overall turn-off losses for the Ćuk PES. There are two issues of using a lower value of turn-off gate resistance. First, the higher dv/dt during turn-off can lead to high common-mode currents in the PES [5]. It can charge the parasitic capacitances between the switching node and earth, and the common-mode EMI can violate the EMI standards [5]. It can increase the CM EMI filter size of the PES [5]. The turn-off gate resistance for the PES is chosen accordingly and is optimized between CM EMI level and turn-off switching losses.

Secondly, for the current fall period (depending on SiC device physics [7], [24]), the presence of high values of L_{ds_2} in the drain-source path (Figure 5), can result in $L_{ds_2} \frac{di}{dt}$ based voltage overshoots which may cause excessive voltage stress on the device. However, for the experimental setup under consideration, L_{ds_2} and currents are low enough not to create issues with device overvoltage stress.

2) Very importantly, the turn-off losses are less susceptible to gate resistance variation than turn-on losses [25]. Since the voltage gradient across the gate resistor is much smaller during the turn-off transition regions, a larger value of gate resistor variation is required to modify the voltage rise and current fall trajectories. Hence, the effect due to minor gate resistance variation during turn-on is not present during turn-off.

D. STC SCHEME AND DSP IMPLEMENTATION

The STC scheme is implemented using a simple mixed signal circuit with low complexity. For the digital signal generation, the E_{PWM} modules of TMSF28379D, a low-cost



FIGURE 8. Figure showing the DSP implementation of the proposed STC scheme.

industrial-scale digital processor and external combinational logic circuitry is used. Figure 8 shows an illustrative example for turn-on transition control of STC switch S_{L1} .

 E_{PWM1} of TMSF28379D is set as a master module and is used to generate the main gate pulses of the SiC half-bridge module. To generate the S_{L1} signal, E_{PWM} modules 2, 3, and 4 are used as slave modules. All the E_{PWM} modules are positive edge triggered. The slave modules 2,3 and 4 create three phase staggered signals ($\emptyset = X_1, X_2, X_3$) having pulse widths (or turn-on time) of T_1, T_2 , and T_3 respectively, with their periods being the same as that of E_{PWM1} master module.

As shown in Figure 8, external to the processor, the three phase staggered signals from E_{PWM2,3,4} are sent to a combinational logic drive to generate the final STC signals. Two important delays, also shown in Figure 8, are considered

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while constituting the signals: 1) Delay₁: denote the transmission delay between the main gate signal generated by the processor, E_{PWM1} and the actual triggering of the SiC switch signal, $V_{gs_{M_2}}$. 2) Delay_{2,3,4}: denote the transmission delay of the switching sequence between the STC signals, $E_{PWM2,3,4}$ generated by the processor and the actual triggering of the STC switches. Both these delays are mainly due to the drive stages and remain constant.

III. EXPERIMENTAL WORK

A. HARDWARE DESIGN OF THE STC NETWORK

The switched resistor network based STC network, the schematic of which is shown in Figure 5a, can modulate the switching pattern of the STC switches S_{L1} and S_{L3} for MOSFET M₂ ($/S_{H1}$ and S_{H3} for MOSFET M₁) to affect the net gate resistance in the gate drive turn-on and turn-off paths, respectively. For a particular operating condition of the PES, the corresponding modulating waveform guiding $S_{L1}/S_{L3}/S_{H1}/S_{H3}$ (calculated by the F28379D processor) is sent to the gate driver of the STC switches. The functional block diagram of the driver with the switched resistor based STC network is shown in Figure 9.



FIGURE 9. Figure showing functional block diagram of the Gen 1/ Gen 2 driver.

For the switched resistor network, the GaN-FETs are chosen because: 1) For test values of load current and blocking voltages, the SiC device transition region varies in the vicinity of 120-130 *ns*. Hence, the switched resistor network should make multiple transitions inside the turn-on and turn-off times of the main SiC device to shape the rise/fall trajectory. Hence, the choice of $S_{L1}/S_{L3}/S_{H1}/S_{H3}$ should be such that its parasitic capacitances and package inductances are 1000-fold smaller than that of the main FET. GaN-FETs are a good choice in this regard.

2) For the desired gate current levels, GaN-FETs are the best commercial option that satisfies (1). This lets them attain very low pulse widths. The pulse widths are much lower than the transition regions of the main SiC FET.

The STC switched resistor network is developed across two generations/iterations (Gen-1 and Gen-2) which is described below for turn-on control of the STC switch S_{L1} (the design of $S_{L3}/S_{H1}/S_{H3}$ are similar):

1) GEN-1 GATE DRIVER PROTOTYPE (HARDWARE DESCRIPTION)

The Gen-1 and the Gen-2 design mainly differs in the design of the STC network. Faster GaN-FETs and more state-ofthe-art gate drivers are used in Gen-2 compared to Gen-1.

Figure 10a shows the Gen-1 gate driver board containing the STC network. The gate driver board houses components encompassing two separate isolated gate drive paths for each of the SiC MOSFETs in the half-bridge module along with the STC network for each MOSFET, with an integrated F28379D processor to give online commands to the STC network. These important functionalities of the Gen-1 gate driver are highlighted in Figure 9 (functional block diagram) and Figure 10a (hardware-Gen-1).

The STC network in Gen-1 uses GS-065-011-1-L GaN-FETs with $C_{rss} < 10 \text{ pF}$, and $C_{oss} < 150 \text{ pF}$ for the gate drive blocking voltage under consideration (See Appendix I for the terms). The GaN-FETs are driven Si8271GB gate drivers from Silicon Labs, with separate turn-on and turn-off paths. The external gate resistance for turn-on and turn-off are set at 1 Ω each. The idea behind the design is to drive the GaN-FETs as fast as possible using low-gate resistances to attain fast transitions. Since the gate driver blocking voltages and currents are much lower than the ratings of the GaN-FETs used, the fast transitions ensure the operation of the device within the thermal limits. The design leads to rise transitions of 8-10 *ns* for the GaN-FETs and fall transitions of 2-3 *ns*.

The targeted pulse widths in the range of 10 ns are not achievable with the Gen-1 design (reasons will be discussed in Section III, A1.3), which lead to a modified Gen-2 design.

2) GEN-2 GATE DRIVER PROTOTYPE (HARDWARE DESCRIPTION)

Figure 10b shows the Gen-2 gate driver board. Like Gen-1, the new board also houses components encompassing two separate isolated gate drive paths, and the F28379D processor. Only one of the isolated legs of the Gen-2 driver with the STC network is highlighted in Figure 10b.





Digital core

(a)





(b)

FIGURE 10. (a) The Gen-1 gate driver prototype and some of its important functionalities (both isolated legs) (b) The Gen-2 gate driver prototype and some of its important functionalities (one isolated leg).

 TABLE 1. Comparison of the STC network.

	Gen-1	Gen-2
STC Device	GS-065-011-1-L	EPC8004
Device Dimensions	5, 6 mm	820, 2080 μm
STC Driver	Si8271-GB	LMG1020
Operating C _{iss}	80 pF	25 pF
Operating C _{rss}	10 pF	1.2 pF
Operating Coss	150 pF	45 pF

The STC network in Gen-2 uses EPC8004 GaN-FETs with $C_{rss} < 2$ pF, and $C_{oss} < 50$ pF for the gate drive blocking voltage under consideration. The EPC GaN-FETs are driven by a state-of-the-art gate driver from Texas instruments, LMG1020. The drivers and switches in the STC network (Gen-1/ Gen-2) are compared in Table 1.

The driver LMG1020 is used in LiDAR applications to drive fast GaN-FETs at 1 *n*s pulse-width. The external gate resistance for turn-on and turn-off are set at 10 Ω and 5 Ω ,

respectively. The design leads to rise and fall transitions in the vicinity of 1 *ns* for the GaN-FETs. Hence the new design can achieve pulse widths well within 10 *ns*, leading to a greater granularity of the STC framework. Section III.A1.3 goes further into the differences in design considerations between Gen-1 and Gen-2 design.

3) GEN-2 V/S GEN-1

Synthesis of the GaN-FET based STC network encompasses some major HF loops which require careful design considerations. Figure 11a and Figure 11b compares the STC device and gate driver design of the GaN-FET based switch S_{L1} in terms of PCB footprint and size.

As previously discussed, the switching of S_{L1} which is a GaN-FET based device, controls the dynamic resistance R_{on_2} to modulate the gate current. The recommended main gate driver IC of each of the MOSFETs M_1 and M_2 in the half-bridge module is rated for 14 A peak current. Hence the GaN-FET based switch was chosen for this application since it is amongst few commercially available options that can conduct the high gate current when S_{L1} is on, and due to its low parasitic capacitance can attain very low pulse widths.

However, the GaN-FET switch poses predicaments in gate and power loop design. The FETs have very low threshold voltage and a very low margin between optimal and maximum allowable gate voltage [3]. An ill-designed gate and power loop may cause a false turn-on of the device, defeating the key objective of STC. Figure 11c identifies two key loops, Loop-1 and Loop-2 that requires careful design considerations both in the Gen-1 and Gen-2 boards.

(a) Loop-1: Loop-1 mainly involves the gate drive design for the GaN-FET network. The GaN-FET in Gen-1 is driven by an isolated gate driver, with separate turn-on and turn-off paths. To reduce PCB design complexity, a single positive supply gate driver is used, and the PCB design is carefully optimized to reduce spurious swings of the gate to source voltage waveforms. Also, the GaN-FET is chosen to have a dedicated Kelvin source that perfectly decouples the gate and the power loop. Using the relation $R_{init_{GaN}}$ + $R_{ext_{GaN}} \ge 2\rho_{GaN}\sqrt{\frac{L_{int}+L_{ext}}{C_{iss}}}$, the gate loop is designed for minimum $R_{ext_{GaN}}$ to get the fastest transition times possible [21]. $R_{init_{GaN}}$, $R_{ext_{GaN}}$ denote the internal and external values of the resistances in the gate drive circuit (lumped together as R_g in Figure 11c), while $L_{int_{GaN}}$, $L_{ext_{GaN}}$ (lumped together as L_{gs} in Figure 11c) denote the internal and external values of the parasitic inductances in the gate drive circuit.

In the Gen-1 board, using a 5 V constant gate drive supply, and a very low gate resistance of $R_g < 2 \Omega$, theoretically transition times of less than 5 *n*s can be achieved. However, for the gate drive circuit shown in Figure 11a, the gate-source inductance L_{gs} (due to larger GaN-FET package) and common source inductance L_{cs} slowed down the switching transitions considerably, resulting in rise transitions of 8-10 *n*s and fall transitions of 3 *n*s. This put a limit on the maximum pulse width of the GaN-FETs that can be achieved in the Gen-1 board, and thus limited the STC granularity.



The shortcomings of Gen-1 are addressed in Gen-2 by carefully designing the gate drive loop. Gen-2 uses EPC8004 GaN-FETs (from EPC) which has a much smaller footprint

than GS-065-011-1-L GaN-FETs from GaN Systems (the comparison is shown in Figure 11a and Figure 11b). Compared to the Gen-1 gate drive design which used 0603 resistors for R_g , Gen-2 uses even smaller 0402 footprints, thereby considerably limiting the inductance L_{gs} . Also, due to the smaller package of EPC8004 GaN-FETs, the common source inductance L_{cs} is bound to have a smaller value in Gen-2, although both the designs use Kelvin source connections.

Gen-2 encompasses another important design change in the choice of the gate driver. Gen-2 makes uses of the LMG1020 gate driver. The miniaturized gate driver (Figure 11b) specialized for Lidar applications can create pulse widths of about 1 *n*s (driving an input capacitance similar to the one in EPC8004 GaN-FETs) and has greater source/sink current capability than the Si8271-GB Gen-1 counterpart. Using a 5 V constant gate drive supply like Gen-1, and a gate resistance of $R_g = 10/5 \Omega$ for turnon/off, theoretical, and practical rise times of 600 *ps*/1 *ns* are achieved, respectively.

Hence, the use of EPC8004 FETs and LMG1020 driver in Gen-2 gives greater granularity to the change of the gate resistance in the transition region compared to Gen-1. The most important parameters of the gate driver are compared in Table 2.

	Gen-1	Gen-2
Gate Driver	Si8271-GB	LMG1020
Dimensions	3.9, 4.9 mm	0.8, 1.2 mm
Source I	4 A	7 A
Sink I	2 A	5 A
Rise time	6 <i>n</i> s	400 <i>p</i> s
Propagation Delay	60 <i>n</i> s	4.5 <i>n</i> s (max)

TABLE 2. Comparison of the gate drivers.

(b) *Loop-2:* The Loop-2 mainly dictates the maximum slew rate of the GaN-FETs that can be achieved. Loop 2 inductance is quite critical since it affects the FET switching behavior the most. The gate resistors, as shown in Figure 11a and Figure 11b, are placed close to the GaN-FET switches to minimize the stray inductance L_{ds} (Figure 11c).

Loop-2 is a relatively high current loop and makes/breaks peak currents as high as 4-6 A in nanoseconds. This causes relatively high $\frac{di}{dt}$ of about 4-6 A/ns. The high $\frac{di}{dt}$ can couple with the common source inductance L_{cs} creating a negative feedback loop, thereby slowing down the GaN-FET and deteriorating the performance of the STC network. Hence the use of Gen-2 STC network is quite important in this regard in creating a design with minimal common source inductance L_{cs} (Figure 11c).

B. THE HARDWARE PLATFORM FOR EXPERIMENTAL VALIDATION

Figure 12 shows the hardware platform of the WBG Cuk PES that is rapidly synthesized to test the gate drivers, Gen-1, and



FIGURE 12. Figure showing the STC hardware validation platform. The V_{gs} signals (probed) of the SiC half-bridge module in the actual hardware platform are shown. The hardware is tested up to 5 kW and switching frequency of 50 kHz.

Gen-2. It consists of Cree SiC half-bridge modules driven by the STC based gate driver board. The set-up is made to handle drain to source voltages up to 800 V, and device currents up to 40 A. Figure 12 also shows the V_{gs} signals (probed) of the SiC half-bridge module in the actual hardware platform. $V_{gs_{M_2}}$ refers to the gate to source voltage of the low-side SiC MOSFET in the half-bridge module (in Figure 5), while $V_{gs_{M_1}}$ refers to the high-side SiC MOSFET gate to source voltage (in Figure 5). Referring to Figure 5, the resistive parameter values of the gate drive path are chosen as per Section II, A2.1: $R_{on_1} = 1 \Omega$, $R_{on_2} = 6.2 \Omega$, and $R_{off} = 2 \Omega$. As discussed in Section II, A2, R_{on_1} is fixed, while R_{on_2} and R_{off} can be modulated by GaN-FET based switches S_{L1} and S_{L3} . (Here only modulation of S_{L1} is considered as discussed in Section II, A2 and A3).

Figure 13 shows the difference in performance between Gen-1 and Gen-2 gate driver boards. S_{L1} is switched to create a pulse width of 10 *n*s on, and 10 *n*s off. Figure 13a and Figure 13b shows the performance of the Gen-1 gate driver board at a time resolution of 10 *n*s and 100 *n*s, respectively. Gen-1 gate driver gives less than satisfactory performance for the reasons discussed in Section III, A1.2. Figure 13c and Figure 13d shows the performance of the Gen-2 gate



FIGURE 13. (a)-(d) Comparison between Gen-1 and Gen-2 gate driver board performances. The traces from top to bottom show $V_{gs_{M_2}}$ and S_{L_1} . (a), (b) and (c), (d) show same waveform but with different time resolutions. $V_{gs_{M_1}}$ (5 V/div), S_{L_1} (5 V/div). Test levels, $V_{ds_{M_2}} = V_{ds_{M_1}} = 500 \text{ V}$, $I_{ds_{M_2}} = I_{ds_{M_1}} = 20 \text{ A}$.

driver. It gives satisfactory system performance in gate resistance variation. Figure 13d shows that the Gen-2 design can indeed achieve rise time of 1 *ns*. Pulse widths of less than 10 *ns* is a limitation on the part of the F28379D processor, and with faster digital processors with higher clock speeds, even 2-3 ns pulse widths can be obtained leading to more granularity of the STC network.

C. TURN-ON TRANSITION CONTROL

In Figure 14, the effect of controlling the turn-on switching transition is shown. Figure 14a and Figure 14b compares the performance of Gen-1 and Gen-2 board in controlling the $V_{ds_{M2}}$ falling transitions for the same operating point $V_{ds_{M2}} = V_{ds_{M1}} = 500 \text{ V}$, $I_{ds_{M2}} = I_{ds_{M1}} = 20 \text{ A}$. As discussed in Section III, A1.2, due to several design modifications in Gen-2 gate drive, STC achieves better granularity in the control of the STC pulse widths and achieves better noise immunity. Compared to only two transition events for the Gen-1 board, Gen-2 could achieve far more transitions that result in tighter control for a pre-defined $V_{ds_{M2}}$ trajectory.

In Figure 14b, $V_{ds_{M2ref}}$ denotes a reference $V_{ds_{M2}}$ trajectory. The trajectory denotes the $V_{ds_{M2}}$ transition for $R_{ext} = 4 \Omega$. Now, STC modulates the switch SL_1 to create the same trajectory using dynamic resistance $R_{ext} = R_{on_1} + \overline{S_{L1}}R_{on_2}$. Since $R_{on_1} = 1 \Omega$, and $R_{on_2} = 6.2 \Omega$, STC selects the switching sequence for switch SL_1 in a way to create an average resistance of $R_{on_1} + 0.4R_{on_2} = 4 \Omega$. Figure 14c also shows a $V_{ds_{M2}}$ trajectory tracking using STC, but with a decreased granularity of the switch SL_1 . In Figure 14c, the switch SL_1 has 35 % duty cycle, which coarsely leads



FIGURE 14. (a) Figure showing the turn-on transition control using STC for the Gen-1 board. The traces 2,3 and 4 show the $V_{ds_{M2}}$ (100 V/div), $V_{gs_{M2}}$ (5 V/div), and SL_1 (5 V/div), respectively. Figure showing the turn-on transition control using STC for the Gen-2 board to follow a $V_{ds_{M2}}$ trajectory (a) for 7 transition levels (b) for 3 transition levels. The traces 1, 2 and 4 in (a) show SL_1 (5 V/div), $V_{gs_{M2}}$ (5 V/div) and $V_{ds_{M2}}$ (100 V/div), respectively, and in (b) show SL_1 (5 V/div), $V_{ds_{M2}}$ (100 V/div) and $V_{ds_{M2}}$ (100 V/div), respectively.

to an external resistance of 5 Ω . $V_{d_{SM2ref}}$ denotes a reference trajectory for fixed $R_{ext} = 5 \Omega$. Increased granularity of the STC drive, thus achieves more smoother tracking of $V_{d_{SM2}}$, as depicted in Figure 14b compared to Figure 14c.

Figure 15a further shows how two different sequences of STC switch S_{L_1} (namely Seq1 and Seq2) can generate different $V_{ds_{M_2}}$ falling trajectories. A higher duty cycle for the STC switch results in lower gate resistance and higher transition speeds (Eqn. 2). Several such $V_{ds_{M_2}}$ falling trajectories are shown in Figure 15b as the duty cycles for the STC switch are varied.

1) REDUCTION IN GATE LOOP OSCILLATIONS DUE TO COMMON SOURCE INDUCTANCE AND EFFICIENCY IMPROVEMENT

As discussed in Section II. A2, decreasing the gate resistance to decrease the switching losses causes severe dv/dt and di/dt

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FIGURE 15. (a) Figure showing how different sequences can create different V_{ds} slopes during the turn-on transition. Seq₁ and Seq₂ denote the state of the STC switch S_{L_1} . The scales are as follows: $V_{ds_{M2}}$ (100 V/div), $V_{gs_{M2}}$ (5 V/div), and SL_1 (5 V/div), respectively. (a) Figure showing different $V_{ds_{M2}}$ transition slopes as a function of the duty cycle of STC switch S_{L_1} . Traces 3,2,4 show $V_{ds_{M2}}$ (100 V/div), $V_{gs_{M2}}$ (5 V/div), and SL_1 (5 V/div), and SL_1 (5 V/div), sequence of STC switch S_{L_1} . Traces 3,2,4 show $V_{ds_{M2}}$ (100 V/div), $V_{gs_{M2}}$ (5 V/div), and SL_1 (5 V/div), and SL_1 (5 V/div), sequence of STC switch S_{L_1} .

induced oscillations in the gate drive of the high-side switch M₁ (Figure 5) in the Ćuk PES. For the SiC module and topology under consideration, the oscillations due to the common source inductance (L_{CS1}) (di/dt induced) is a bigger issue than the Miller charging current (dv/dt induced). Figure 16a shows the gate drive signal of the high-side switch $M_1(V_{gs_{M1}})$ when the low-side switch is turning on $(V_{gs_{M2}})$ at R_{ext} = $R_{on_1} + \overline{S_1}R_{on_2} = R_{on_1} = 1 \Omega$. It shows severe ringing which persists even in Figure 16b, when an active Miller clamp is applied to the high-side switch M₁ which proves that the oscillations are due to the large common source inductance L_{CS1} ((di/dt induced). Using the STC scheme, as delineated in Section II, A2(methodology), A3(DSP implementation), and Section III, A2 (V_{ds} tracking results), the gate drive response of high-side switch M1 in Figure 16c is obtained (lower trace). It is compared to the upper trace in Figure 16c which shows the scenario when a higher gate resistance R_{ext} = $R_{on_1} + \overline{S_{L1}}R_{on_2} = R_{on_1} + R_{on_2} = 7.2 \ \Omega$ is applied. Hence, STC creates a scenario where a lower gate resistance can be applied to parts in the SiC transition region to increase PES efficiency while reducing gate-source oscillations.

2) STC IMPROVES PES EFFICIENCY

Figure 17 shows the constant efficiency increment of over 1% with increasing power levels achieved by the STC turn-on control scheme for the Ćuk PES, as delineated in



FIGURE 16. (a) Figure showing the gate-source oscillations resulting due to reduced gate resistance. (b) Figure showing persistent gate oscillations even with the implementation of active Miller clamp. Traces 1-4 show $V_{gS_{M2}}$ (5 V/div), V_{gSM_1} (5 V/div), SH_3 (10 V/div), and SL_1 (5 V/div). SH_3 is turned on to give a low impedance path to the current discharging C_{GD1} (Figure 4a). In (a) and (b), SL_1 is turned on decrease the turn-on resistance of the switch M_2 . (c) Figure showing reduced oscillations in gate-source due to the STC scheme.



FIGURE 17. Figure showing improvement of PES efficiency at $V_{dSM_2} = 500 \text{ V}.$

Section II, A2. For the experimental result in Figure 17, with the drain to source voltage of 500 V of the lower side switch M_2 , the switch currents are gradually increased. The improvement of efficiency is compared to a fixed gate resistance of $R_{ext} = 7.2 \Omega$. When a smaller value of the gate resistor $R_{ext} = 1 \Omega$ is used, the gate source oscillation increase to such high levels that the PES cannot be operated above 10 A peak (I_{dsM_2}) , as shown in Figure 17. From an efficiency standpoint, although a fixed gate resistor $R_{ext} = 1 \Omega$ will give higher efficiency numbers than STC initially, however, the severe di/dt induced oscillations will cause extra conduction losses in the system. Moreover, the oscillations lead to more V-I overlap, at the transition leading to increased switching losses too.



FIGURE 18. (a)-(d) Figure showing modes of operation in Ćuk PES for CCM.

With reference to Figure 3, the switching loss of switch M_2 still dominates the loss spectrum of the converter and contributes to about 70 % of the overall PES losses at 5 kW for $V_{ds_{M2}} = V_{ds_{M1}} = 500$ V (down from 80 % in Figure 3). The still higher percentage is attributed mainly to the overall lesser net losses because of improved efficiency due to STC and also due to dominant switching losses of switch M_2 across all operating conditions.

D. COMMENTS ON TEMPERATURE DEPENDENCY OF V_{th} AND TRANSCONDUCTANCE

As depicted in [26], the threshold voltage $(V_{gs_{th_{M2}}},$ Appendix II) and transconductance $(g_{fs_{M2}},$ Appendix II) of the SiC MOSFETs are functions of junction temperature of the MOSFETs. For the test scenarios undertaken and the thermal design of the PES, $g_{fs_{M2}}$ remains almost fixed, and variation of $V_{gs_{th_{M2}}}$ is under 50 mV (obtained from the device static and switching characterization results provided from the manufacturer). The deviation of these parameters are hence negligible in the present scenario and test setup. However, for even higher power levels, and different thermal designs, the junction temperature of the MOSFETs can indeed vary. Hence, as per the calculations of [26], the variation in $V_{gs_{th_{M2}}}$ and $g_{fs_{M_2}}$ need to be taken into account for affecting a particular transition region. Future works can be undertaken in that direction.

IV. CONCLUSION

An STC framework is created to affect the turn-on transition of a WBG PSD and to meet a PES level target (which in this case is an efficiency increment). First, depending on PES topological behavior and device physics, optimization areas to meet this target are identified and then the STC scheme is synthesized accordingly. For the test HF Cuk PES, the STC network achieved optimality of performance in terms of switching losses and diode reverse recovery stresses to meet the system level target. STC network achieved this optimality and gave a satisfactory performance for the test operating conditions.

Contrary to a contemporary analog technique based active gate drives, the proposed STC takes a simple mixed-signal approach in driving a GaN-FET switched resistor-based gate drive using commands from an industrial scale processor, and easily procurable discrete components. The STC network differentiates itself from the conventional switched resistor network based on the operational principle. Instead of using multiple resistors in a gate drive to achieve granularity that increases PCB gate drive footprint to the point of infeasibility, the STC network uses an extremely HF device and state of the art fast gate drivers to create an averaged gate resistance in a targeted transition region.

APPENDIX I

Some of the common abbreviations and nomenclature used is delineated here:

STC	Switching transition control
PSD	Power Semiconductor device
WBG	Wide bandgap
SiC	Silicon carbide
HF	High frequency
PES	Power electronic system
FET	Field-effect transistor
R _{init}	Internal gate resistance of SiC
	module
R _{ext}	External gate resistance of SiC
	module
R_{on1}, R_{on2}	External gate resistances of SiC
	module
$S_{L1}, S_{L3}, S_{H1}, S_{H3}$	STC GaN-FET switches
Lint, Lext	Internal and external gate inductance
	of SiC module
L_{cs_1}, L_{cs_2}	Common source inductance of
	M_1 , and M_2
L_{ds_1}, L_{ds_2}	Drain to source inductance of
	M_1 , and M_2

$$t_{3} - t_{1} = \frac{(I_{L_{a}} + I_{L_{b}} + I_{ds_{RR}})(\left(C_{gd_{M_{2}}}(t) + C_{gs_{M_{2}}}\right)(R_{ext} + R_{init}) + g_{fs_{M_{2}}}L_{cs_{2}}}{g_{fs_{M_{2}}}(V_{E} - 0.5\left(V_{M} + V_{gs_{th_{M_{2}}}}\right))}$$
(11)

$V_{ds_{M_{1,2}}}, I_{ds_{M_{1,2}}}$	Drain to source voltages and currents
1,2	of SiC module
R _{init GaN}	Internal gate resistance of GaN-FET
$R_{ext_{GaN}}$	External gate resistance of GaN-FET
$T_{w_1}, T_{w_2}, T_{w_3}, \emptyset$	Control parameters of STC switches
Gen-1, Gen-2	Generation-1 and 2

APPENDIX II

A. OPERATING MODES OF THE Cuk PES

Figure 18 shows the modes of the HF Cuk PES in continuous conduction mode (CCM). During Mode-1, the current iL_a through the inductor L_a , and iL_b through the inductor L_b , flows through the body diode of switch M_1 , after the switch M_1 is turned off. After a certain period of deadtime, Mode-2 starts with the turn-on of the switch M_2 , which now supports the entire current $iL_a + iL_b$. As reverse voltage $V_{ds_{M_1}}$ starts to build across the switch M_1 , and hence its body-diode, the diode undergoes reverse recovery at the onset of Mode-2, which adds to the current $iL_a + iL_b$ through switch M_2 . As Mode-2 ends, switch M_2 is turned off, and blocks voltage $V_{ds_{M_2}}$. The body-diode of M_1 again conducts during deadtime in Mode-3. During Mode-4, M_1 is turned on again with zero voltage across it.

APPENDIX III

With reference to Figure 7, the dynamics of the MOSFET M_2 transitions is discussed in this Appendix. The work in the literature [7], [24] for SiC MOSFETs is mainly followed since it closely matches the application at hand. The important regions required for STC is focused and only switch M_2 is considered.

After the threshold voltage $V_{gs_{th_{M_2}}}$ at t_1 (Figure 7), the drain current $I_{ds_{M_2}}$ rises following:

$$I_{ds_{M_2}} = g_{fs_{M_2}} \left[V_{gs}(t) - V_{gs_{th_{M_2}}} \right]$$
(7)

where $g_{fs_{M_2}}$ is the transconductance of the SiC MOSFET [7]. The drain current becomes $I_{L_a} + I_{L_b}$ at t_2 . After t_2 , the diode reverse recovery current of M_1 is added to $I_{L_a} + I_{L_b}$. Let $I_{ds_{RR}}$

be the peak reverse recovery current of the body diode. Then the duration from t_1 to t_3 can be written as follows:

$$t_3 - t_1 = \frac{(I_{L_a} + I_{L_b} + I_{d_{SRR}})(C_{gd_{M_2}}(t) + C_{gs_{M_2}})}{g_{fs_{M_2}}I_{g_{M_2}}}$$
(8)

At t_3 the MOSFET M_2 reaches its gate-source plateau voltage which can be written as:

$$V_M = V_{g_{s_{th_{M_2}}}} + (I_{L_a} + I_{L_b} + I_{d_{s_{RR}}})/(g_{f_{s_{M_2}}})$$
(9)

The gate current $(I_{g_{M_2}})$ in (8) can be written as:

$$I_{g_{M_2}} = \frac{V_E - 0.5 \left(V_M + V_{g_{s_{th}}} \right) - L_{cs_2} \frac{(I_{L_a} + I_{L_b} + I_{d_{s_{RR}}})}{t_3 - t_1}}{R_{ext} + R_{init}}$$
(10)

 L_{cs_2} is the common source inductance of SiC switch M₂, and $R_{ext} + R_{init}$ is the gate resistance. The time duration $t_3 - t_1$ can be calculated using (8)-(10) as (11), shown at the top of the page.

The peak reverse recovery current of the body diode, $I_{ds_{RR}}$, can be approximated as [7]:

$$I_{ds_{RR}} = \sqrt{2(I_{L_a} + I_{L_b}) \frac{I_{ds_{RR}} - datasheet}{T_{rr_{datsheet}}} \frac{Q_{rr} - datasheet}{I_o - datasheet}} \quad (12)$$

In (12), $Q_{rr-datasheet}$, $I_{o-datasheet}$ are the reverse recovery charge and test current levels from the device datasheet, respectively. Similarly, $I_{dsRR-datasheet}$, $T_{rr_{datsheet}}$ are the reverse recovery peak currents and times from the datasheet at the $I_{o-datasheet}$ test condition.

Then, we come to the next region $t_4 - t_3$. At t_3 , the non-linear capacitance $C_{gd_{M_2}}$ is at the lowest possible value [7], [24] and rate of fall of $v_{ds_{M_2}}$ is maximum.

$$t_4 - t_3 = \frac{C_{gd_{M_2}}(t)(R_{ext} + R_{init})(v_{ds_{M_2}}(t_4) - v_{ds_{M_2}}(t_3))}{V_E - V_M} \quad (13)$$

At t_4 , when the diode has reverse recovered, the voltage slope rate decreases, and the interval is given by:

$$t_6 - t_4 = \frac{C_{gd_{M_2}}(t)(R_{ext} + R_{init})(v_{ds_{M_2}}(t_6) - v_{ds_{M_2}}(t_4))}{V_E - V_M}$$
(14)

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