A Novel Modulation Scheme for Isolated PWM Active-Clamp Ćuk DC/DC Converter

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***Abstract*—A novel modulation scheme for a bidirectional isolated pulsewidth modulation active-clamp (PAC)-Ćuk converter is presented in this article. In the PAC-Ćuk converter, the clamping circuit consisting of a capacitor, a series inductor, and an active device enables zero-voltage-switching (ZVS) turn-ON capability of all the active devices. This additional circuit equips the converter with three independent control parameters. This article discusses power transfer, ZVS region, and circulating current dependency on the control parameters across the converter gain. Minimal circulating current is generally desired to decrease the conduction losses. With the help of the proposed modulation technique, the optimization of the control parameters to achieve lower circulating current while ensuring ZVS operation is also discussed. A 2-kW experimental converter is also designed and fabricated to validate the analysis.**

***Index Terms*—Active clamp, circulating current optimization, Ćuk converter, dc/dc converter, zero-voltage switching (ZVS).**

NOMENCLATURE

$V_{\text{in}},\ V_o$	Steady-state average input and output voltages of the converter, respectively.
$I_{Lin},\ I_{Lo}$	Steady-state average input and output currents of the converter, respectively.
$L_{\text{in}},\ L_o$	Input and output inductors, respectively.
$S_{P1},\ S_{P2}$	Primary-side main and auxiliary circuit switches, respectively.
$S_{S1},\ S_{S2}$	Secondary-side main and auxiliary circuit switches, respectively.
T_{sw}	Switching time period.
d_1, d_2	Duty cycles of the primary-side main switch (S_{P1}) and the secondary-side main switch (S_{S1}), respectively.
Δ_ϕ	Phase-shift ratio defined as the ratio between the time period when both main switches S_{P1} and S_{S1} are inactive in the switching period, T_{sw}.
d_1', d_2'	Duty cycles of the primary-side auxiliary switch (S_{P2}) and the secondary-side auxiliary switch (S_{S2}), which is complementary of the main switch.
$C_{B1},\ C_{B2}$	Primary- and secondary-side blocking capacitors, respectively.
$V_{CB1},\ V_{CB2}$	Steady-state average voltages across capacitors C_{B1} and C_{B2} over a switching period T_{sw}, respectively.
$C_{T1},\ C_{T2}$	Primary- and secondary-side auxiliary circuit capacitors, respectively.
$V_{CT1},\ V_{CT2}$	Steady-state average voltages across the capacitors C_{T1} and C_{T2} over a switching period T_{sw}, respectively.
L_r	Auxiliary inductor in series with C_{B1}.
L_{lk}	Leakage inductance of the transformer referred to the primary side.
L_{eq}	Lumped equivalent inductor $(L_r + L_{\text{lk}})$ in series with the blocking capacitor C_{B1} referred to the primary side.
$i_{L\text{eq}}(t)$	Instantaneous current through L_{eq}.
$v_1(t), v_2(t)$	Instantaneous node voltages across the main devices S_{P1} and S_{P2}, respectively.
$i_1(t)$	Total current going into the node voltage $v_1(t)$.
$i_2(t)$	Total current going out of the node voltage $v_2(t)$.
$v_2'(t)$	Instantaneous node voltage $-v_2(t)$ referred to the primary side.
C_B	Equivalent blocking capacitor referred to the primary side.
t_{db}	Deadband between the gate of the main and auxiliary switches.
C_{oss}	Equivalent constant output capacitance of the switch.
$I^2_{L,\text{RMS}}$	Mean square current through the equivalent series inductor, L_{eq}.
G	Converter gain defined as the ratio between V_o and V_{in}.
I_{in}	Current from the primary-side connected source with a 100-μH filter.

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I. INTRODUCTION

BIDIRECTIONAL dc/dc converters have emerged as the center of research in power electronics. The capability of bidirectional power flow allows this category of converters to

be used in a multitude of applications, such as dc smart grids [1]–[3], electric vehicles [4], [5], and energy storage systems [6]–[8]. Extensive research work has focused on the development of reliable, compact, and efficient isolated dc/dc converters. Conventional galvanic isolation for these systems requires bulky and costly low-frequency transformers [9], [10]. An isolated dc/dc converter is equipped with high-frequency-transformer-based isolation, yielding a cheaper and lightweight isolation solution. High-voltage conversion gain required in some applications can also be realized by using the turns ratio of the transformer [11], [12].

Numerous isolated bidirectional dc/dc converters have been proposed and researched in recent times. The most popular among them is the dual active bridge (DAB), introduced in [13]. The converter requires two H-bridges, comprising a total of eight active switches for bidirectional power flow. The single-phase-shift (SPS) modulation has a limited zero-voltage-switching (ZVS) region of operation and suffers from higher current stress [14]. Other modulation techniques are proposed, such as those based on dual phase shift (DPS) [15], triple phase shift (TPS) [16], and others with some variations [17]. These modulation techniques extend the ZVS turn-ON region and decrease the circulating current, resulting in higher efficiency of the system. However, circulating current minimization requires complex computation. Also, the DAB dc/dc converter has discontinuous input and output currents and, hence, requires additional filtering for practical applications. An additional blocking capacitor or control technique is also required to block the dc magnetization of the HF transformer.

In contrast, an isolated Ćuk converter requires only two active switches [18] to realize the bidirectional dc/dc converter. In addition, the input and output inductors of the pulsewidth modulation (PWM)-clamp Ćuk converter ensure continuous current flow, reducing the filter size. The magnetic component of the isolated Ćuk converter can also be integrated, resulting in a high-density system [19], [20]. However, switches in a conventional Ćuk converter are hard-switched, resulting in higher losses. In a bidirectional isolated Ćuk converter, the leakage inductance of a typical high-frequency transformer requires a lossy snubber circuit to dissipate the energy stored in the leakage inductor to limit the drain-to-source voltage across the devices [21]. This causes additional losses in the converter, reducing its application. Li *et al.* [22] explored a lossless active-snubber solution for bidirectional application. However, the snubber requires a complicated circuit with additional switches, diodes, capacitors, and inductors. The diodes incur additional losses, yielding a limited improvement in efficiency.

Incorporating an active-clamp snubber circuit in an isolated Ćuk converter can also limit the voltage stress on the components and transfer energy from the leakage inductance of the transformer [23]–[25] to auxiliary capacitors of the active-clamp circuit. The stored energy is then redirected back to the system with the possibility to achieve ZVS on the main switches and the added auxiliary switches.

The PWM active-clamp (PAC) circuit introduced in [26] enables the converter to achieve ZVS turn-ON. The active-clamp circuit exhibits circulating current, which results in the ZVS turn-ON of the main switch. In [25] and [27], a PAC circuit has been applied to a Ćuk converter for unidirectional power flow.

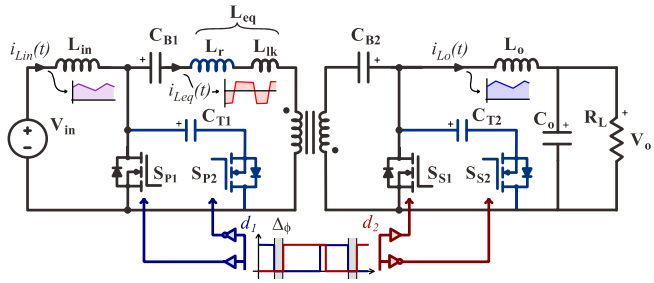

Fig. 1. Proposed bidirectional PAC-Ćuk converter topology.

In [24], a high-switching-frequency-operated bidirectional PAC-Ćuk converter was introduced. However, the ZVS operation of the converter relies on the magnetizing inductance of the transformer, whereas the active-clamp circuit is used as a snubber circuit to mitigate the effect of transformer leakage inductance. The magnetizing current of the transformer needs to be larger than the sum of input and output inductors for the ZVS operation, resulting in twice the current stress on the components. In addition, lower leakage inductance requires a larger auxiliary and blocking capacitor to avoid resonance between them, and hence, it is not practical for low-switching-frequency operation.

Fig 1. shows the proposed isolated bidirectional PAC-Ćuk converter. Two active-clamp circuits are added to the conventional isolated Ćuk converter: The primary-side circuit comprises capacitor C_{T1} and switch S_{P2}, whereas the secondary-side circuit comprises capacitor C_{T2} and switch S_{S2}. An additional series inductor L_r is also added, which is common to both active-clamp circuits. Two active clamp circuits are required in the proposed converter for a bidirectional operation. The PAC-Ćuk converter enables ZVS turn-ON of the switches while increasing the switch count by two and requires additional auxiliary capacitors. The leakage inductance energy of the transformer is now used by the clamp circuit to circulate current, which assists in ZVS turn-ON. As in the case of the conventional isolated Ćuk converter, the input and output inductors of the PAC-Ćuk converter provide continuous current flow. The proposed modulation of the bidirectional PAC-Ćuk converter is based on three control parameters as shown in Fig 1: the duty cycle of S_{P1}, d_1; the duty cycle of S_{S1}, d_2; and the phase-shift ratio Δ_ϕ, defined as the ratio between the time period when both S_{P1} and S_{S1} are inactive in the switching period. Table I provides a comparison between the PAC-Ćuk converter and other competitive converters and their modulation techniques. The proposed modulation for the PAC-Ćuk converter is easier to implement, has a wide ZVS range, and yields competitive efficiency for wide gain.

In conventional modulation [23]–[25], [27], the duty cycles of S_{P1} and S_{S1} are complimentary, whereas for the proposed modulation, the duty cycles are controlled independently. Independent control of the two duties and the phase-shift ratio allows three degrees of freedom for modulation. A more

TABLE I
COMPARISON BETWEEN THE PAC-CÚK AND THE DC–DC CONVERTERS

Converter	Soft-switching range	Soft-switching and optimization complexities	Range of converter gain, G	Power range	Efficiency
DAB with SPS [28]	Narrow	Low	0.6–1.2	200 W to 1 kW	85.0–96.1 %
DAB with DPS [29]	Medium	Medium	0.4–1	380 W	75.0–95.0 %
DAB with TPS [28]	Wide	High	0.6–1.2	200 W to 1 kW	96.0–97.3 %
DAB with unified TPS [16]	Wide	High	0.54–0.85	300–900 W	95.0–97.0 %
CLLC [4]	Wide	High	1	200 W to 1 kW	95.5–97.4 %
PAC-Ćuk with the proposed modulation	Wide	Low	0.6–1.3	400 W to 2 kW	96.5–97.8 %

accurate closed-form model as a function of the three independent control parameters of the PAC-Ćuk converter is developed in this article with experimental verification to form a new modulation scheme. The effects of the three control parameters on the power transfer capability of the converter, its ZVS region, and the circulating current through the leakage inductor are analyzed in detail using the model. Higher degrees of freedom enable the PAC-Ćuk converter to provide a set of solutions for the same operating condition, which allows the possibility of multiobjective optimization. In this article, the objective of the optimization is to minimize circulating current for a given output power while ensuring ZVS operation to limit conduction losses. Optimization of the duty cycles d_1 and d_2 to achieve the minimal circulating current for a constant Δ_ϕ is presented in this article.

The rest of this article is organized as follows. Section II presents the operation and analysis of the proposed converter. In Section III, power transfer, circulating current, and ZVS range are discussed. Section IV provides hardware design considerations and optimization of the control parameters for minimal circulating current. Section V provides the experimental results for validation of the analysis. Finally, Section VI concludes this article.

II. OPERATION AND ANALYSIS OF THE PAC-ĆUK CONVERTER

The PAC-Ćuk converter offers ZVS turn-ON of all the switches by using active-clamp circuits and the equivalent series inductor L_{eq}. The active-clamp circuit forces negative drain-to-source current, i_{ds}, through the FET forcing the body diode to turn ON before the gate, resulting in ZVS turn-ON of the switches. Large auxiliary capacitors (C_{T1} and C_{T2}) and blocking capacitors (C_{B1} and C_{B2}) act as a constant voltage (CV) source over a switching cycle. These capacitor voltages are imposed on the equivalent series inductor L_{eq} as per the active state of switches ($S_{P1}, S_{P2}, S_{S1}, S_{S2}$), resulting in power transfer and circulating current. Linear operation of the converter and analysis requires that the inductor current $i_{L\text{eq}}$ must be linear across the main modes, which is ensured by avoiding *LC* resonance during the operational modes. The minimum capacitor size condition is discussed in Section IV. In this article, only the forward power flow is considered where Δ_ϕ is referred from turn-OFF of S_{P1} to turn-ON of S_{S1}. For backward power flow, Δ_ϕ is referred from turn-OFF of S_{S1} to turn-ON of S_{P1}. The backward power flow follows the same analysis due to converter symmetry and is not discussed in detail. The transformer turn ratio of unity is chosen for simplicity in this article.

The operation of the converter can be divided into eight modes: four main modes ($M_1,\ M_2,\ M_3,$ and M_4) and four transition modes ($T_1,\ T_2,\ T_3,$ and T_4) as shown in Fig. 2. The waveforms associated with the modes are shown in Fig. 3. By applying volt-second balance on input inductor L_{in}, output inductor L_o, and series inductor L_{eq} over a switching cycle, the following steady-state average voltages are obtained:

$$V_{CT1} = V_{\text{in}}/d_1' \tag{1}$$

$$V_{CT2} = V_o/d_2' \tag{2}$$

$$V_{CB1} + V_{CB2} = V_{\text{in}} + V_o. \tag{3}$$

The duration of the phase shift between the primary and secondary gate signals is $\Delta_\phi T_{\text{sw}}$, as shown in Fig. 3. The input inductor ripple ($\Delta I_{L\text{in}}$) and output inductor current ripple (ΔI_{Lo}) are given as follows:

$$\Delta I_{L\text{in}} = \frac{V_{\text{in}} d_1 T_{\text{sw}}}{2L_{\text{in}}} \tag{4}$$

$$\Delta I_{Lo} = \frac{V_o d_2 T_{\text{sw}}}{2L_o}. \tag{5}$$

In Sections II and III, the current flowing into the node with voltage $v_1(t)$ is defined as $i_1(t)$, whereas the current coming out of the node with voltage $v_2(t)$ is defined as $i_2(t)$, as shown in Fig. 2. Currents $i_1(t)$ and $i_2(t)$ can be defined as follows:

$$i_1(t) = i_{L\text{in}}(t) - i_{L\text{eq}}(t) \tag{6}$$

$$i_2(t) = i_{Lo}(t) + i_{L\text{eq}}(t). \tag{7}$$

A. Modes of Operation of the Bidirectional PAC-Ćuk Converter

Analysis of modes of operation for the bidirectional PAC-Ćuk converter is drawn using Figs. 2 and 3. At t_0, S_{P2} and S_{S2} are conducting. Drain-to-source current of switch S_{P2}, $i_{P2}(t)$, is equal to $-i_1(t)$ and is negative in amplitude.

Mode 1 [$t_0 < t < t_1$] (Main mode, M_1): In this main mode, gate of S_{P2} is still OFF. As $i_{P2}(t)$ is negative, the body diode of S_{P2} is conducting. Before $i_{P2}(t)$ becomes positive, the gate is applied on S_{P2}, resulting in ZVS turn-ON of the device. Since the switches S_{P2} and S_{S2} are active, the voltage across the

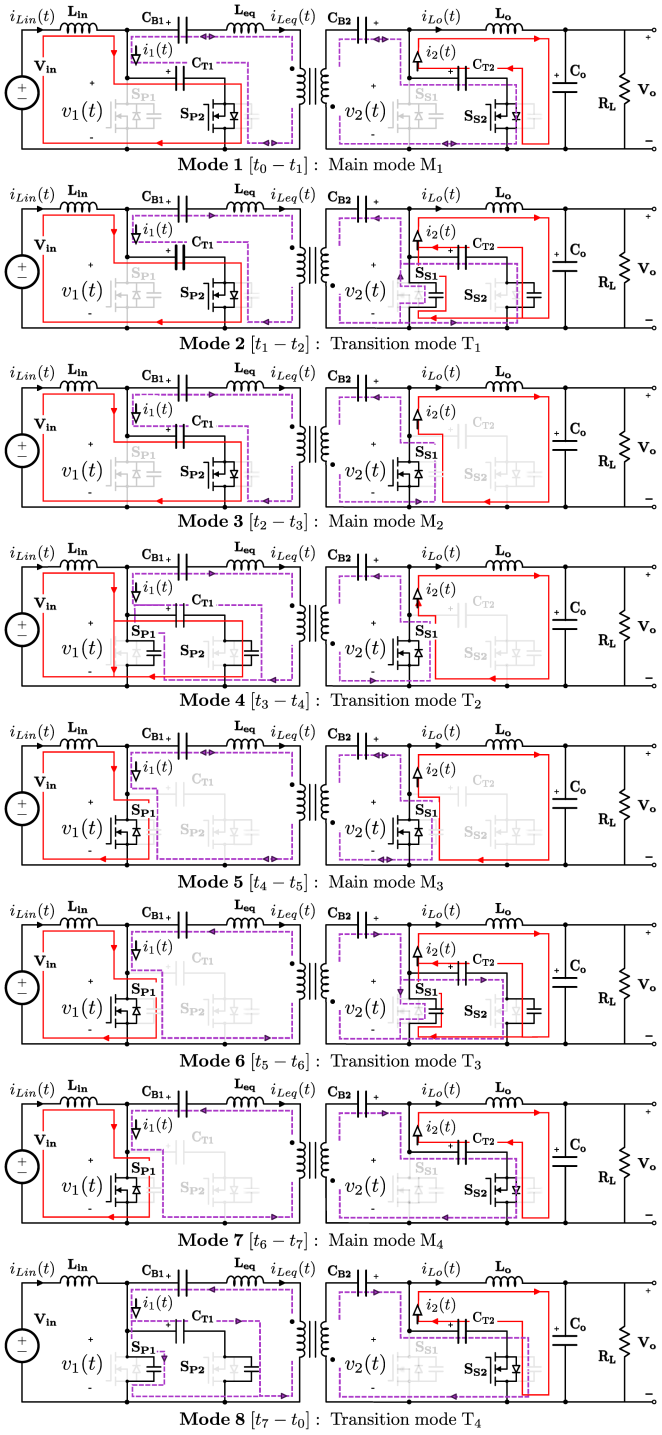

Fig. 2. Modes of forward operation of the bidirectional PAC-Ćuk converter.

inductor L_{eq} equals $V_{CT1} + V_{CT2} - V_{CB1} - V_{CB2}$. Current $i_{Leq}(t)$ ramps up linearly and is given as follows:

$$i_{Leq}(t) = \frac{V_{CT1} + V_{CT2} - V_{CB1} - V_{CB2}}{L_{\text{eq}}} (t - t_0) + i_{Leq}(t_0). \tag{8}$$

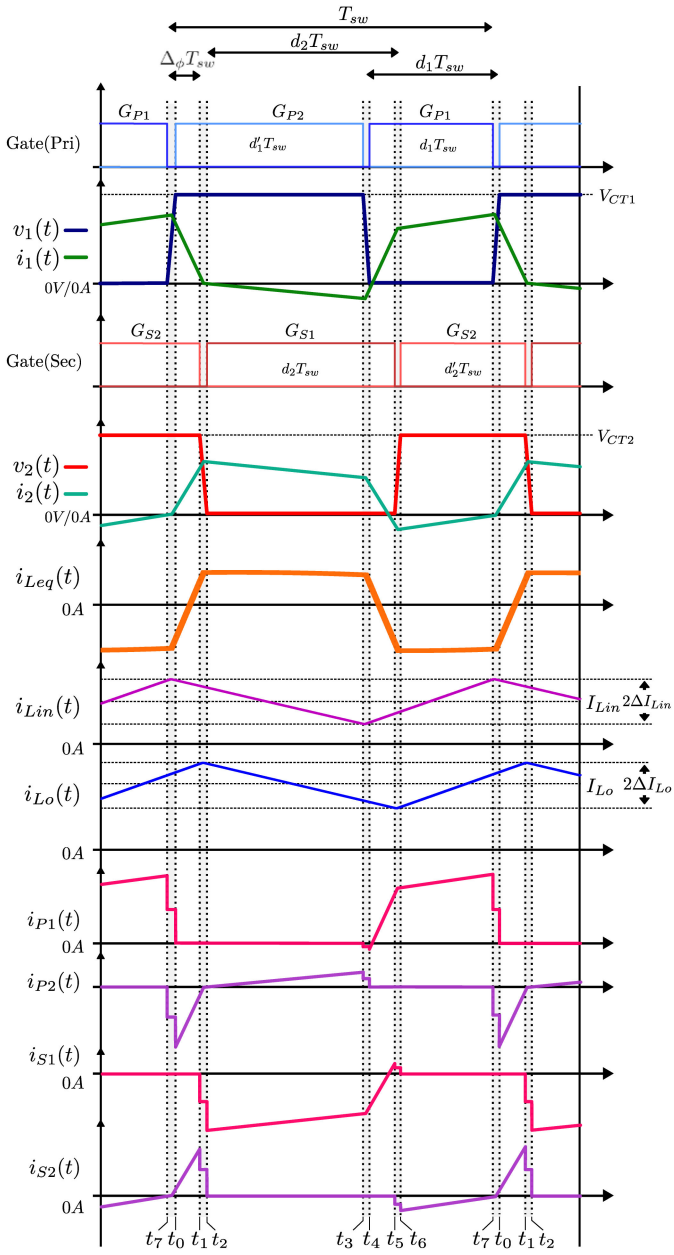

Fig. 3. Operating waveform of the proposed PAC-Ćuk converter.

At time t_1, mode M_1 ends with the removal of gate of S_{S2}. Duration of this mode, T_{M1} is given as follows:

$$T_{M1} = t_1 - t_0 = \Delta_\phi T_{\text{sw}} - (T_{T1} + T_{T4})/2 \tag{9}$$

where T_{T1} and T_{T4} are the durations of the transition modes T_2 and T_4, respectively.

Mode 2 [$t_1 < t < t_2$] (Transition mode, T_1): In this transition mode, T_1, S_{S2} is turned OFF by removing the gate signal. Turn-OFF of S_{S2} results in current $i_2(t)$ to divert from S_{S2} to S_{S1}, resulting in discharging of the output capacitance of S_{S1}, $C_{\text{oss},S1}$, and charging of the output capacitance of S_{S2}, $C_{\text{oss},S2}$. ZVS turn-ON of S_{S1} requires that the $C_{\text{oss},S1}$ is fully discharged [equivalent to $v_2(t)$ falling to zero] before the gate of S_{S1} is applied. Current $i_2(t)$ results in $v_2(t)$ to fall linearly until it is

clamped by the body diode of S_{S1} marking the end of this mode. The duration of the transition mode T_{T1} is given as follows:

$$T_{T1} = t_2 \ - \ t_1 = \frac{(C_{\text{oss},S1} + C_{\text{oss},S2})\, V_{CT2}}{i_2\,(t_1)} \tag{10}$$

$$i_2\ (t_1) = \ (I_{Lo} + \Delta I_{Lo}) + i_{L\text{eq}}\,(t_1) \tag{11}$$

where inductor current $i_{L\text{eq}}(t_1)$ is given by (8).

Mode 3 [$t_2 < t < t_3$] (Main mode, M_2): At time t_2, the body diode of S_{S1} is conducting as $i_{S1}(t)$, equal to $-i_2(t)$, is negative. The gate is applied to S_{S1} while $i_{S1}(t)$ is still negative, resulting in the turn-ON of S_{S1} under ZVS. As S_{P2} is also active, the voltage across the inductor L_{eq} is now reduced to $V_{CT1} - V_{CB1} - V_{CB2}$, which, depending on V_{CT1}, can be positive or negative. The series inductor current $i_{L\text{eq}}(t)$ is given as follows:

$$i_{L\text{eq}}\ (t) = \frac{V_{CT1} - V_{CB1} - V_{CB2}}{L_{\text{eq}}}\ (t - t_2) + i_{L\text{eq}}\,(t_2)\,. \tag{12}$$

During this mode, current $i_{P2}(t)$ equals $-i_1(t)$, whereas i_{S1} equals $-i_2(t)$. The duration of this mode T_{M2} is given as follows:

$$T_{M2} = t_3 \ - \ t_2 = (d_1' - \Delta_\phi)\, T_{\text{sw}} - (T_{T2} + T_{T1})\,/2 \tag{13}$$

where T_{T2} and T_{T1} are the durations of the transition modes T_2 and T_1, respectively.

Mode 4 [$t_3 < t < t_4$] (Transition mode, T_2): At time t_3, duty cycle of S_{P2}, $(1 - d_1)$, is elapsed and S_{P2} is turned OFF by removing the gate signal. Current $i_1(t)$ starts to discharge $C_{\text{oss},P1}$ and charge $C_{\text{oss},P2}$. The voltage $v_1(t)$ falls linearly due to current $i_1(t)$ until it reaches zero and gets clamped by the body diode of S_{P1}, marking the end of this mode. The duration of this transition mode, T_{T2}, and current $i_1(t_3)$ is given as follows:

$$T_{T2} = t_4 \ - \ t_3 = \frac{(C_{\text{oss},P1} + C_{\text{oss},P2})\, V_{CT1}}{i_1\,(t_3)} \tag{14}$$

$$i_1\ (t_3) = \ (I_{L\text{in}} + \Delta I_{L\text{in}}) - i_{L\text{eq}}\,(t_3) \tag{15}$$

where $i_{L\text{eq}}(t_3)$ is obtained using (12).

Mode 5 [$t_4 < t < t_5$] (Main mode, M_3): At time t_4, the body diode of S_{P1} is still conducting as current $i_{P1}(t)$, equal to $i_1(t)$, is still negative. Applying the gate on S_{P1} results in ZVS turn-ON of S_{P1}. As S_{P1} and S_{S1} are ON, the voltage across the inductor L_{eq} is equal to $-V_{CB1} - V_{CB2}$. The negative voltage results in fall of the inductor current $i_{L\text{eq}}(t)$ as shown in Fig. 3 and is given as follows:

$$i_{L\text{eq}}\ (t) = \frac{-V_{CB1} - V_{CB2}}{L_{\text{eq}}}\ (t - t_4) + i_{L\text{eq}}\,(t_4)\,. \tag{16}$$

The duration of this mode, T_{M3}, is given as follows:

$$T_{M3} = t_5 - t_4 = (d_1 - d_2' + \Delta_\phi)\, T_{\text{sw}} - (T_{T3} + T_{T2})\,/2 \tag{17}$$

where T_{T3} and T_{T2} are the durations of the transition modes T_3 and T_2, respectively.

Mode 6 [$t_5 < t < t_6$] (Transition mode, T_3): Current $i_{L\text{eq}}(t)$ forces the current $i_2(t)$ to become negative. At time t_5, S_{S1} is turned OFF by removing the gate signal. Current $i_2(t)$ starts to discharge capacitance $C_{\text{oss},S1}$ and charge $C_{\text{oss},S2}$. The voltage $v_2(t)$ rises linearly until it reaches V_{CT2} and gets clamped by the body diode of S_{S2}. The duration of this transition mode T_{T3} and current $i_2(t_5)$ is given as follows:

$$T_{T3} = t_6 \ - \ t_5 = \frac{(C_{\text{oss},S1} + C_{\text{oss},S2})\, V_{CT2}}{-i_2\,(t_5)} \tag{18}$$

$$i_2\ (t_5) = \ (I_{Lo} + \Delta I_{Lo}) + i_{L\text{eq}}\,(t_5) \tag{19}$$

where $i_{L\text{eq}}(t_5)$ is obtained using (16).

Mode 7 [$t_6 < t < t_7$] (Main mode, M_4): As $C_{\text{oss},S2}$ is fully discharged, the diode of S_{S2} starts to conduct at time instant t_6. While current $i_{S2}(t)$, equal to $i_2(t)$, is still negative, applying the gate on $S2$ results in ZVS turn-ON of S_{S2}. With S_{P1} and S_{S2} ON, the voltage across the series inductor L_{eq} is equal to $V_{CT2} - V_{CB1} - V_{CB2}$. Current $i_{L\text{eq}}(t)$ rises or falls in this mode according to the voltage across the inductor L_{eq} and is given as follows:

$$i_{L\text{eq}}\ (t) = \frac{V_{CT2} - V_{CB1} - V_{CB2}}{L_{\text{eq}}}\ (t - t_6) + i_{L\text{eq}}\,(t_6) \tag{20}$$

The duration of this main mode, T_{M4}, is given as follows:

$$T_{M4} = t_7 \ - \ t_6 = (d_2' - \Delta_\phi)\, T_{\text{sw}} - (T_{T4} + T_{T3})\,/2 \tag{21}$$

where T_{T4} and T_{T3} are the durations of the transition modes T_4 and T_3, respectively.

Mode 8 [$t_7 < t < t_0 + T_{sw}$] (Transition mode, T_4): At time t_7, S_{P1} is turned OFF by removing the gate signal. Current $i_1(t)$ starts to discharge the capacitance $C_{\text{oss},P2}$ and charge $C_{\text{oss},P1}$. The voltage $v_1(t)$ rises linearly till it reaches V_{CT1} and clamped by body diode of S_{P2}. The duration of this transition mode, T_{T4}, and current $i_1(t_7)$ is given as follows:

$$T_{T4} = t_0 \ + T_{\text{sw}} - t_7 = \frac{(C_{\text{oss},P1} + C_{\text{oss},P2})\, V_{CT1}}{-i_2\,(t_7)} \tag{22}$$

$$i_1\ (t_7) = \ (I_{L\text{in}} + \Delta I_{L\text{in}}) - i_{L\text{eq}}\,(t_7) \tag{23}$$

where $i_{L\text{eq}}(t_7)$ is obtained using (20).

III. Power Transfer, Circulating Current, and ZVS Analysis

In a conventional Ćuk converter, the energy is transferred from the input to the output through the blocking capacitor. In the PAC-Ćuk converter, energy is transferred via the blocking capacitor and the series inductor. The PAC-Ćuk converter has additional modes (Modes M_1 and M_3) where the ON and OFF states of the main switches S_{P1} and S_{S1} overlap, resulting in high *di/dt* limited only by the series inductor. More accurate analysis requires accounting for these overlapped modes. Also, the input and output inductor currents in the PAC-Ćuk converter are confined through either S_{P1} and S_{S1} or C_{T1} and C_{T2}, respectively, and should be considered in the converter analysis. Current $i_{L\text{eq}}(t)$ is dependent upon the voltage of the capacitors, V_{CT1}, V_{CT2}, V_{CB1}, and V_{CB2} , as given by (8), (12), (16), and (20).

Power transfer, circulating current, and ZVS analysis, which are essential for the analysis of this topology, require series inductor current states. The transition modes (T_1, T_2, T_3, and T_4)

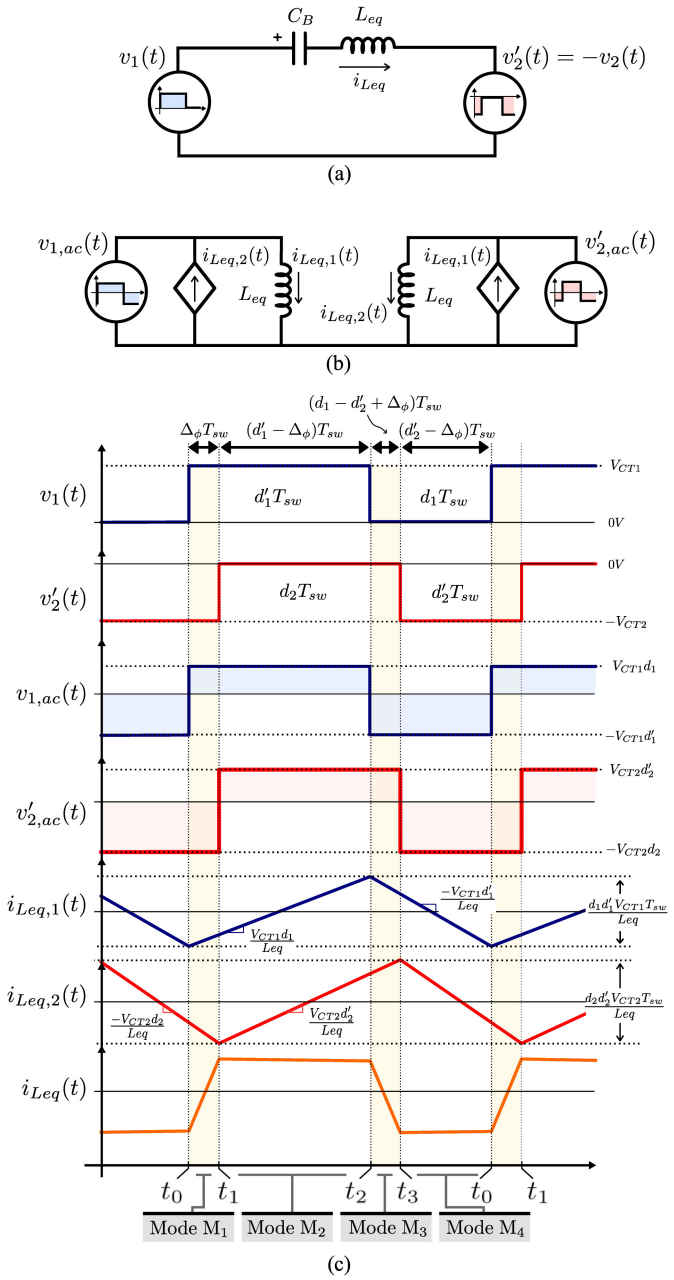

Fig. 4. Simplified model of the proposed PAC-Ćuk converter for power and circulating current analysis. (a) Primary referred circuit. (b) AC equivalent of the circuit shown in (a). (c) Waveforms associated with the circuit.

are active for an insignificant time compared to the main modes ($M_1, M_2, M_3,$ and M_4) and can be ignored in power flow and circulating current analysis. Hence, the topology is reduced to four main modes of operation, as shown Fig. 4(c). A simplified circuit is developed as depicted in Fig. 4(a) to analyze the power transfer and circulating current through the series inductor. Node voltage $v_2(t)$ referred to the primary side is denoted by $v_2'(t)$ for the unity gain transformer. C_B is the lumped blocking capacitor equivalent of series connected C_{B1} and C_{B2}. The effect of transformer magnetizing inductance L_m is ignored in the simplified circuit as magnetizing current is insignificant for $L_m \gg L_{\text{eq}}$.

Node voltages $v_1(t)$ and $v_2'(t)$ are imposed on L_{eq} and C_B as shown in Fig. 4(a). DC components of $v_1(t)$ and $v_2'(t)$ are V_{in} and $-V_o$, respectively, and are blocked by C_B. Fig. 4(b) shows the ac equivalent of the circuit shown in Fig. 4(a), which is obtained by removing the dc components of $v_1(t)$ and $v_2'(t)$. Applying the gyrator theory [9], [10], an equivalent circuit is formed by placing separate inductors L_{eq} across the two voltage sources to determine $i_{Leq}(t)$. $v_{1,\text{ac}}(t)$ and $v_{2,\text{ac}}'(t)$ produce $i_{Leq,1}(t)$ and $i_{Leq,2}(t)$, respectively, as shown in Fig. 4(b) and (c), where $i_{Leq}(t) = i_{Leq,1}(t) - i_{Leq,2}(t)$. $v_{1,\text{ac}}(t)$ and $v_{2,\text{ac}}'(t)$ for the four main modes are given as follows:

$$v_{1,\text{ac}}(t) = \begin{cases} V_{CT1}d_1 & \text{when } t_0 \le t < t_1 \quad [M_1] \\ V_{CT1}d_1 & \text{when } t_1 \le t < t_2 \quad [M_2] \\ -V_{CT1}d_1' & \text{when } t_2 \le t < t_3 \quad [M_3] \\ -V_{CT1}d_1' & \text{when } t_3 \le t < t_0 + T_{\text{sw}} \quad [M_4] \end{cases} \tag{24}$$

$$v_{2',\text{ac}}(t) = \begin{cases} -V_{CT2}d_2' & \text{when } t_0 \le t < t_1 \quad [M_1] \\ V_{CT2}d_2 & \text{when } t_1 \le t < t_2 \quad [M_2] \\ V_{CT2}d_2 & \text{when } t_2 \le t < t_3 \quad [M_3] \\ -V_{CT2}d_2' & \text{when } t_3 \le t < t_0 + T_{\text{sw}} \quad [M_4] \end{cases} \tag{25}$$

where $d_1' = 1 - d_1$ and $d_2' = 1 - d_2$.

A. Power Transfer Analysis

The output power of the PAC-Ćuk converter is equivalent to the total power transferred to $v_2'(t)$ by $i_{Leq}(t)$ and is given as follows:

$$P_o = \frac{1}{T_{\text{sw}}} \int_0^{T_{\text{sw}}} v_2'(t)\, i_{Leq}(t)\, dt = \frac{1}{T_{\text{sw}}} \int_0^{T_{\text{sw}}} \times \left(V_{2,\text{dc}}' i_{Leq}(t) + v_{2,\text{ac}}'(t)\, i_{Leq}(t) \right) dt \tag{26}$$

where $V_{2,\text{dc}}'$ is the dc component, and $v_{2,\text{ac}}'(t)$ is the ac component of $v_2'(t)$. As the average of $i_{Leq}(t) = 0$ over a switching cycle, power transferred through the dc component is zero. Simplifying (26) results in the following:

$$P_o = \frac{1}{T_{\text{sw}}} \int_0^{T_{\text{sw}}} v_{2,\text{ac}}'(t) \left(i_{Leq,1}(t) - i_{Leq,2}(t) \right) dt = \frac{1}{T_{\text{sw}}} \int_0^{T_{\text{sw}}} v_{2,\text{ac}}'(t)\, i_{Leq,1}(t)\, dt. \tag{27}$$

From (27), it can be noted that the power transferred to $v_2'(t)$ is linked to the current produced by $v_1(t)$ that flows through L_{eq}. Hence, the powers transferred within each main mode ($M_1, M_2, M_3,$ and M_4) are obtained as follows:

$$P_1 = \frac{V_{CT1}V_{CT2}d_1d_2T_{\text{sw}}}{2L_{\text{eq}}} \Delta_\phi (d_1' - \Delta_\phi) \tag{28a}$$

$$P_2 = \frac{V_{CT1}V_{CT2}d_1d'_2T_{\text{sw}}}{2L_{\text{eq}}} \Delta_\phi (d_1' - \Delta_\phi) \tag{28b}$$

$$P_3 = \frac{V_{CT1}V_{CT2}d_1'd'_2T_{\text{sw}}}{2L_{\text{eq}}} (d_2' - \Delta_\phi)(d_2 - d_1 + \Delta_\phi) \tag{28c}$$

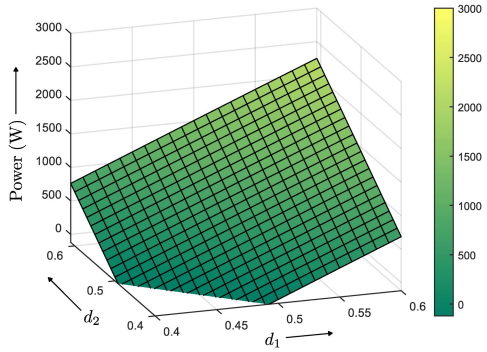

Fig. 5. Three-dimensional plot showing power transfer dependency on duty cycles (d_1 and d_2) for $V_{\text{in}} = 350$ V, $V_o = 350$ V, $L_{\text{eq}} = 200\,\mu$H, and $\Delta_\phi = 0.05$.

$$P_4 = \frac{V_{CT1} V_{CT2} d_1' d_2 T_{\text{sw}}}{2L_{\text{eq}}} (d_2' - \Delta_\phi)(d_2 - d_1 + \Delta_\phi). \tag{28d}$$

Using the above-mentioned power equations and substituting the capacitor voltage relationship from (1) and (2), total power transferred in a steady state over a switching cycle is given as follows:

$$P_o = \frac{V_{\text{in}} V_o T_{\text{sw}}}{2L_{\text{eq}}} \left(2\Delta_\phi + (d_1 + d_2 - 1) - \frac{\Delta_\phi^2}{d_1' d_2'} \right). \tag{29}$$

The power transferred during the transition modes is ignored as the duration of the transition modes is small compared to the main modes. It can be observed from (29) that the power transferred is linearly dependent upon the three control parameters . For a resistive load, the gain of the converter is obtained by substituting $P_o = V_o^2/R_L$. In a conventional Ćuk converter, the duty cycle of the main switches is complementary ($d_1 = 1 - d_2$). If conventional modulation of the Ćuk converter is implemented, the power transfer will be only the function of phase-shit ratio, Δ_ϕ. Fig. 5 shows a 3-D plot of power transferred to the output as a function of control parameters (d_1 and d_2) for a constant Δ_ϕ. Fig. 7(d)–(f) shows the impact of Δ_ϕ on the power transfer. Power transfer given by (29) is also valid for backward power flow by referring to the power and Δ_ϕ from the secondary side.

B. Circulating Current Analysis

In the PAC-Ćuk converter, ZVS turn-ON of all the switches requires circulating current through the inductor, L_{eq}. High circulating current results in higher conduction loss and, hence, should be limited while ensuring ZVS. One method to quantify the circulating current is by taking the mean square of $i_{L\text{eq}}(t)$ over a switching cycle denoted by $I^2_{L,\text{RMS}}$. Parasitic resistive elements present in the path of current $i_{L\text{eq}}(t)$ result in the conduction loss proportional to $I^2_{L,\text{RMS}}$. $I^2_{L,\text{RMS}}$ can be computed by taking the mean square inductor current in each main mode and is given as follows:

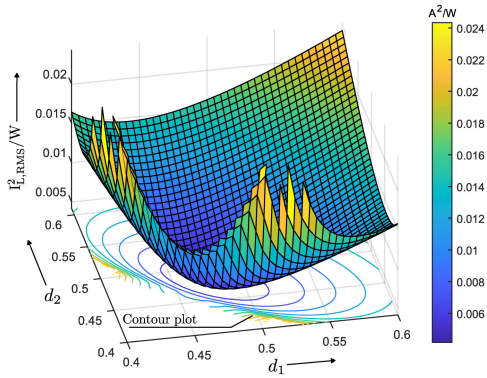

Fig. 6. Three-dimensional plot showing mean square series inductor current per Watt ($I^2_{L,\text{RMS}}/\text{W}$) dependancy on duty cycles (d_1 and d_2) for $V_{\text{in}} = 350$ V, $V_o = 350$ V, $L_{\text{eq}} = 200\,\mu$H, and phase-shift ratio $\Delta_\phi = 0.05$.

$$I^2_{L,\text{RMS}} = \frac{1}{T_{\text{sw}}} \sum_{i=1}^{4} \int_{t_{i-1}}^{t_i} i^2_{L\text{eq}}(t)\, dt \tag{30}$$

where i is the index of the main mode, M_i.

Inductor current, $i_{L\text{eq}}(t)$, is calculated using the ac equivalent circuit shown in Fig. 4. As $i_{L\text{eq}}(t)$ is linear for each main mode, it can be described as follows:

$$i_{L\text{eq}}(t) = m_i\,(t - t_{i-1}) + i_{L\text{eq}}(t_{i-1}) \tag{31}$$

where m_i is the slope of the current, $i_{L\text{eq}}(t_{i-1})$ is the initial condition of the current at the start of the ith mode. Slope m_i and initial condition $i_{L\text{eq}}(t_{i-1})$ are obtained using $i_{L\text{eq},1}(t)$ and $i_{L\text{eq},2}(t)$ as shown in Fig. 4(c) and are summarized in Table II.

The total mean square current $I^2_{L,\text{RMS}}$ over a switching cycle is obtained by using (30) and is given by (32) shown at the bottom of this page. In Fig. 6, $I^2_{L,\text{RMS}}$ normalized by power transferred is shown to provide better insight into the circulating current relation with the duty cycles d_1 and d_2 for constant phase-shift, Δ_ϕ. It can be seen from the figure that $I^2_{L,\text{RMS}}$ per unit power transferred takes a convex shape; hence, the minimum current for the required output power is found by the optimization of d_1, d_2, and Δ_ϕ. Fig. 7(d)–(f) shows the impact of Δ_ϕ on the circulating current. Increasing Δ_ϕ results in higher circulating current compared with d_1 and d_2 for high Δ_ϕ.

$$I^2_{L,\text{RMS}} = \left(\frac{T_{\text{sw}}}{L_{\text{eq}}}\right)^2 \left\{ \frac{V_o\left(12V_{\text{in}}\Delta_\phi^2 + V_o\right)}{12} + \frac{V_{\text{in}} d_1^2 (V_{\text{in}} + 4V_o)}{12} + \frac{V_{\text{in}} {d_2'}^2 (4V_{\text{in}} + V_o)}{12} \right.$$
$$\left. - \frac{V_o d_2' (V_o + 6V_{\text{in}}\Delta_\phi)}{6} - \frac{V_{\text{in}} V_o \Delta_\phi^3}{3d_2' - 3d_1 d_2'} - \frac{V_{\text{in}} V_o d_1 (3d_2' - 6\Delta_\phi + 1)}{6} \right\}. \tag{32}$$

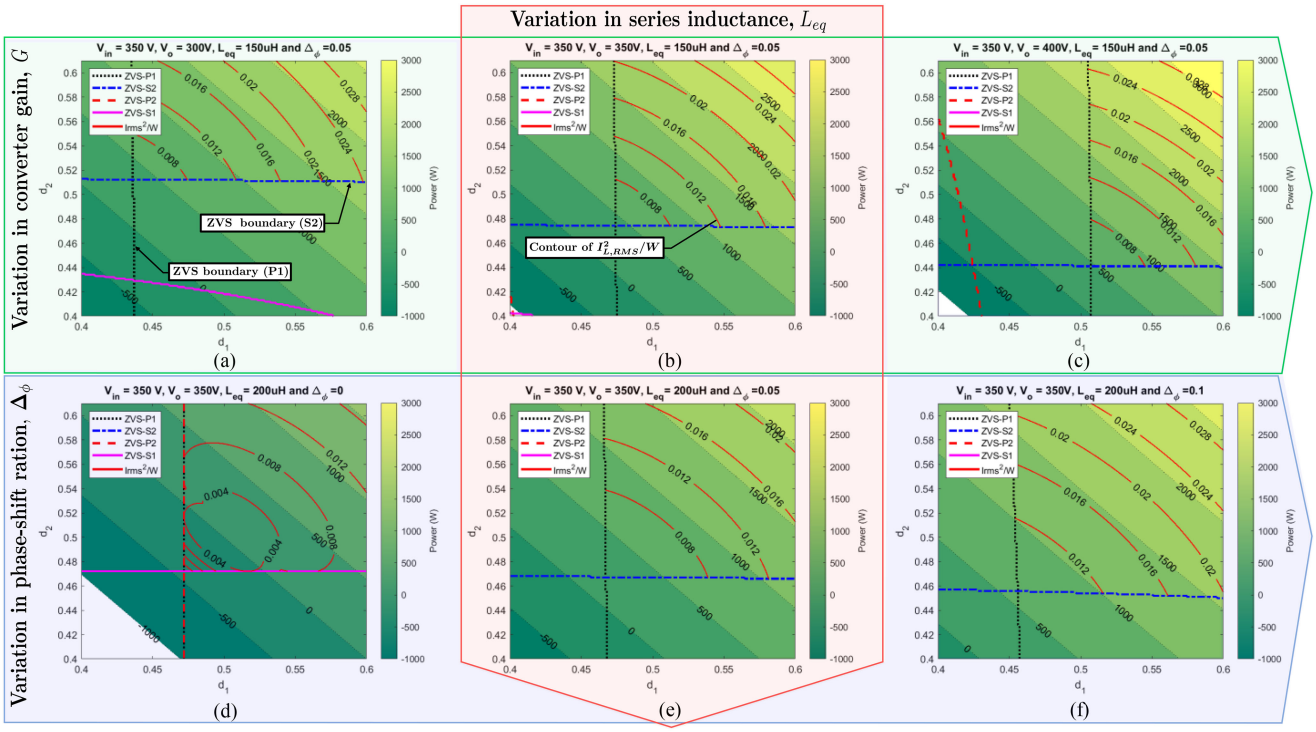

Fig. 7. Plots to depict dependency of power transfer, circulating current, and ZVS region of the PAC-Ćuk converter on different system parameters. All graphs have d_1 on the x-axis and d_2 on the y-axis. (a)–(f) Contour plots with both power transfer and mean square current per unit power along with the ZVS region for different operating conditions.

TABLE II
SERIES INDUCTOR CURRENT EQUATION FOR EACH MODE

Main mode	Slope of the current $i_{Leq}(t)$ for ith mode	Initial current at the start of the ith mode
M_1	$m_1 = (V_{CT1}d_1 + V_{CT2}d_2)/L_{eq}$	$i_{Leq}(t_0) = \left(-0.5d_1d_1'V_{CT1} - 0.5d_2d_2'V_{CT2} + (d_2' - \Delta_\phi)d_2V_{CT2}\right)T_{sw}/L_{eq}$
M_2	$m_2 = (V_{CT1}d_1 - V_{CT2}d_2')/L_{eq}$	$i_{Leq}(t_1) = \left(-0.5d_1d_1'V_{CT1} + \Delta_\phi d_1V_{CT1} + 0.5d_2d_2'V_{CT2}\right)T_{sw}/L_{eq}$
M_3	$m_3 = (-V_{CT1}d_1' - V_{CT2}d_2')/L_{eq}$	$i_{Leq}(t_2) = \left(0.5d_1d_1'V_{CT1} + 0.5d_2d_2'V_{CT2} - (d_1' - \Delta_\phi)d_2'V_{CT2}\right)T_{sw}/L_{eq}$
M_4	$m_4 = (-V_{CT1}d_1' + V_{CT2}d_2)/L_{eq}$	$i_{Leq}(t_3) = \left(0.5d_1d_1'V_{CT1} - (d_1 - d_2' + \Delta_\phi)d_1'V_{CT1} - 0.5d_2d_2'V_{CT2}\right)T_{sw}/L_{eq}$

C. ZVS Condition

ZVS turn-ON requires complete discharging of the output capacitance (C_{oss}) of the switch turning-ON and complete charging of the C_{oss} of the switch turning-OFF within the deadband t_{db} [32], [33]. C_{oss} is assumed to be constant, whereas t_{db} between the gates of the complementary switches is taken as constant for all switches in this article. The deadband t_{db} between the complimentary switches should be larger than the switching transition time (as discussed in Section II) to achieve full ZVS turn-ON of the switches. Minimum threshold current through the switch, which can charge and discharge the output capacitance of the switches before t_{db} elapse, is given by the following equation:

$$i_{ZVS,min} = 2C_{oss}V_{DS}/t_{db} \tag{33}$$

where V_{DS} is the voltage across the switch that is turning OFF. Conditions on current $i_{Leq}(t)$ required to ensure enough current through the switches at the time of transition for ZVS turn-ON are obtained using Fig. 4 and are given as follows:

$$i_{Leq}(t_2) > (I_{in} - \Delta I_{in}) + 2C_{oss}V_{CT1}/t_{db}\ [\text{ZVS } S_{P1}] \tag{34a}$$

$$i_{Leq}(t_0) < (I_{in} + \Delta I_{in}) - 2C_{oss}V_{CT1}/t_{db}\ [\text{ZVS } S_{P2}] \tag{34b}$$

$$i_{Leq}(t_1) > -(I_o + \Delta I_o) + 2C_{oss}V_{CT2}/t_{db}\ [\text{ZVS } S_{S1}] \tag{34c}$$

$$i_{Leq}(t_3) < -(I_o - \Delta I_o) - 2C_{oss}V_{CT2}/t_{db}\ [\text{ZVS } S_{S2}] \tag{34d}$$

where $i_{Leq}(t_i)$ at the time of transition is obtained from Table II. Conditions for ZVS turn-ON of switches S_{P2} and S_{S1} are easily achievable as $i_{Leq}(t_0) < (I_{in} + \Delta I_{in})$ and $i_{Leq}(t_1) > -(I_o + \Delta I_o)$ are generally satisfied and can be verified using Table II. However, ZVS turn-ON of S_{P1} and S_{S2} requires proper selection of d_1, d_2, and Δ_ϕ. Using (4), (5), (29), (34a), (34c), and Table II, an analytical expression for the ZVS turn-ON conditions

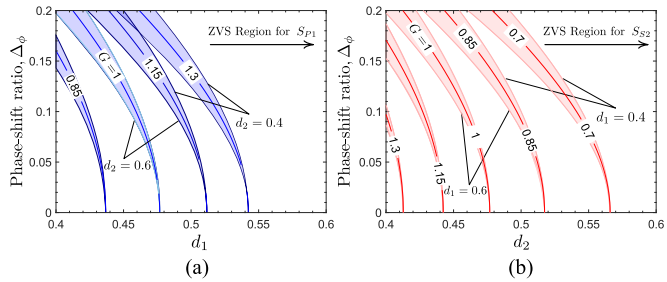

Fig. 8. ZVS turn-ON boundary condition of (a) switch S_{P1} and (b) switch S_{S2} as a function of control parameters: duty cycles (d_1, d_2) and phase-shift ratio Δ_ϕ for varying converter gain, G.

of S_{P1} and S_{S2} is determined to be

$$d_{1,\text{ZVS}(P1)} > \frac{\left(\frac{G}{L_{\text{eq}}}\left(1-\frac{\Delta_\phi^2}{d_1' d_2'}\right)\right)+\frac{4C_{\text{oss}}}{d_1' t_{\text{db}} T_{\text{sw}}}}{\left(\frac{G+1}{L_{\text{eq}}}+\frac{1}{L_{\text{in}}}\right)} \tag{35a}$$

$$d_{2,\text{ZVS}(S2)} > \frac{\left(\frac{1}{L_{\text{eq}}}\left(1-\frac{\Delta_\phi^2}{d_1' d_2'}\right)\right)+\frac{4C_{\text{oss}}}{d_2' t_{\text{db}} T_{\text{sw}}}}{\left(\frac{G+1}{L_{\text{eq}}}+\frac{G}{L_o}\right)} \tag{35b}$$

where $G\ (=V_o/V_{\text{in}})$ is the converter gain. It can be seen from (35) that the ZVS boundary for S_{P1} is nearly decoupled from d_2 and for S_{S2}, it is nearly decoupled from d_1. Fig. 8 shows the plot of the ZVS boundary for S_{P1} and S_{S2} for various G values. With the increasing G, the ZVS boundary condition of S_{P1} $d_{1,\text{ZVS}(P1)}$ decreases, whereas for S_{S2}, $d_{2,ZVS(S2)}$ increases [also shown in Fig. 7(a)–(c) as V_o is increasing]. It can also be noted from Fig. 8 that increasing the Δ_ϕ provides more room for ZVS operation but with an increase in circulating current as discussed previously. An increase in the phase-shift ratio also results in more coupling between ZVS boundary conditions, $d_{1,ZVS(P1)}$ and $d_{2,ZVS(S2)}$, as shown in Fig. 8 by the shaded region, making the boundary condition more complex.

IV. Design Consideration

A. Hardware Design

ZVS operation of the PAC-Ćuk converter over a wide output power and voltage range requires proper selection of the passive components based on the control parameter range. The dependence of power transfer, circulating current, and ZVS condition on passive components is evident from (29), (32), and (35), respectively. Hence, proper selection of the components is important and is discussed in detail below.

MOSFET selection: The maximum voltage across S_{P1} and S_{P2} is clamped by the auxiliary capacitor C_{T1}, whereas for S_{S1} and S_{S2}, it is clamped by C_{T2}. Hence, the maximum voltage across these capacitors will dictate the voltage ratings of the switches. For the maximum input voltage and the maximum d_1, the maximum voltage across S_{P1} and S_{P2} can be deduced using (1). Similarly, the maximum voltage across S_{S1} and S_{S2} is obtained using (2). Absolute peak currents through the switches $(S_{P1},\ S_{P2})$ and $(S_{S1},\ S_{S2})$ are given by (36) from the turn-OFF current through the switches at the end of the main modes M_1 and M_2

$$i_{P1,\max} = i_{P2,\max} = \left|(I_{\text{in},\max}+\Delta I_{\text{in}}) - i_{L\text{eq},\max}(t_0)\right| \tag{36a}$$

$$i_{S1,\max} = i_{S2,\max} = \left|(I_{o,\max}+\Delta I_o) - i_{L\text{eq},\max}(t_1)\right|. \tag{36b}$$

Equivalent series inductance, L_{eq}: Inductance L_{eq}, which is equivalent to $L_r + L_{\text{lk}}$, plays a vital role in power transfer and producing the circulating current necessary for the ZVS turn-ON of the switches. Power transfer and the circulating current through the inductor are both inversely proportional to L_{eq} as given in (29) and (32). The design objective for L_{eq} is to choose the inductance that satisfies the minimum load requirement for a small constant phase-shift ratio with ZVS turn-ON. Fig. 7(b) and (e) shows the effect of increasing the series inductance, resulting in lower power output and lower mean square circulating current per Watt for the same modulation conditions. Minimum condition for L_{eq} is given as follows:

$$L_{\text{eq}} > \frac{V_{\text{in}} V_o T_{\text{sw}}}{2P_{\min}}\left(2\Delta_\phi + d_{1,\text{ZVS}} + d_{2,\text{ZVS}} - 1 - \frac{\Delta_\phi^2}{d'_{1,\text{ZVS}} d'_{2,\text{ZVS}}}\right) \tag{37}$$

where $P_{\min}$ is the minimum required output load and $d_{1,\text{ZVS}}$ and $d_{2,\text{ZVS}}$ are the ZVS boundary constraints on duty cycles given by (35) for a constant Δ_ϕ.

Input and output inductors, L_{in} and L_o: As in the case of designing a conventional Ćuk converter, input and output inductors are chosen as per ripple requirements. However, higher inductor current ripple over the inductors assists in ZVS operation and is preferred, as evident from ZVS boundary constraints.

Auxiliary capacitors, C_{T1} and C_{T2}: The auxiliary capacitor C_{T1} is chosen to make sure that the resonance period of the circuit formed by C_{T1}, C_{B1}, C_{B2}, and L_{eq} is much greater than the maximum duration of the main mode (M_2). Similarly, auxiliary capacitor C_{T2} should be large enough that the resonance period of the circuit formed by C_{T2}, C_{B1}, C_{B2}, and L_{eq} is much greater than the maximum duration of the main mode (M_4). Conditions (38) and (39) can be used to select the auxiliary capacitor as it ensures a small deviation from the linear analysis presented in this article

$$(1-d_{1,\max}-\Delta_\phi)\,T_{\text{sw}} \ll 2\pi\sqrt{L_{\text{eq}}\left(C_{T1}\|C_{B1}\|C_{B2}\right)} \tag{38}$$

$$(1-d_{2,\max}-\Delta_\phi)\,T_{\text{sw}} \ll 2\pi\sqrt{L_{\text{eq}}(C_{T2}\|C_{B1}\|C_{B2})} \tag{39}$$

where $d_{1,\max}$ and $d_{2,\max}$ are the maximum allowable duty cycles, limited by the capacitor and switch voltage ratings.

B. Control Parameter

The PAC-Ćuk converter has three control parameters, including d_1 and d_2 and Δ_ϕ. An operating condition is achieved using a combination of these three control parameters. The choice of parameters for a given operation can be made based on the required objective. In this article, the objective is to minimizing the circulating current by optimizing the duty cycles for a constant Δ_ϕ.

Phase-shift ratio, Δ_ϕ: The phase between the two duty cycles is responsible for circulating current, which assists in achieving

ZVS turn-ON of the switches. A higher phase-shift ratio Δ_ϕ results in higher power flow but also increases circulating current. It also extends the ZVS region, but at the cost of higher circulating current losses, as shown in Fig. 7(d)–(f). In this article, a constant phase-shift ratio is considered for design and operation, where smaller phase-shift results in an overall minimal circulating current for varying duty cycles. As power transfer is dependent upon control parameters (duty cycles $d_1$andd_2 and Δ_ϕ) and the voltage across the device is dependent on the duty cycle, when the duty cycle cannot be increased due to an allowable voltage constraint, Δ_ϕ is increased at the cost of higher circulating current.

Duty cycles, d_1 and d_2: With the phase-shift ratio Δ_ϕ held constant, the minimum duty cycles $d_{1,\min}$ and $d_{2,\min}$ are set by ZVS boundary constraint (35), whereas the maximum duty cycles $d_{1,\max}$ and $d_{2,\max}$ are limited by the voltage rating of switches and auxiliary capacitors as given by (1) and (2). Increase in either d_1 or/and d_2 also results in higher power transfer, as given by (29). However, an optimal relation between the duty cycles is required to achieve the minimal circulating current for a chosen Δ_ϕ.

Optimization between duty cycles, d_1 and d_2: According to the Lagrange multiplier method, a common normal to both the contours (I^2_{rms}/W and power, P_o) can provide a relationship between duty cycles d_1 and d_2, which results in the minimum circulating current $I^2_{L,\text{RMS}}$ for a constraint on power P_o and is given as follows:

$$\frac{\partial I^2_{\text{rms}}}{\partial d_1} = \lambda \frac{\partial P_o}{\partial d_1} \tag{40a}$$

$$\frac{\partial I^2_{\text{rms}}}{\partial d_2} = \lambda \frac{\partial P_o}{\partial d_2} \tag{40b}$$

$$P_o = P_c \tag{40c}$$

where λ is the Lagrange multiplier and P_c is the constraint for the required output power. Using (29) and (32), the relationship between the duty cycles with the objective of minimal circulating current for a small constant Δ_ϕ is found and given as follows:

$$d_1 \approx G d_2 \tag{41}$$

where G is the gain of the converter. This relation can be interrupted in the sense that the PAC-Ćuk converter is a symmetric converter. Gain G creates voltage inequality in the symmetry and is accounted for by (41) through auxiliary capacitor voltages, reducing the circulating current. Also, this relation helps to distribute the voltage stress on the switches. A higher gain results in a smaller duty cycle on secondary main switch d_2, which, in turn, reduces the voltage stress on the switch.

V. Hardware Results

A 2-kW rated hardware prototype is designed for the validation of the work outlined in the earlier sections. Table III lists the parameters of the hardware prototype, and a detailed design process of the prototype is given in the Appendix. The TDK EE 65 N27 cores are used for the input inductor and the output inductor, and the transformer is used for the desired design parameter. The size of the required external inductor L_r is reduced by adopting nonconcentric primary and secondary windings for the transformer.

TABLE III
Design Parameters of the Prototype Converter

Parameter	Value
V_{in}	350 V
V_o	245 – 455 V
L_{lk}	170 μH
L_r	30 μH
L_{in}, L_o	1 mH
L_m	1.92 mH
C_{T1}, C_{T1}	3.8 μF
C_{B1}, C_{B1}	3.8 μF
C_{in}, C_o	2 μF
P_1, P_2, S_1, S_2	UF3C120040K4S
Switching frequency f_{sw}	40 kHz
$d_{1,max}$, and $d_{2,max}$ at G =1	0.6

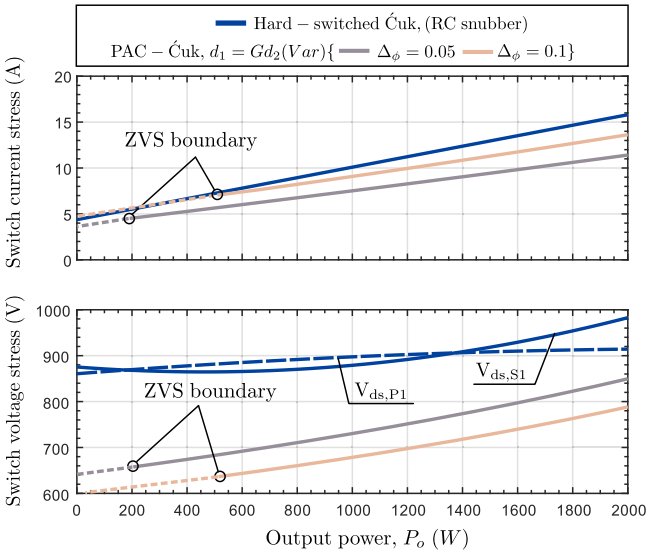

Fig. 9. Comparison of voltage and current stresses on switches for the *RC* snubber ($R = 50\ \Omega$ and $C = 2.2$ nF)-based isolated Ćuk converter with the proposed PAC-Ćuk converter when $V_{\text{in}} = V_o = 350$ V.

A comparison of peak voltage and peak current stresses on the switches for the designed prototype is shown in Fig. 9 using simulation. Converter gain of $G = 1$ is used for which the nominal voltage across the primary- and secondary-side switches is the same due to symmetry. A comparison of the proposed modulation scheme for the PAC-Ćuk converter and the hard-switched Ćuk converter with an *RC* snubber is also shown in the figure with variations in the output power. A separate transformer with the same magnetic core and number of turns as used for the PAC-Ćuk converter was built for the hard-switched converter to determine the leakage inductance. The secondary winding is sandwiched between the primary winding to attain a low leakage inductance of $L_{\text{lk}} = 4.5\ \mu$H. The *RC* snubber are tuned to limit the v_{ds} overshoot to the maximum allowed voltage. For the proposed optimized modulation using duty cycles to control the output power, the voltage stress increases whereas the current stress decreases for the increase in Δ_ϕ, as shown in the figure. In comparison to the *RC*-snubber-based isolated Ćuk converter, the peak voltage and current stresses are observed to be lower for the proposed modulation on the PAC-Ćuk converter.

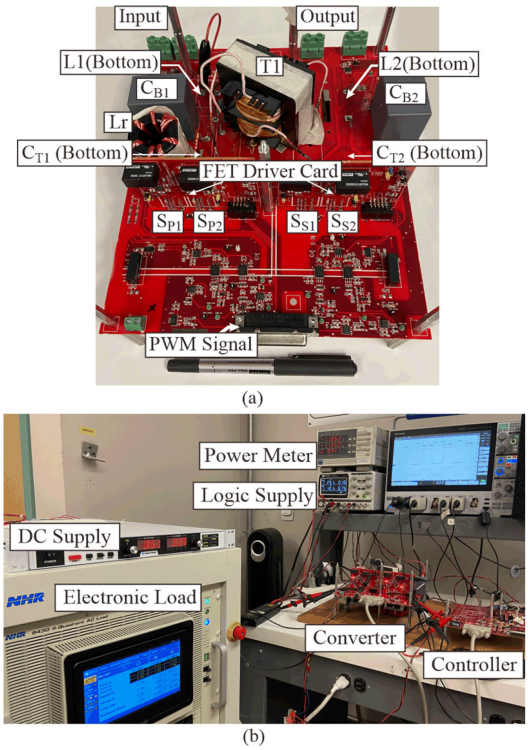

Fig. 10. Photograph of the (a) 2-kW hardware prototype and (b) test bench.

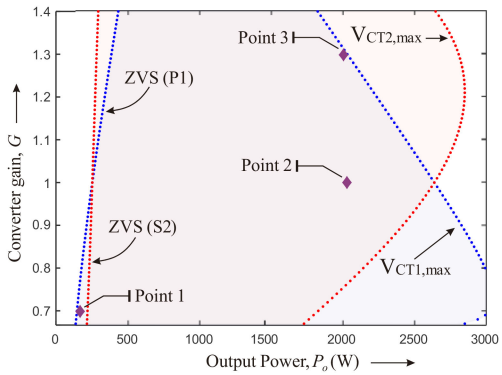

Fig. 11. Operating region for minimum circulating current condition ($d_1 = Gd_2$) of the designed hardware with $\Delta_\phi = 0.05$.

Fig. 10 shows the photograph of the hardware prototype and the test bench. A digital power meter, WT230 from Yokogama, is used to measure the efficiency of the converter. A digital controller, TMS320F28379D from Texas Instruments, is used to generate the required PWM signal. An electronic load from NHR research is used in the CV mode to operate the converter at the output power for the desired converter gain. The output power flow is controlled using the duty cycles d_1 and d_2, where $d_1 = Gd_2$.

Fig. 11 shows the ideal allowed region of operation of the designed prototype for minimum circulating current constraint, $d_1 = Gd_2$ obtained from (41). The ZVS constraint for S_{P1} and S_{S2} limits the minimum output power set by (37), whereas the voltage rating limit of the components defined by $V_{CT1,\max}$ and $V_{CT2,\max}$ limits the maximum output power.

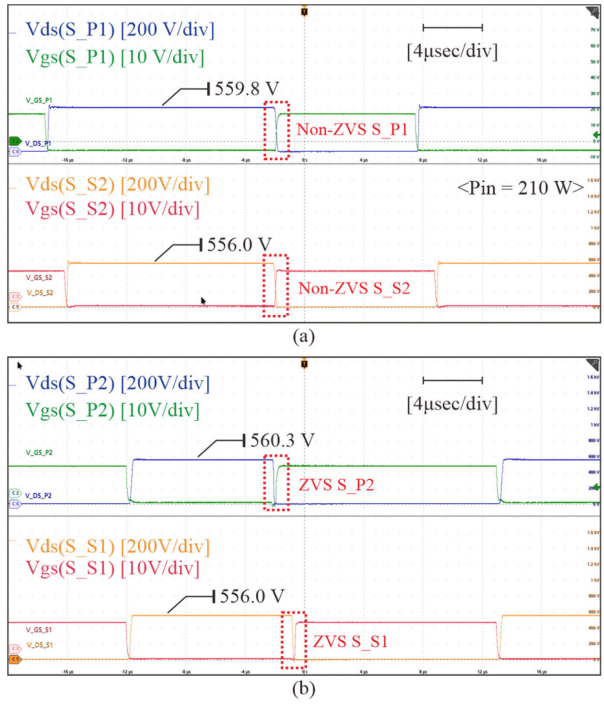

Fig. 12. Experimental verification of ZVS turn-ON of (a) S_{P1} and S_{S2}, and (b) S_{P2} and S_{S1}, for point 1: Gain $G = 0.7$ and $P_{\text{in}} = 210$ W.

The ZVS operation of all the active switches of the designed hardware prototype is shown for three operating points as marked in Fig. 11. For operating point 1, as shown in Fig. 12, switches S_{P1} and S_{S2} are losing ZVS turn-ON, which is in agreement with the ZVS constrain shown in Fig. 11. For operating points 2 and 3 (see Figs. 13 and 14, respectively), ZVS turn-on of all switches can be observed as the drain–source voltage, v_{ds}, falls to 0 V before the gate, v_{gs}, is applied, confirming the ZVS turn-ON of the switches. The drain-to-source voltages of devices are also marked in the figures and are observed to satisfy the auxiliary capacitor voltages given by (1) and (2).

The power transfer relation given by (29) and the rms of series inductor current $I_{L,\text{rms}}$ given by the square root of (32) are compared with the experimental data shown in Fig. 15 for validation for unity-gain operation. The maximum percentage error on output power is 2.5%, whereas the maximum error for $I_{L,\text{rms}}$ is 7.5%. As the analysis for power transfer and circulating current was derived for ideal passive components, the experimental data are within reasonable error. The discrepancy can be accounted for by parasitic resistance of the components and the variation of series inductance with different bias currents.

The prototype efficiency under different gains is shown in Fig. 16. The proposed modulation is used to control the output power flow by increasing d_1 and d_2 while keeping Δ_ϕ at 0.05. The duty cycle of the secondary-side switch is defined by (41) for the minimum circulating current. The efficiency for a gain of 1.3 is observed to be higher for higher loads owing to smaller conduction losses in comparison to the power transferred. The measured peak efficiency is 97.8% when gain $G = 0.7$, whereas the overall efficiency for the designed prototype converter is above 96% for 20% to full load over a wide gain (0.7–1.3).

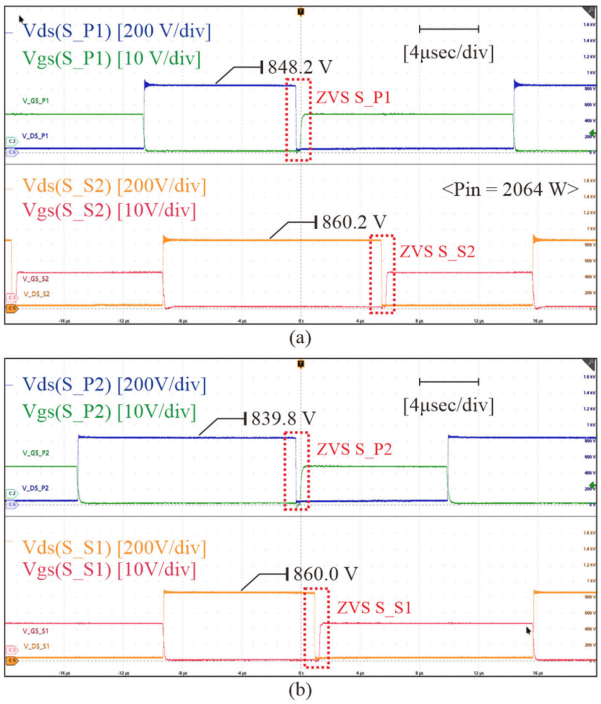

Fig. 13. Experimental verification of ZVS turn-ON of (a) S_{P1} and S_{S2}, and (b) S_{P2} and S_{S1}, for point 2: Gain $G = 1.0$ and $P_{\text{in}} = 2064$ W.

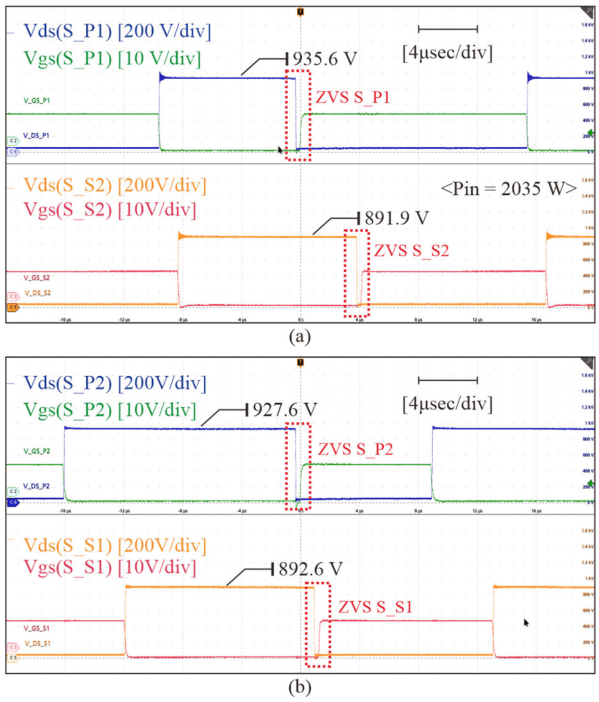

Fig. 14. Experimental verification of ZVS turn-ON of (a) S_{P1} and S_{S2}, and (b) S_{P2} and S_{S1}, for point 3: Gain $G = 1.3$ and $P_{\text{in}} = 2035$ W.

The converter was not operated till 2 kW for lower gain due to the saturation limit of the output inductor. Fig. 17(a) shows the estimated loss distribution of the prototype at an output power of 2 kW and at unity gain, whereas Fig. 17(b) shows the thermal image of the switches, which are located at the bottom of the converter. Due to ZVS turn-ON, the switching losses are significantly reduced. Low losses on the switches as shown in Fig. 17(a) enables the use of low form factor heat-sink, resulting in the switch temperature rise to 47 °C. For the designed magnetics, more than half of the losses are incurred in L_r and T_1, resulting in hotspots of 78 °C and 62 °C, respectively, at rated power.

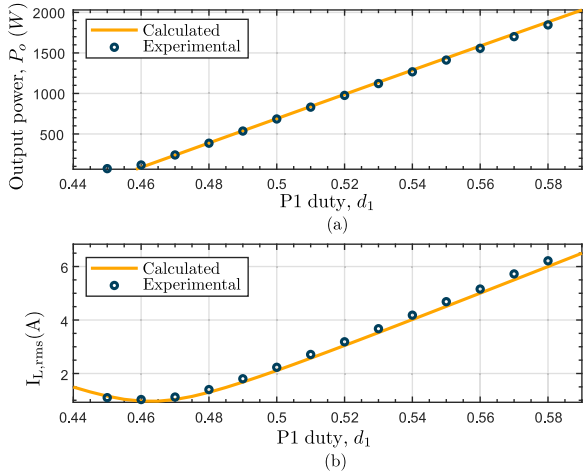

Fig. 15. Comparison of calculated and experimental data for (a) output power P_o, (b) series inductor current, $I_{L,\text{rms}}$, using the proposed optimized modulation ($d_1 = Gd_2$) for $\Delta_\phi = 0.05$ and unity gain ($V_{\text{in}} = V_o = 350$ V).

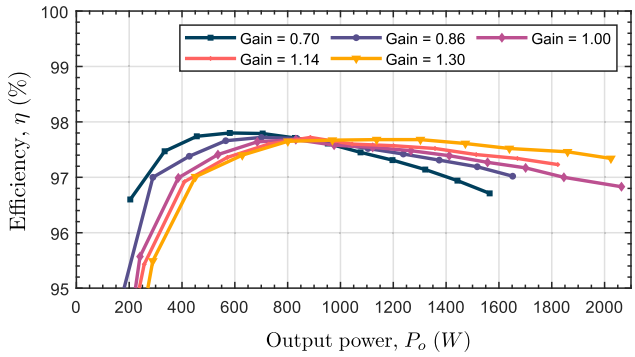

Fig. 16. Measured efficiency versus output power for various gains with constant input voltage $V_{\text{in}} = 350$ V and $\Delta_\phi = 0.05$

The proposed modulation is optimized to minimize the circulating current through L_{eq} for constant output power. The power transfer given by (29) for $d_1 + d_2 = k$ becomes nearly independent from the duties for a constant, k. The d_1 and d_2 at which $I_{L,\text{rms}}$ is minimum with $d_1 + d_2 = k$ are the optimized duties for that output power. In Fig. 18(a), three different output power cases with unity gain are presented, where circulating inductor current $I_{L,\text{rms}}$ normalized by output power is measured against $d_1, (d_2 = k - d_1)$ for different k values. The experimental data prove that the proposed modulation ($d_1 = Gd_2$) operates the converter with minimal circulating current for a wide power range. Fig. 18(b) shows the efficiency comparison of the conventional modulation (as used in [23]–[25] and [27]) and the proposed modulation over the output power. ZVS is ensured in both the modulation cases to provide a fair comparison. As discussed earlier, the conventional modulation $(d_2 = 1 - d_1)$

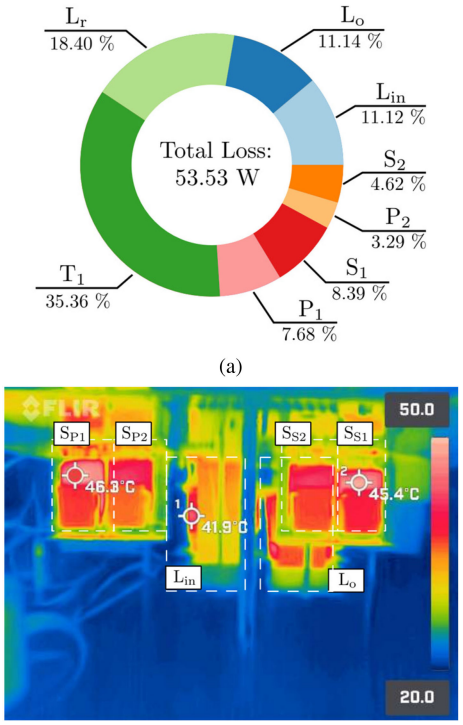

Fig. 17. 2-kW unity gain operation of the converter. (a) Projected loss distribution. (b) Thermal image of the switches.

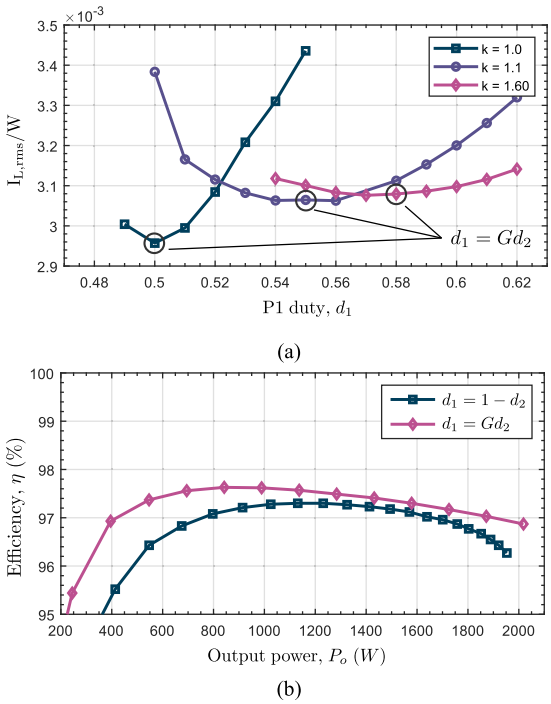

Fig. 18. Experimental data showing (a) circulating inductor current $I_{L,\text{rms}}$ normalized by output power for $d_1 + d_2 = k$ to validate the proposed optimized modulation ($d_1 = Gd_2$). (b) Efficiency comparison between the proposed modulation and the conventional modulation ($d_1 = 1 - d_2$) of the PAC-Ćuk converter.

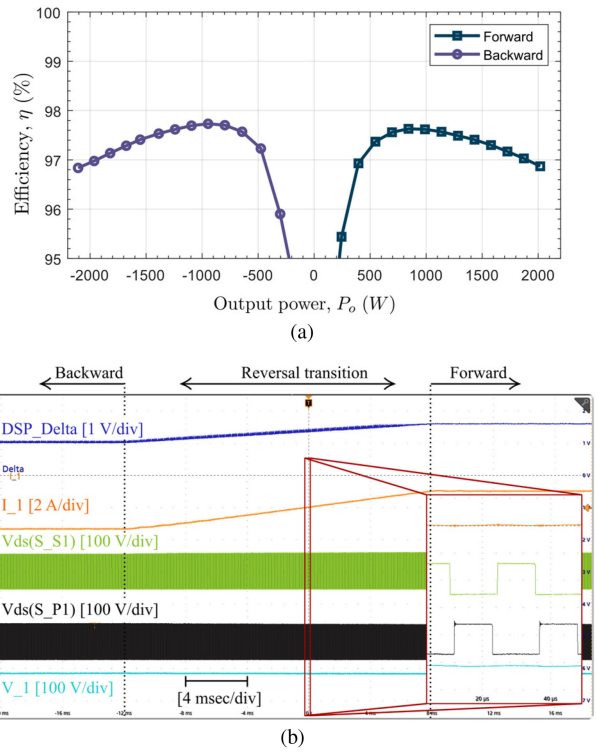

Fig. 19. Experimental results for (a) comparison of forward and backward power flow and efficiency for $\Delta_\phi = 0.05$ and unity gain and (b) transition from backward to forward power flow by changing Δ_ϕ reference from backward to forward with a rate limiter. Orange trace is the current entrying the converter, I_{in}, through the input port, light blue is the voltage at the input port, V_{in}, and blue trace is the digital to analog converter (DAC) ouput of digital signal processor (DSP) indicating PWM phase-shift.

does not provide output power control through the duties. Hence, Δ_ϕ varies for the conventional modulation. The proposed modulation offers better efficiency than the conventional modulation, as shown in the figure. The difference is more prominent for low- and full-load conditions. The efficiency for conventional modulation drops rapidly near full-load condition due to high Δ_ϕ, which results in a steep rise in circulating current.

The PAC-Ćuk converter is symmetric, and the power flow can be reversed by generating Δ_ϕ referred to the power delivery side of the main switch. By generating $\Delta_\phi = 0.05$ for both forward and backward power flows, the bidirectional efficiency plot of the converter is obtained as shown in Fig. 19(a) for unity gain. The efficiency plot is near symmetric along the y-axis due to the converter symmetry. In Fig. 19(b), the converter transition from backward to forward is shown at derated input voltage of 100 V using unidirectional sources and loads. Δ_ϕ is gradually shifted from backward to forward, as shown by the blue trace in the figure. During backward flow, current I_{in} is negative at -1.21 A and gradually increases to 1.09 A at the end of the power reversal transition period. The voltage across the switches remains stable during the transition while maintaining ZVS turn-ON as shown in the zoomed snippet at the zero-crossing of the current, showcasing smooth power reversal transition.

VI. Conclusion

This article proposes a novel modulation scheme for an isolated dc/dc PAC-Ćuk converter for a wide voltage range application. Using the leakage of the isolation transformer, the proposed scheme provides three control parameters, i.e., primary-side main switch duty cycle d_1, secondary-side main switch duty cycle d_2, and the phase-shift ratio between the two switches, Δ_ϕ. A new model of PAC-Ćuk to find the output power transfer, circulating current, and ZVS region of the converter as a function of these control parameters was derived and validated through experimental data. The optimality between duty cycles to minimize the circulating current through the series inductor is also discussed and verified through experiment. As ZVS turn-ON is essential to achieve high efficiency on the converter, ZVS conditions were analyzed and experimentally validated. From the analysis, it is observed that the optimality between the duty cycles and the ZVS constraints is simple to compute for the proposed converter. Finally, a 2-kW prototype with an input voltage of 350 V was demonstrated over wide load conditions for an output voltage range of 245–455 V. The converter achieved a peak efficiency of 97.8% for an output voltage of 245 V while maintaining a flat efficiency curve for 20% or more of the rated power operation.

Appendix
Design Process of the Prototype

Required design specification for the prototype:

$$P_{\text{max}} = 2\text{kW}, P_{\text{min}} = 400\ \text{W}, V_{\text{in}} = 350\ \text{V}\ , f_{\text{sw}} = 40\ \text{kHz}, t_{\text{db}} = 0.03T_{\text{sw}}, \text{and}\ G = 1.$$

Using (4) and (5), the input and output inductors are selected at 1 mH for 50% ripple condition in a full-load operation. As the input voltage is 350 V and the maximum output voltage is 455 V for gain of 1.3, 1200 V-rated MOSFETs are chosen for switches S_{P1}, S_{P2}, S_{S1}, and S_{S2}. UF3C120040K4S is used as the choice of MOSFET, which has $C_{\text{oss}} = 280$ pF. The minimum duty cycles with ZVS $d_{1,\text{ZVS}}$ and $d_{2,\text{ZVS}}$ are dependent on L_{eq}, and iterations using (35) and (37) are used to select L_{eq} for the required minimum output power with ZVS for $\Delta_\phi = 0.05$. $L_{\text{eq}} = 200\ \mu$H is obtained, satisfying the minimum output power under the ZVS constraint with $d_{1.\text{ZVS}} = d_{2.\text{ZVS}} = 0.4705$. The maximum allowable duty cycle is dictated by the voltage rating of the device and the auxiliary capacitors as given by (1) and (2). Setting the allowable voltage to 950 V, maximum duty cycles $d_{1,\text{max}}$ and $d_{2,\text{max}}$ are equal to 0.63. Using (38) and (39), assuming $C_{B1} = C_{B2} = C_{T1} = C_{T2} = C_x$, and taking the maximum duration of mode to be 8 times the resonance period, we have, $C_{x,\text{cal}} = 3.43\ \mu$F. For these capacitors, film capacitor C4AQNLW4380M34J of 3.8 μF is used, which has a rated voltage of 1 kV.

Acknowledgment

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