High-Power Design Challenges for Differential-Mode EV Universal Battery Supercharger

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***Abstract*—Rapid widespread vehicle electrification has incentivized fast chargers to improve their performances. In this article, an integrated-magnetic-based differential-mode Ĉuk rectifier (IM-DMCR) as a universal battery supercharger is introduced. The design challenges associated with the high-power operation of IM-DMCR are outlined, and optimized solutions are presented. A SiC-based full-scale 60-kW experimental prototype for the IM-DMCR is built and tested to verify the design.**

***Index Terms*—DC-fast charger, differential-mode ĉuk rectifier, integrated magnetics, SiC, universal battery supercharger (UBS).**

I. Introduction

ELECTRIFICATION of the transportation systems has gained significant momentum over the past few years [1], [2]. This is influenced by environmental concerns [3] and enabled by significant advances in the field of power electronics. Transportation electrification has a great potential to aid the ongoing global efforts to reduce carbon emissions. However, it has a unique set of challenges that need to be overcome before transitioning to electric vehicles (EV).

Although significant strides have been made to improve the EV range, it is not yet competitive with gasoline-powered vehicles [4]. The cost of EVs is also not on par with its gasoline-powered counterpart. Furthermore, battery-charging time is much higher compared with filling a tank of gas. The state-of-the-art for commercial EV charger has been studied in several publications [2], [4]–[6], and to solve several pending challenges, the trend is toward realizing high-power chargers using wide-bandgap (WBG) devices (such as SiC FETs) to deliver the same amount of energy to the battery in a shorter span of time.

The emerging maturity of SiC devices in recent years has accelerated the high-power converter utilization in industrial design. To effectively substitute SiC in high-power designs, specific features, such as high di/dt and dv/dt, characterization of the device, thermal considerations, and passive components design, need to be recognized and addressed in a power-electronic system (PES). Different aspects of these challenges are studied in detail, and a wide range of solutions is proposed [7]–[19]. Fast transition of switch voltage and current reduces the switching loss and thermal requirements; however, it, in turn, causes current and voltage oscillation due to parasitic capacitance and inductance in the circuit. One way to address this challenge is in the gate driver by slowing down the device passively or actively during the fast transitions [8], [20], [21]. Alternatively, the printed circuit board or the bus bar parasites can be optimized and mitigated to enhance the high speed behavior [7], [9], [10], [14]. The device module needs to be characterized due to its internal parasitic impedance and determine the safe operation area. Double pulse (DP) test is the standard method to characterize module's switching behavior under a variety of operational conditions [22]–[24].

Passive components in a battery charger need to rise to the performance level of the SiC device operating at high power/high frequency. The plurality of design and optimization techniques are proposed to condition the circuit passives into a viable counterpart to WBG [11], [13]–[19]. The solutions include the application of high-performance materials in the capacitors and inductors or using more subtle techniques, such as integrated magnetics.

In this article, the design challenges of an integrated-magnetic-based differential-mode Ĉuk rectifier (IM-DMCR) based universal battery supercharger (UBS) are addressed at a component and a system level. These challenges are manifested in power and control stages. Each design aspect is analyzed with a simplified model that captures the low- and high-frequency behaviors of the PES. The analysis is used to address the challenges of the high-power PES design leading to the best practices to minimize these challenges.

The rest of this article is organized as follows. In Section II, the UBSs IM-DMCR topology and its model are briefly introduced. In Section III, the power stage of the UBS is analyzed, and the challenges in design using an IM-DMCR are addressed. In

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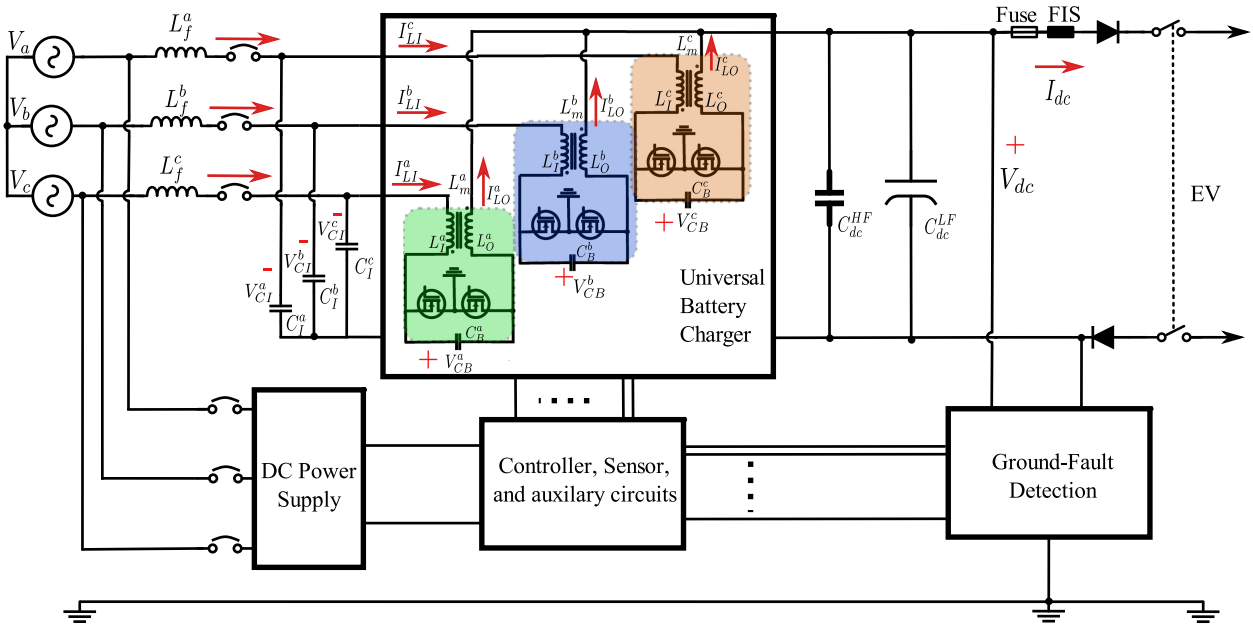


Fig. 1. Three-phase IM-DMCR topology in a UBS.

Section IV, the control architecture and challenges associated with the high-power control are discussed. In Section V, the experimental prototype of the high-power UBS is presented, along with parametric and time-domain results analysis. Finally, Section VI concludes this article.

II. Converter Topology and Model Outline

DMCR has been explored, under low-power conditions and without using IM, in previous publications in terms of the operational modes, modulation, and control architecture [25]–[28]. The high-power IM-DMCR topology is shown in Fig. 1 that forms the basis for the UBS. The IM-DMCR is a single-stage high-power converter with variable gain capable of increasing or decreasing input voltage. A reduced converter stage will potentially enable higher power density and efficiency. Input- and output-side inductors make the converter continuous input and output currents, while the proportional voltages on both inductors ease integrating both in an integrated magnetics structure [29], [30]. If further isolation is required, transformers can be integrated into the device without increasing device count [31]. Therefore, the filtering requirements for input and output sides are reduced [32]. Additionally, since the energy transfer is indirect (capacitive) in the Ĉuk converter, this will further reduce the filtering requirements. Finally, discontinuous operation of the converter can be exploited to reduce the switching losses [33].

Target specifications for the UBS are presented in Table I. In this section, a simplified high- and low-frequency model is presented that is used in the design and optimization procedure.

To improve the efficiency of the IM-DMCR, a discontinuous modulation scheme (DMS) is used [34], [35]. The voltage and current stresses and oscillations are modeled for the power-stage components for operating conditions. For the low-frequency components, it is assumed that the input is a set of balanced three-phase voltages

TABLE I
Specification of the IM-DMCR

Specification	Value
Input Voltage ($\boldsymbol{V_{ab}}, \boldsymbol{V_{bc}}, \boldsymbol{V_{ca}}$)	480 Vrms (L-L)
Output Voltage ($\boldsymbol{V_{dc}}$)	500 Vdc
Power (P)	60 kW
Ac-Link Capacitance ($\boldsymbol{C_I^a}$, $\boldsymbol{C_I^b}$, $\boldsymbol{C_I^c}$)	0.86 μF
Dc-Link Capacitance ($\boldsymbol{C_O^a} \parallel \boldsymbol{C_O^b} \parallel \boldsymbol{C_O^c}$)	4.7 mF
Blocking-Link Capacitance ($\boldsymbol{C_B^a}$, $\boldsymbol{C_B^b}$, $\boldsymbol{C_B^c}$)	0.92 μF
Switching Frequency (f)	50 kHz
Input-side Inductor ($\boldsymbol{L_I^a}$, $\boldsymbol{L_I^b}$, $\boldsymbol{L_I^c}$,)	75 μH
Output-side Inductor ($\boldsymbol{L_O^a}$, $\boldsymbol{L_O^b}$, $\boldsymbol{L_O^c}$)	75 μH
Coupling factor (Input-Output, k)	0.46
Max. Operating Temperature (T_{max})	80 °C

$$\left[V_{ab}\ \ V_{bc}\ \ V_{ca}\right] V \left[\sin(\omega t)\ \ \sin\left(\omega t - \tfrac{2\pi}{3}\right)\ \ \sin\left(\omega t + \tfrac{2\pi}{3}\right)\right] \tag{1}$$

$$V^* = \min\left\{V_{ab}, V_{bc}, V_{ca}\right\}. \tag{2}$$

The gains are generated in the model as follows:

$$\left[G^a\ G^b\ G^c\right] = \frac{1}{\sqrt{3}} \frac{V_{\rm dc}}{V} \left[|V^*|\, V_{ab} + |V^*|\, V_{bc} + |V^*|\, V_{ca}\right]. \tag{3}$$

Following that, the duty cycles are found to be

$$D^{PH} = G^{PH}/1 + G^{PH}\ \forall\ PH \in \{a, b, c\}. \tag{4}$$

The peak input current is controlled using a proportional–resonance compensator. The control architecture is outlined in [34] and [36]. Thereafter

$$\left[I^a\ I^b\ I^c\right] = I_{pk} \left[\sin\omega t\ \sin\left(\omega t - \tfrac{2\pi}{3}\right)\ \sin\left(\omega t + \tfrac{2\pi}{3}\right)\right] \tag{5}$$

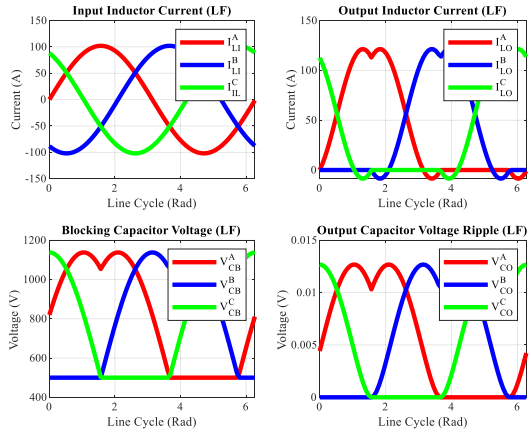


Fig. 2. Select low-frequency waveforms of the IM-DMCR.

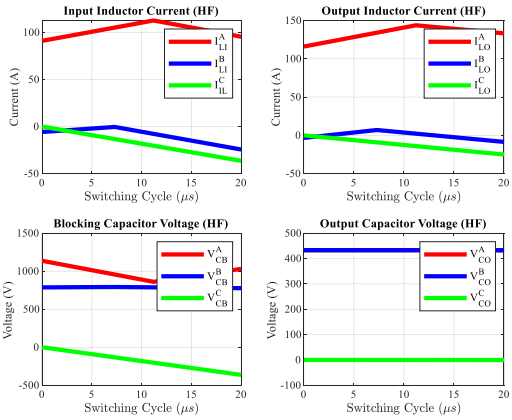


Fig. 3. Select high-frequency waveforms of the DMCR at $t = \sim 2$ rad.

and the currents through the power-stage components are

$$\left[I_{LI}^{PH} \;\; I_{LO}^{PH} \;\; I_{SI}^{PH} = I_{SO}^{PH} \;\right] = I^{PH} \;\left[1 \; G^{PH} \; 1 + G^{PH} \right] \tag{6}$$

$$I_{\text{dc}} = I_a \, G_a + I_b G_b + I_c G_c. \tag{7}$$

In (7), I_{LI}^{PH} is the ac-side inductor current of phase *PH*, I_{LO}^{PH} is the dc-side inductor current of phase *PH*, and I_{SI}^{PH} and I_{SO}^{PH} are the switch currents of the ac-side and dc-side devices, respectively. The corresponding component voltages are found to be

$$\left[V_{CO}^{PH} \;\; V_{CI}^{PH} \;\; V_{CB}^{PH} \right] = V_{\text{dc}} \;\left[1 \; G^{PH} \; 1 + G^{PH} \right]. \tag{8}$$

The resulting waveforms for some of these equations are presented in Fig. 2 at the rated power of 60 kW.

For the high-frequency modeling, the ac component is calculated using the state-space equation of each phase module with the initial condition from the previous low-frequency operation point and the average component from the low-frequency solution of the IM-DMCR. The low-frequency average component of the IM-DMCR is assigned as follows:

$$X^{PH} = \left[I_{LI}^{PH} \;\; I_{LO}^{PH} \;\; V_{Cb}^{PH} \;\; V_{CO}^{PH} \right]^T. \tag{9}$$

This value is used as the average value in (10) to predict the high-frequency behavior of the converter for two switching cycles, for rising and falling ripple

$$\frac{dX^{PH}}{dt} = \left\{ \begin{array}{l} K^{-1} \left(A_1 X^{PH} + B_1 V_{CI}^{PH} \right) \\ K^{-1} \left(A_2 X^{PH} + B_2 V_{CI}^{PH} \right) \end{array} \right\}. \tag{10}$$

The high-frequency component of the converter is shown in Fig. 3 for the state-space variables at an instance ($t = \frac{2\pi}{3}$ or ~ 2 rad) along with the low-frequency profile. As presented, following the DMS, only two high-frequency components are switching at this instance (phases *A* and *B*), while phase *C* is not switching and following the low-frequency trend.

Using the low- and high-frequency components of the state-space variables in this simplified representation, the power-stage components are designed and optimized without a complicated physical model. In this approximation, the high- and low-frequency temporal scales are assumed to be wide apart. Also, the input voltage is assumed to be constant.

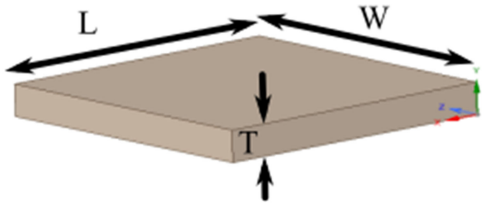


Fig. 4. Sample piece of copper for analyzing PCB performance parameters.

III. Power-Stage Challenges

In this section, power-stage challenges associated with high-power IM-DMCR are outlined.

A. High-Current PCB (HC-PCB) Design

To assemble the converter with low form factor, the components need to be connected with low inductance and resistance while maintaining reasonable temperature. HC-printed circuit board (PCB) that utilizes heavy copper is appropriate to link several components in a small package. The ability to integrate light and heavy copper simultaneously further improves the surface utilization of the HC-PCB.

The HC-PCB design optimization has the following three aspects:

power losses and associated temperature rise;

physical volume and weight of the board, affecting the power density and specific power;

inductance and capacitance causing current or voltage oscillation.

Assuming a constant length ($L = 150$ mm) of the sample copper piece, these three design aspects are explored, as shown in Fig. 4, with variation in width (*W*) and thickness (*T*). These parameters are calculated with converter specifications presented in Table I.

As evident from Fig. 5, by increasing thickness (*T*) in the sample plane, the ratio of ac to dc resistance is ($f_r = R_{\text{ac}} / R_{\text{dc}}$) and the ratio of reactance to dc resistance is ($f_x = X / R_{\text{dc}}$). This trend is aligned with increasing the volume and weight of the HC-PCB as well. On the other hand, increasing the thickness will reduce both conductive (within the copper) and convective (copper-to-ambient) thermal resistance and reduce

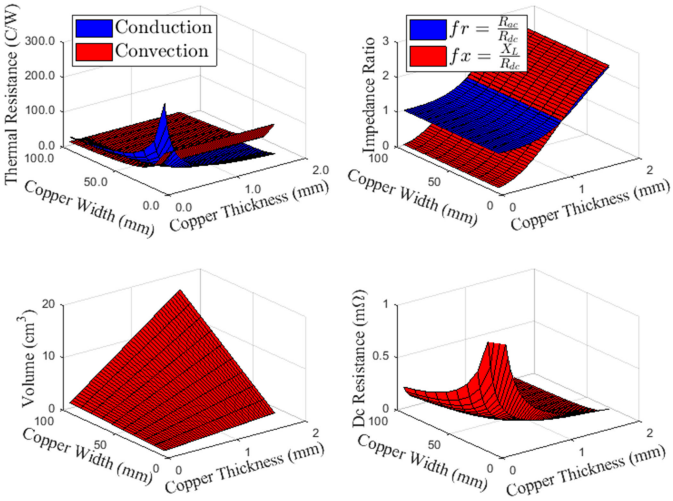


Fig. 5. Sweeping design variables with copper width and thickness.

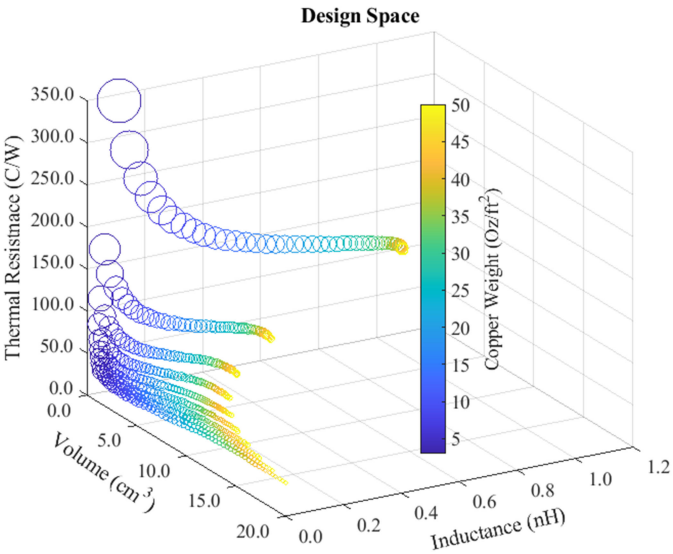


Fig. 6. Five-dimensional design space for the HC-PCB.

the dc resistance and, consequently, dc power losses. The smaller thickness (T) can be compensated by increasing the width (W), however, that yields adverse effects on the size and weight.

A five-dimensional (polygonal) design space is shown in Fig. 6, including samples thickness, width, track inductance, loss, and volume. From the trends projected in Fig. 6, the designer can limit the thickness (T) by adjusting the minimum width (W) of a certain copper. This tradeoff needs to be corrected by the tolerable temperature rise or loss as well as the inductance of the polygon (the size of the circle represents the relative loss of each design point). This is inversely related to the volume (power density) and weight (specific power). The inductance of the polygon tends to be lower at heavier copper, which enables faster switching and lower losses in the converter.

Considering the specification of this design, 16 oz/ft^2 is selected as relative optimal weight for the converter. This is augmented with an embedded 2 oz/ft^2 copper for the sensing signal routing and surface mounted device (SMD) components. With this copper design, the temperature rise profiles for input

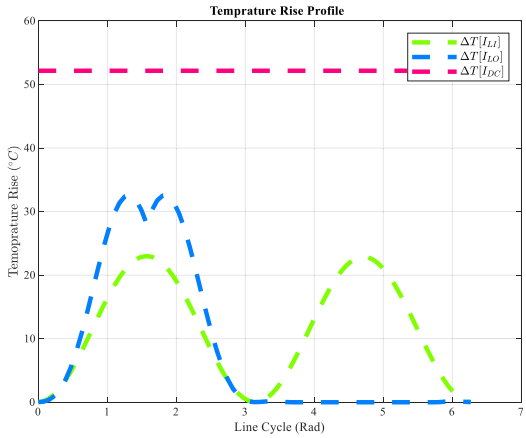


Fig. 7. Temperature rises in the ac side, dc side of the IM, and dc current in the sample copper sample.

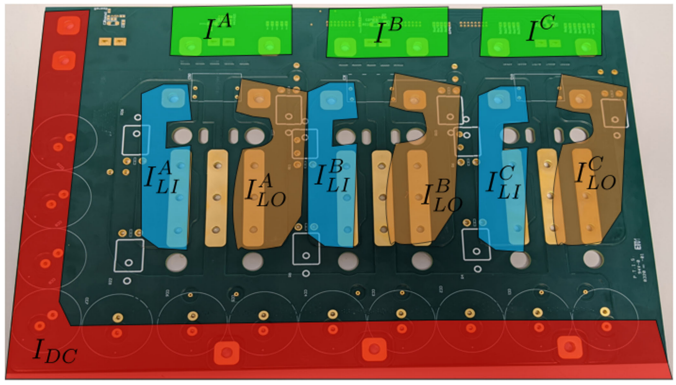


Fig. 8. Current patches in the high-power PCB for the major current carrying sections.

inductor current, output inductor current, and output dc current at the rated power are shown in Fig. 7. This representation of the temperature rise is for the sample copper polygon, as presented in Fig. 4 (no thermal capacitance). It should be noted that, in practice, the temperature rise is slower due to the thermal capacitance of the copper. This analysis informs the HC-PCB design consideration for respective loop current, as shown in Fig. 8. The return path for all currents is the ground plane laid along with the board. The minimum plane width is 50 mm. Switch current loops are distributed on several layers with smaller width to reduce inductance and ac resistive losses.

B. Integrated Magnetics

Along with the switching devices, the magnetic components affect the efficiency, volume, and weight of a PES. Soft-magnetic materials are prevalent in the inductors/transformers, which are used in the converter. Ferrite is traditionally used to yield low losses at high frequency and high permeability; however, the application of ferrite in high power is limited by either using a large core size (yielding low-power density) or inserting airgap (yielding low permeability and fringing fields). On the other hand, iron-based soft-magnetic materials, such as iron powder and electrical steel, are used in high-power application due to their high saturation tolerance at high dc bias. However, these

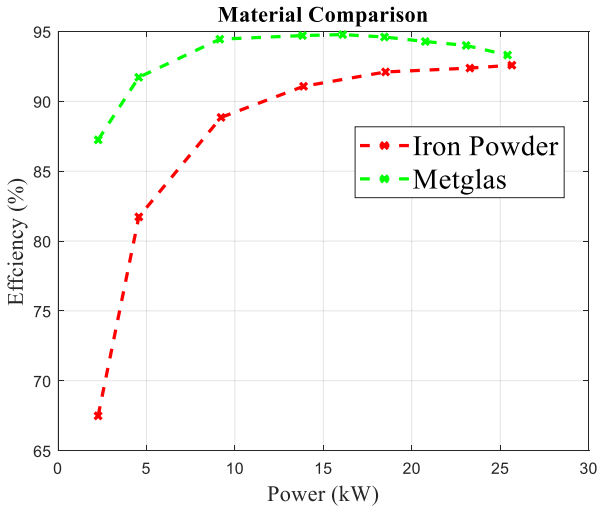


Fig. 9. Comparison of efficiencies of two IMs (for one IM-DMCR module) developed using iron-powder and Metglas materials.

TABLE II
CHARACTERISTICS OF IMS USED IN THE EFFICIENCY COMPARISON OF IRON-POWDER MATERIAL AND METGLAS IN THE IM-DMCR MODULE

Specification	Iron Powder	Metglas
Manufacturer	MicroMetal	Hitachi Metals
Part number	E315-52A	AMCC80
Stacking	Yes (Double E)	Yes (Double C)
Effective Length	193 mm	244 mm
Effective Area	490 mm^2	525 mm^2
Mass	660 g	938 g

materials are not comparable to ferrite regarding high-frequency loss and permeability.

SiC devices enable high-power switching at increased frequency; therefore, the magnetic components in the converter also need to rise to this challenge. Nanocrystalline and amorphous-metal-based materials are being increasingly used in the high-power applications [37]–[40]. Other techniques, such as flux cancellation and IM, combined with the improved performance of these materials push the power/frequency limits even further [41].

The symmetry of the DMCR topology using IM can significantly enhance the power density and efficiency of the converter [26], [27]. Based on the work done in [28] and the simplified model outlined therein, several winding configurations with different couplings have been studied with different core materials. High-power experimental comparisons are made between IM made with iron-powder core (double EE) and Metglas (double C) in a single DMCR module. In this experiment, the power loss of the soft material is evaluated for the DMCR module's IM at 450 V and 50 kHz, while the power is swept from 2.5 to 26 kW. In Fig. 9, the efficiency results are shown for both the materials with approximately the same size for the IM. The specifications of both cases are presented in Table II, while the physically fabricated device is presented in Fig. 10. The purpose of this experiment is to evaluate the relative performance of the Metglas relevant to the iron powder. The losses are improved significantly while compromising moderately on the size. To realize this IM with the Metglas material, double C geometry is

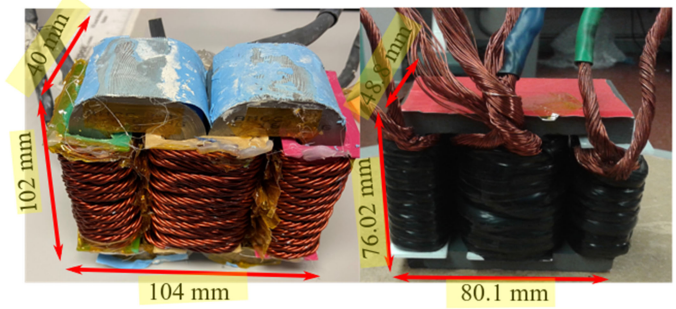


Fig. 10. Side by side comparison of iron powder and Metglas-material-based IM with relatively the same size.

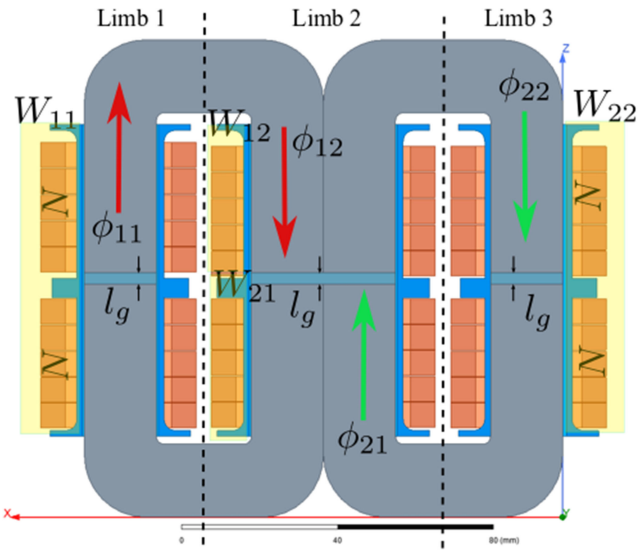


Fig. 11. IM design architecture for high-power IM-DMCR with double C cores.

selected instead of an iron-powder IM with double EE geometry. Following the magnetic device architecture, as shown in Fig. 11, the IM design is carried out.

There are certain constraints in the design of high-power IM that impose limits on design space boundaries. The thermal resistance of the core and winding, allowable temperature rise, required inductance, power density, and efficiency are among some of the more salient factors. Multiple design points are evaluated with two candidates Metglas (AMCC xx) cores [42] (AMCC200 and AMCC80). The key specifications of each design (encompassing loss, average flux density, and inductance) are shown in Fig. 12 with varying number of turns (N) and airgap length (l_g), where $N \in \{5,\ 10,\ 15,\ 20\}$ turns and $l_g \in \{0.5, 1, 23\}$ mm.

It should be noted that the inductance of the IM is limited by the stability limits of the feedback system and the ripple handling capability of the power stage. The power losses are limited by the thermal limits of the wire and the core. The average flux density is limited by the saturation flux density and B–H curve of the core material. Finally, the number of turns that can be placed on each core, as illustrated in Fig. 11, is limited by the bobbin size, bowing factor, and fill factor of the wire, as well as the available window area of the IM core.

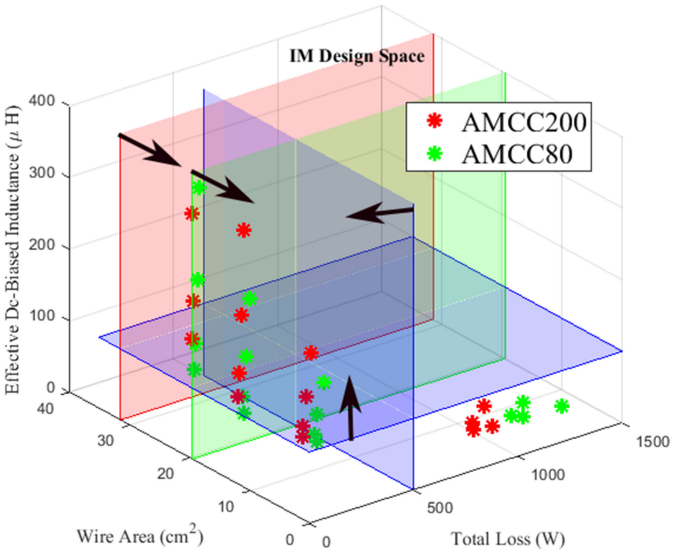


Fig. 12. Magnetics design space with imposed limits on losses, window is of the core (red plane for AMCC200 and green plane for AMCC80), and minimum inductance required.

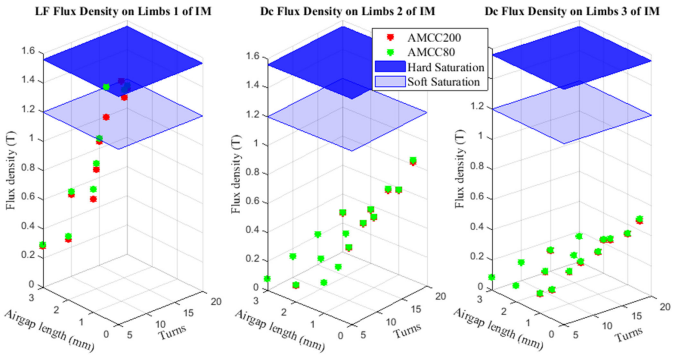


Fig. 13. Maximum flux density at peak current for both ac-side and dc-side windings in the integrated magnetics.

Considering the maximum dc current through the IM and temperature rise of the windings of the IM, Litz wire with 1350 strands AWG #38 gives the current density of 540 cm^2/A at a peak load current of 120 $\mathrm{A_{dc}}$. The wires are rated for insulation up to 1 kV. The thermal conductions of the windings are through natural convection because the windings are distributed on different limbs, and they include both ac-side and dc-side currents; the flux density is not uniform on the core. The maximum flux bias on all three limbs of the IM is shown in Fig. 13 in a line cycle. Limb 2 shows a trivial difference in the flux between the two sizes due to partial flux cancellation. Limb 3 hosts a major part of the dc-side winding resulting in much higher flux density and dictates the size of the core. The hard saturation and soft saturation limits for the core material are presented, and the designs exceeding them are avoided.

To avoid saturation at peak ac-side current as well as full load dc-side current while adhering to design limits dictated by the thermal, physical, and circuit constraints, the design point $\{N = 10 \text{ and } l_g = 2 \text{ mm}\}$ is selected from Fig. 12. This design point is selected to get low loss while compromising the size slightly. The acceptable design points are in the arrow

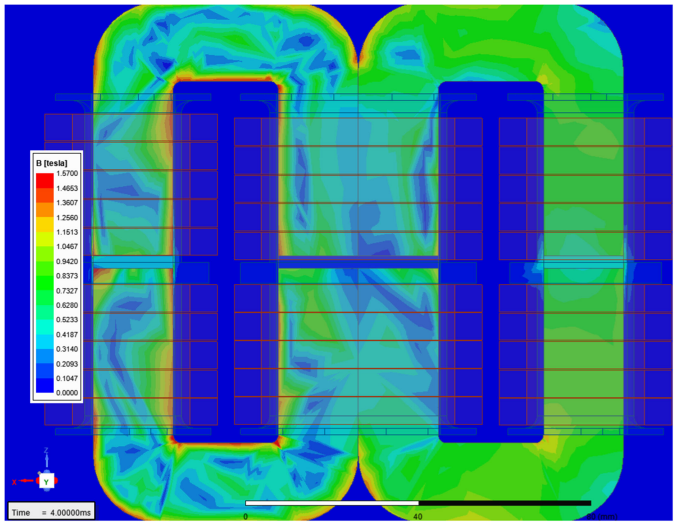


Fig. 14. Flux density field distribution on the IM-DMCR at the peak high-frequency current ripple and peak low-frequency bias for ac- and dc-side windings.

direction of the limit planes. In doing so, limits of Fig. 13 should be considered such that the cores are not saturated; this is especially important in the loosely coupled magnetics used in this design since the windings are distributed on all limbs and the dc-side windings create large high flux density (refer to Fig. 14). The total copper and core losses are 36.37 W and 275 W, respectively, while the weight and winding factor are determined to be 4195 g and 0.24, respectively. Maximum flux densities on limbs 1–3 are found to be 818 mT, 213 mT, and −133 mT, respectively, while the maximum high-frequency flux densities are determined to be 964 mT, 213 mT, and 1193 mT on limbs 1–3, respectively. The average dc-biased inductance matrix for W_{11}, W_{12}, W_{21}, and W_{22} as referred to in Fig. 11 is found to be the following:

$$L = \begin{bmatrix} W_{11} & W_{12} \\ W_{21} & W_{22} \end{bmatrix} = \begin{bmatrix} 116 & -31 \\ -31 & 103 \end{bmatrix} \mu\mathrm{H}.$$

This matrix is extracted from the finite element method (FEM) analysis of the IM carried out in ANSYS MAXWELL. The flux density distribution of this IM design is presented in Fig. 14 at the peak dc-bias excitation from the ac side (102 $\mathrm{A_{peak}}$) and dc side (120 $\mathrm{A_{dc}}$) with the maximum point (red) in the color map is saturation flux density of the Metglas material (1.56 T). The fabricated IM is shown in Fig. 15 as used in the 60 kW IM-DMCR setup.

C. Input Filter Design

To curb the electromagnetic interface (EMI) conduction noise caused by switching operation, a line filter is designed to keep the current ripple within the converter. The design methodology is adopted from the article presented in [43], augmented by the high-power consideration in the process.

The input impedance of the converter starts to resonate with the input filter at the corner frequency of the input filter. While the input filter is inevitable to prevent switching frequency and its

Fig. 15. Fabricated IM comprising Litz wire and Metglas cores.

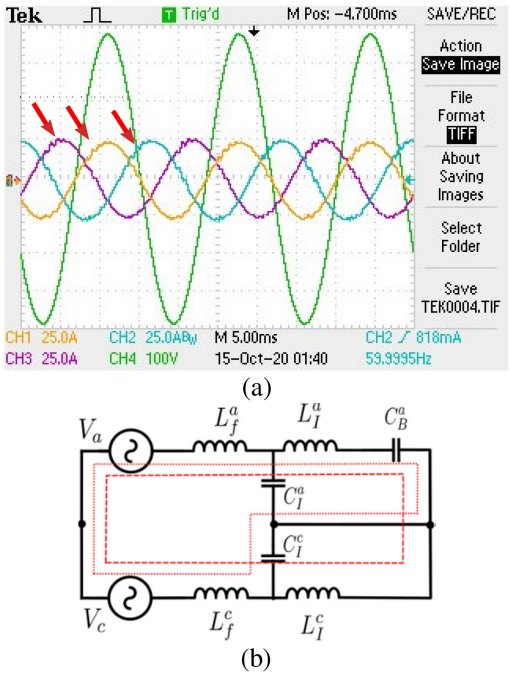


Fig. 16. (a) Input filter resonance oscillations. (b) Resonance current path in the differential module.

harmonics from entering the source, it causes these resonances that may jeopardize the performance of the converter.

An *LCL* filter topology is used at the input of the rectifier to maintain the EMI noise. Due to the topology of the IM-DMCR, only the addition of one line inductor is needed since the input side of the converter has the *CL* component to perform the filtering. This is shown in Fig. 1, where the first inductor is shown as L_f^{PH}, capacitor is shown as C_I^{PH}, and the second inductor is shown as L_I^{PH} ($\forall\ PH \in \{a, b, c\}$).

The challenges associated with the filter for this design are as follows: first, avoiding the frequency resonance with the passive components and, second, avoiding resistive elements due to the nature of the high power as it will result in extra losses.

The resonance problem is shown in the three-phase current at a line voltage of 480 V_{rms} and peak current controlled at 24 A_{peak}, as shown in Fig. 16(a). In Fig. 16(b), the resonance current path is shown in a differential module when phase *C* is carrying the return current.

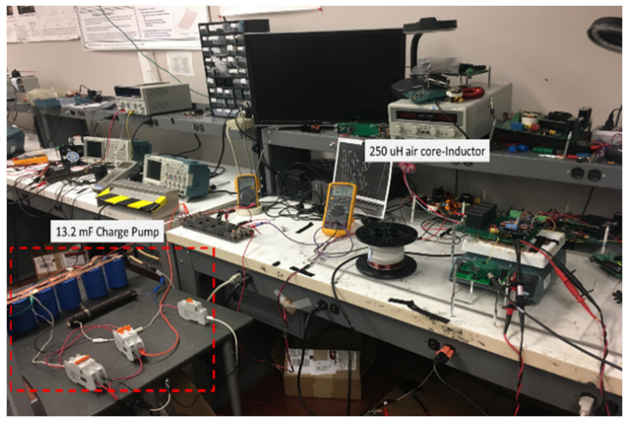


Fig. 17. DP test setup for characterization of the 1700 V SiC module.

To avoid this problem, the corner frequency of the filter and the resonance frequencies of the converter (input impedance transfer function) need to be stagnated to avoid overlap. At the input, a laminated iron inductor with 1.2 mH of inductance is selected. This inductor with the input capacitance of the converter 0.87 μF and inside inductors effective input inductance $\sim$90.87 μH ($L_{\text{eff}} = L_I^{PH}\ (1 + k^2)$ shapes the *LCL* input filter. The attenuation of the filter is on the input-side inductor current, which is ~ -117 dB at the switching frequency (50 kHz) with the resonance frequency of ($\sim$18.56 kHz).

D. SiC Power Module

Dominant Semiconductor in low voltage classes of 1200V and 1700V is SiC MOSFET, which is being used for pushing the performance limits in high-voltage, high-power applications. Based on the topology and worse operating conditions, maximum voltage and current stress across the device are 1178 V and 330 A, respectively. Multiple discrete devices can be used to support such high currents; however, this increases the stray inductance and complexity of the HC-PCB design. For the DMCR-based off-board charger, a 1700 V SiC power module is used. SiC power modules provide maximum current throughput while operating at elevated temperatures. Since the power module is not an off-the-shelve product, and with a limited amount of information, a DP test setup is prepared for its characterization, as shown in Fig. 17.

The power module was characterized for different case temperatures and gate resistances at the drain-to-source voltage and current of 800 V and 100 A, respectively. Fig. 18(a) displays the reverse recovery current profile with variation in the case of temperature and gate resistance. For a given operating temperature, the SiC module body diode generates lower reverse recovery current at gate resistance of 6.2 Ω. However, as evident from Fig. 18(b), it yields higher switching energy loss due to larger turn-ON and turn-OFF transition time. In addition to that, total switching energy loss (E_{total}) remains approximately constant with temperature rise. However, independently, turn-ON and turn-OFF losses do not follow the same trend. The turn-ON losses reduce, while the turn-OFF loss increases with temperature. This is due to the negative temperature coefficient dependence of threshold voltage. With multiple experimental observations,

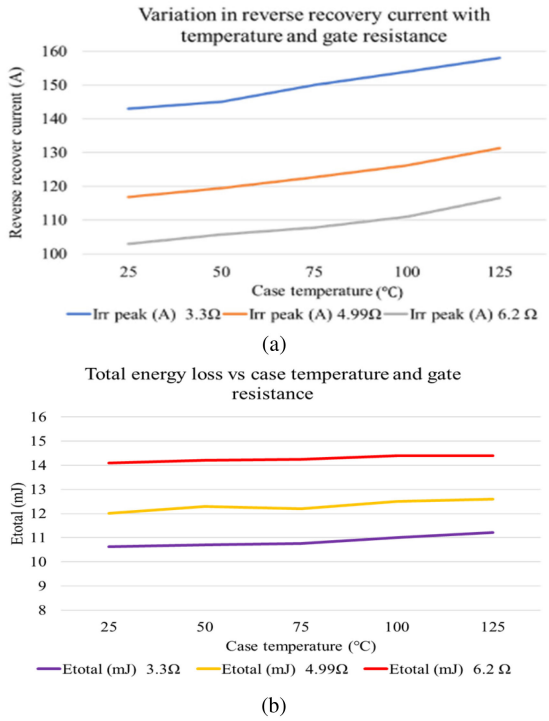


Fig. 18. (a) Reverse recovery current profile. (b) Total switching energy loss during turn-ON and turn-OFF transitions with case temperature and gate resistances.

$R_g = 5\ \Omega$ is chosen as the gate resistance. The transition time for the SiC power module at 800 V, 100 A is found to be 150 ns. This characterization aids in optimizing the electrical and thermal performance of the SiC power module. The turn-ON and turn-OFF transitions are depicted in Fig. 19 for one of the conducted experiments, as shown in Fig. 18.

E. Capacitors

The classical Ĉuk converter works based on capacitive energy transfer through the blocking capacitors. While in the IM-DMCR, there is an extra energy transfer route through the magnetic coupling, the main portion of the output energy is transferred through the capacitive link. On the other hand, the dc link traditionally takes a larger portion of the converter's size (volume and mass).

Therefore, the optimized design of capacitors is critical in the overall power density and performance. The ac-link capacitors, while insignificant (in some cases can be removed) in the traditional Ĉuk converter, are important in IM-DMCR. First, the voltage of this capacitor is unidirectional; therefore, there is a dc-bias voltage on the capacitor that needs to be considered in the DMS. Second, its ability to sink the ripple current is critically important in maintaining total harmonic distortion (THD) of the DMCR on the grid-side interface.

Using the simplified model in Section I, the voltage across the blocking capacitor and the rms current through it are evaluated. The blocking capacitor carries the ac-side inductor ripple when the dc-side device is ON and vice versa. During the switching transitions, high *di*/*dt* through this capacitor can cause oscillation

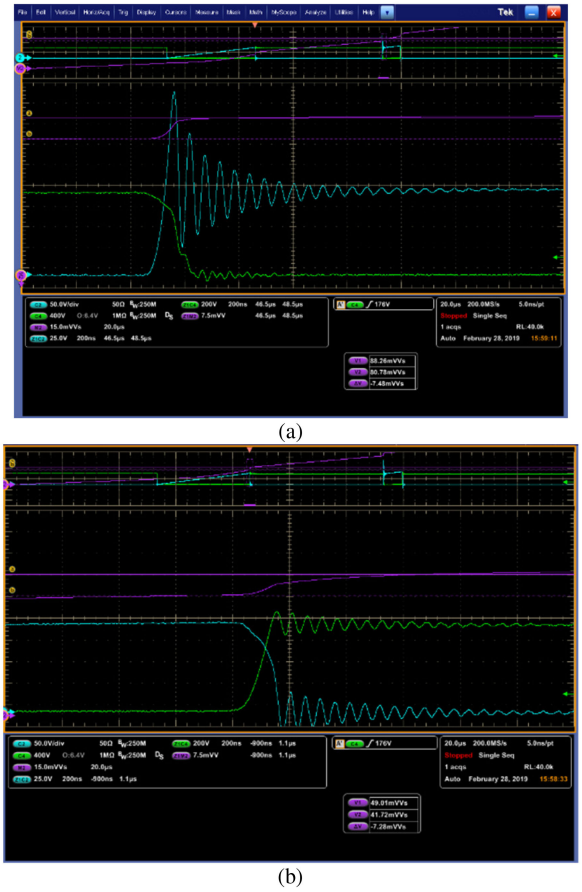


Fig. 19. (a) Turn-ON and (b) Turn-OFF transitions of SiC MOSFET module during DP test. In this figure, the blue signal is switch current (50 A/div), the green signal is switch voltage (500 V/div) that shows the switch current. This test is conducted at 800 V.

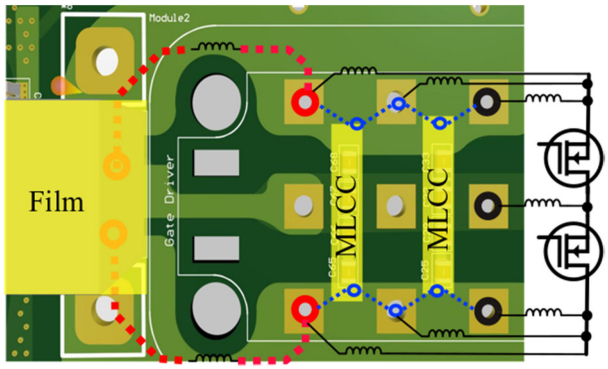


Fig. 20. High-frequency commutation loop layout of the blocking capacitors and the HB module.

in its voltage, which is across the device. Therefore, minimizing the loop inductance with the half-bridge module that makes the ac-side and dc-side devices is critical to avoid severe oscillation across the switch. Besides that, placing low equivalent series resistance (ESL) multilayer ceramic capacitor (MLCC) in parallel with a smaller loop can also redirect the current ripple away from the switch. The layout and commutation loops for this loop are shown in Fig. 20.

The second facade is the ripple current through the blocking capacitor. This ripple is at the switching frequency, and it depends on the ripple of IM. The choice of blocking capacitors is limited by the circuit parameters (C_B , $V_{CB,\max}^{LF}$, $\Delta i_{CB,\max}$), losses/temperature rise ($P_{\text{Loss}}, \Delta T_{\max}$), and the size constraints (m_{CB}, Vol_{CB}). At each operating point on the *LF* scale

$$V_{CB,\max}^{PH} = V_{\text{dc}} \left(1 + G^{PH}\right) \tag{11}$$

$$\Delta\, i_{CB,\max}^{PH} = \Delta\, i_{LI}^{PH} = \frac{D^{PH} V^{PH} \left(L_O^{PH} - L_m^{PH}\right)}{f_s \left(L_I^{PH} L_O^{PH} - L_m^{PH\,2}\right)} \tag{12}$$

$$\Delta\, V_{CB,\max}^{PH} = \frac{I_{LI}^{PH} D^{PH}}{C_B f_s}\,. \tag{13}$$

The power loss and subsequent temperature rise are given as follows [44]:

$$\Delta\, T_{\max} = T_{\text{amb}} + R_{\text{th}} P_{\text{Loss}} \tag{14}$$

$$P_{\text{Loss}} = \text{ESR}(\text{rms}\left\{\Delta i_{LI}^{PH}\right\})^2 + \frac{\left(V_{CB,\max}^{PH}\right)^2}{R_{\text{ins}}}. \tag{15}$$

In (11)–(15), T_{amb} is the ambient temperature considered to be 25 $^\circ C$, $\Delta T_{\max}$ is the maximum temperature rise in the capacitor, f_s is the switching frequency, R_{th} is thermal resistance of the capacitor, R_{ins} is the insolation resistance of the capacitor, and ESR is the equivalent series resistance of the capacitor. The capacitor related components can be found in the datasheets, and the circuit variables are derived from the simplified model, as introduced in Section I. The values used for the design are presented in Table I. According to the constraints demanded from the circuit and thermal and insolation limits of film capacitors, 2 $\times$ 0.47 μF capacitors are placed in parallel for the blocking capacitor.

The dc-link capacitor is one of the voluminous parts of the converter. Aluminum electrolytic capacitors are used for their high energy density and fixed capacitance under dc voltage bias. In the IM-DMCR with DMS, the low-frequency ripple (f_{Line}) is filtered by the dc-link capacitors, while they can filter high-frequency (f_s) ripple from the switching of the inductor current; however, to avoid high-frequency oscillation in the output voltage, a small value ceramic capacitor (C_{Dc}^{HF}) can be placed in parallel with the AL electrolytics' capacitors (C_{Dc}^{LF}), and both ripples are represented as follows:

$$\Delta\, V_{\text{Dc}}^{LF} = \sum_{PH \in a,b,c} \frac{I_{LO}^{PH}}{24 C_{\text{Dc}}^{LF} f_{\text{line}}} \tag{16}$$

$$\Delta\, V_{\text{Dc}}^{HF} = \frac{I_{LO}^{PH}}{8 C_{\text{Dc}}^{HF} f_s}. \tag{17}$$

To keep the output voltage swing within 5 V, which is recommended for the Li-ion batteries, 12 $\times$ 360 μF electrolytic capacitors are parallel. To reduce the high-frequency pollution of the output voltage, one 1 μF MLCC is placed in parallel to the dc link closer to the switching leg.

To maintain the applied ac voltage to the IM-DMCR phase module and remove the high-frequency ripple on the input modular voltage, a small high-frequency capacitor needs to be placed in the input side of the converter (as explained in Section III-C; this capacitor also serves as C link of the input *LCL* filter). This capacitor is usually considered as an extension of the EMI filter. However, since the voltage across it is used to synchronize the converter by the phase lock loop (PLL), it is discussed in this article. The voltage ripple across the ac link is

$$\Delta\, V_{CI}^{PH} = \frac{\Delta I_{LI}^{PH}}{8 C_I^{PH} f_{sw}}. \tag{18}$$

To stabilize this voltage and keep the high-frequency ripple within the converter, 0.86 μF film capacitor is placed on the ac link. Alternatively, ceramic capacitors with class 2 dielectric can be used to reduce the size significantly; however, they tend to be a lot more costly and less reliable.

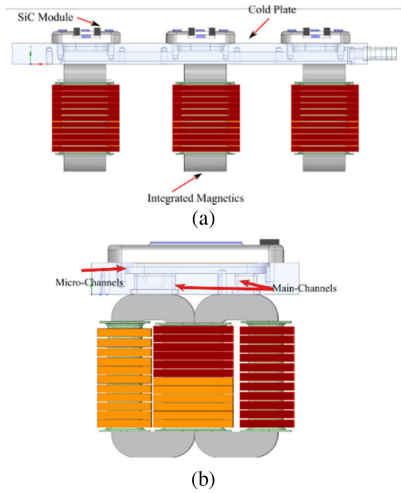


Fig. 21. Cooling solution for the high-power IM-DMCR. (a) Side view (b) front view.

F. Thermal Design

In EV applications, the available volume and weight of various components are of the essence. Efforts are made to shrink the components to make EVs more spacious and lightweight. This requires the manufacturers to move toward electronics that have the higher form factor and lower specific weight, which, in turn, creates a design challenge for finding the most efficient yet cost-effective modes of removing excess heat for keeping the critical components within optimum operating temperature ranges. Apart from conventional air-cooled heat sinks, liquid-cooled cold plates have gained widespread acceptance and have emerged as an attractive alternative for high-power and high-density PES. Liquid cooling takes advantage of the higher density, thermal conductivity, and heat capacity of the liquid in comparison to air. Furthermore, in comparison to a tubed single-side cooling, double-sided cold plates with microchannels allow the exchange of heat in much efficient way by reducing the overall thermal resistance while allowing cooling of the top- and bottom-side simultaneously.

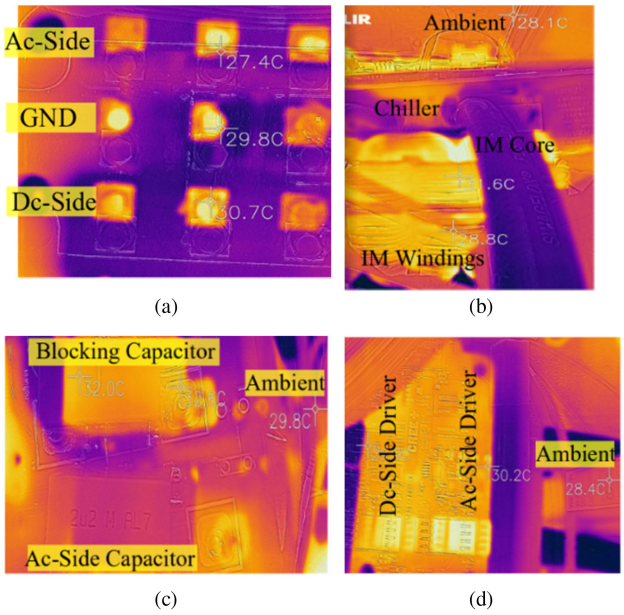


Fig. 22. Infrared image of the thermal performance of the UBS components. (a) HB SiC module. (b) Integrated magnetics core and windings. (c) Blocking capacitor as well as ac-side capacitor. (d) Cree's HB gate driver.

Fig. 21 shows the connection of IM and power module to the double-sided cold plate. The cold plate is from the Wieland-Microcolon. The power modules, due to their fast thermal transients and low thermal capacitance, are placed on top of the microchannel, and the integrated magnetics are placed on the other side on the main liquid circulation channels (double-sided cooling). Water is used as a cooling liquid and its temperature and circulation are controlled by an RC045 KODIAK circulating chiller. The chiller has a maximum heat dissipation of 5900 W. The water temperature is controlled at 19 °C.

Fig. 22(a)–(d) shows the thermal capture of the IM-DMCR power-stage components. Temperature rises of half-bridge SiC module, IM, blocking capacitor, and gate driver are shown, respectively, in Fig. 22(a)–(d).

IV. Challenges in Control Implementation and Operation

The control architecture of the IM-DMCR is presented in the previous publications [26], [27]. In this section, challenges related to scaling up the power in the IM-DMCR are outlined.

A. Total Harmonic Distortion

Increasing the voltage in the Ĉuk converter directly affects the small signal and large signal gains of the system. To maintain the same level of stability and current control tracking: 1) proportional, 2) resonance gains of the compensator are tuned, 3) higher order compensations (4th, 5th, and 7th) are added to keep the THD under 5%, 4) input capacitance from 5 μF in low-power design to 0.86 μF, the latter is a combination of two ceramic capacitors and a film capacitor.

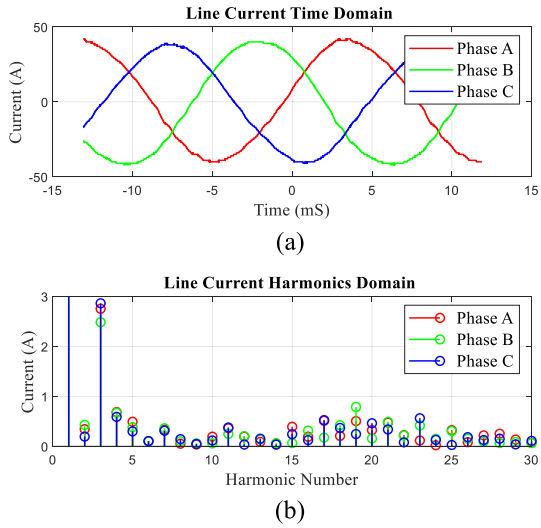


Fig. 23. (a) Three-phase line currents. (b) Spectral decomposition of the line current.

B. Third Harmonic

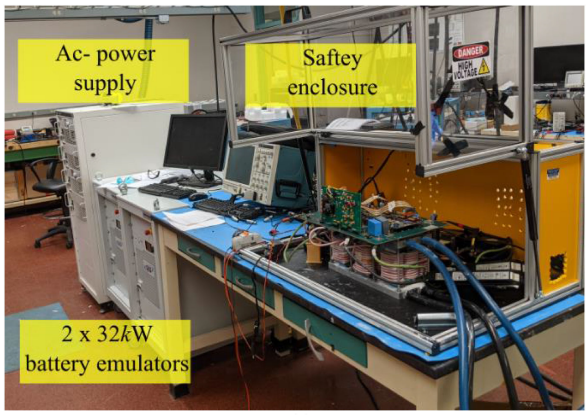
Due to nonidealities in the three-phase system and lack of neutral connection in DMCR, there exists a salient presence of the third harmonic in the line currents (see spectral decomposition in Fig. 23). To overcome this, passives need to be symmetrical in all phases as well as fine tuning the PLL controller.

C. Dead Time

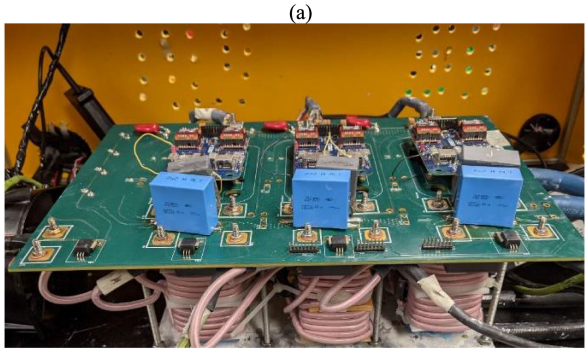
A higher dead time between the switching of the devices results in loss of duty cycle near the zero crossing. As a result, the gate-to-source voltage does not recognize small duty-cycle widths, does not switch the device, and does not affect the THD of the input current. This effect becomes more pronounced with the devices of high transition time (rise time and fall time) as to ensure no overlap of drain-to-source voltage ($V_{\rm ds}$) between high side and low side devices during transition, and a large dead time is required. A lower dead time can improve the THD; however, it results in shorting of the ac-link capacitor, which, in turn, dips the output voltage and results in loss of efficiency. In lieu of this, the dead time is optimized on the current setup and is kept at 800 ns.

D. Power Factor Correction

Near unity power factor is achieved by sensing the input modular voltages. The voltage sensors must cover the entire range from 0 to 678 V and are typically designed for the highest sensing voltage. This results in a loss of accuracy at lower operating voltages and affects the power factor correction. Furthermore, in a three-phase system, since the three input voltage vectors are 120° apart (ideally 0°, 120°, and 240°), the loss of power factor correction (PFC) becomes more pronounced and reduces the total active power component. To mitigate this, a phase compensation of 20° is given in the code such that the three reference vectors that are generated by sensing the input voltages are aligned at 20°, 140°, and 260° but still apart by 120°.



(a)



(b)

Fig. 24. (a) IM-DMCR experimental setup. (b) Power-stage components and board of the IM-DMCR.

V. Experimental Results

Based on the design criteria in Sections III and IV, a 60 kW experimental IM-DMCR is designed and tested. Experimental setup and the IM-DMCR board configurations are shown in Fig. 24(a) and (b), respectively. Two 32 kW, TC32.500.80-Q14-GSS-20064 battery emulators from Regatron are placed in parallel and controlled through serial communication to act as the load for the battery charger. The power supply is a 60 kW ac source made by combining four 3150AFX supplies from Pacific Power. All the time-domain voltage measurements are made by THDP0200 probes, and the current measurements are done by TCP303 current probes with TCPA300 amplifiers. Component values for rated power experimental results are presented in Table I.

The semiconductor device is a half-bridge 1.7 kV, 600 A SiC device from Cree accompanied by off-the-shelf gate drivers. Integrated magnetics is made by Metglas core supplied by Hitachi Metals America and Litz wire from New England Wire Technologies. The HC-PCB is manufactured by EPEC technologies.

To demonstrate the operational functionality of the experimental setup at 60 kW, the power level of the UBS is increased gradually by increasing the input current reference. Fig. 25 displays a comparison of the tracking reference and feedback current.

The mismatch in the phase current is owing to the dissimilarity in the passives between the IM-DMCR modules and propagation delays mismatch on each driver.

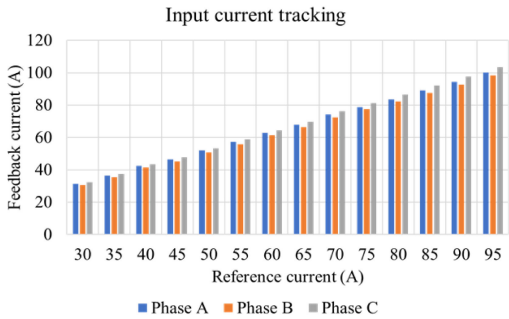


Fig. 25. Input current feedback and reference for phases *A*, *B*, and *C*.

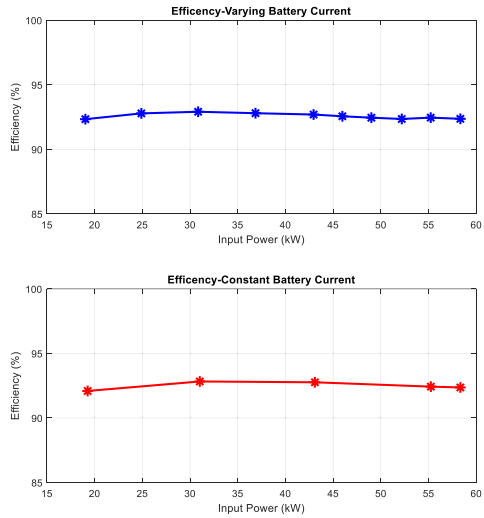


Fig. 26. Efficiency of the experimental DMCR for two different battery modes with varying power.

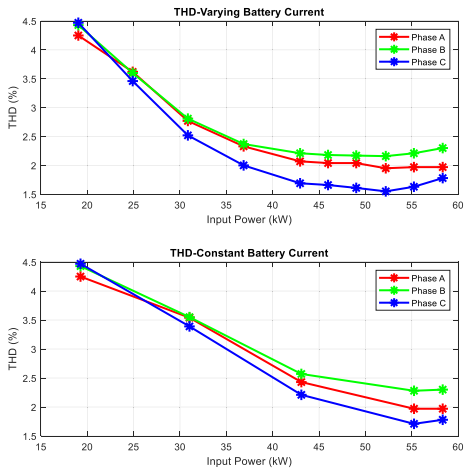


Fig. 27. THD in the experimental setup at two different battery modes with varying power.

Fig. 26 shows the parametric plots of the efficiency of phases *A*, *B*, and *C* with input power variation for two modes of battery charging. The IM-DMCR with hard switching reaches a peak of 93% efficiency at 30 kW and is plateaued at 92.5% from 20% to 100% of the rated power.

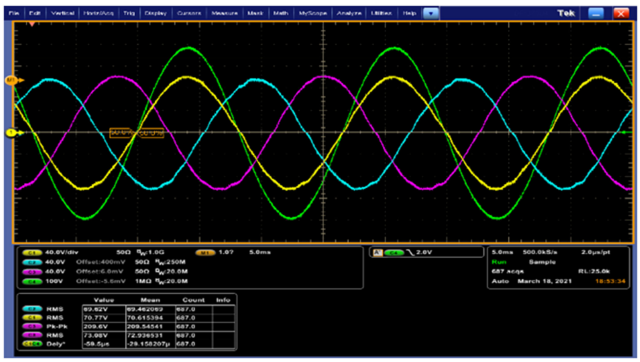


Fig. 28. Steady-state time-domain results of the three-phase input current and phase A input voltage. The yellow curve is phase A current (40 A/div), the blue curve is phase B current (40 A/div), the purple curve is phase C current (40 A/div), and the green curve is phase A voltage (100 V/div).

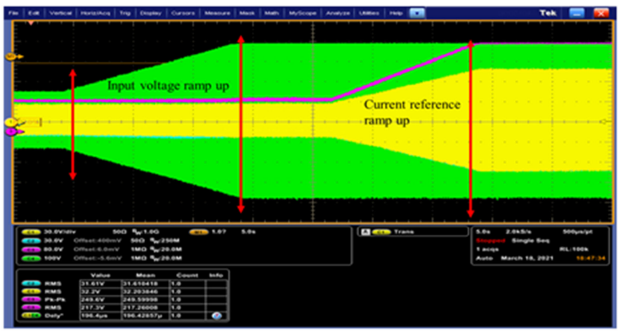


Fig. 29. Sequence of increasing the power on the UBS setup from 20% of the rated power to the rated power.

Fig. 27 plots the THD of phases *A* (red), *B* (green), and *C* (blue) and the THD reduces from 7% to 2% on average as the power is increased to the rated power. The reduction in THD is the result of an increment in the fundamental current component, while the fundamental voltage component is the same.

Fig. 28 displays the steady-state time-domain waveform for input currents phase *A* (yellow), phase *B* (blue), phase *C* (purple), and L-N voltage of phase *A* (green) at the rated power of 60 kW.

Fig. 29 displays the sequence of increasing the power on the IM-DMCR setup during the initial testing phase. The signals in yellow, green, and purple represent phase *A* current, phase *A* voltage, and output voltage, respectively. As evident from Fig. 29, the prototype is turned ON at a lower input voltage of 40 V_{rms} (L-L) and is ramped up to 480 V_{rms} (L-L) in 15 s. In this duration, the input current can maintain its tracking reference of 20 A due to the current control mode of operation. When the input voltage reaches 480 V_{rms} (L-L), the input power is increased from 13.5 to 60 kW by increasing the current reference from 20 A_{peak} to 100 A_{peak}.

VI. Conclusion

In this work, the design challenges associated with IM-DMCR-based SiC UBS are presented. Furthermore, appropriate methodologies to address technical challenges in high-power design are discussed. The design challenges encompass power and control stages. Regarding the former, the focus of this manuscript has been on IM, HC-PCB, SiC power module, thermal design, and capacitors considering on efficiency and power density. The control challenges focus on the implementation and operation with performance metrics focusing on power quality, dead time, and power factor correction considering dynamic performance. Finally, a 60 kW IM-DMCR for a UBS is experimentally fabricated and tested, yielding satisfactory performance.

Acknowledgment

The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

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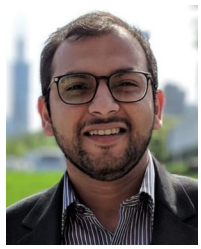

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