Confluence of Integrated Magnetics and TCM for a ZVS Based Higher Order Differential-Mode Rectifier

Moien Mohamadi, *Student Member, IEEE*, and Sudip K. Mazumder, *Fellow, IEEE*

***Abstract*—Two driving performance metrics in modern power-electronic systems are power density and efficiency: usually, improvement in one result in sacrificing the other. In this article, triangular conduction mode (TCM) is used alongside integrated magnetics to achieve both performance metrics simultaneously. TCM is implemented by extending the switch current high enough to reverse direction and provide enough energy at the onset of the deadtime to discharge the parasitic capacitance of the SiC MOSFET. The elevated current ripple is alleviated by distributing the rectifier low-frequency current among parallel interleaved sub-modules. Taking advantage of the symmetrical topology of the differential mode Ćuk rectifier, an integrated interleaved magnetic (IIM) structure is proposed to house all the inductors in a module. In doing so, flux cancellation technique is used between the ac-and dc-side inductors to reduce the losses and size while using a custom core structure to control the flux coupling between the interleaved windings. A step by step design algorithm is presented to manage the different types of coupling within IIM. Challenges in design, fabrication, and testing of the system are analyzed and appropriate solutions are presented in each section. The solutions are supported by mathematical analysis to optimize the power stage design and validated by circuit as well as finite element simulations. An experimental setup is assembled to test this concept and multiple time-domain and parametric results are presented for proof of the concept in rectifier mode and single module mode.**

***Index Terms*—Differential mode, integrated magnetics, interleaved converter, rectifier, soft switching, triangular conduction mode (TCM).**

I. Introduction

APPLICATION of ac to dc converters are prevalent across multiple industries [1], [2]. The defined specification for a converter depends on its performance requirements set by government and industry standards. High efficiency and power density are two opposing requirements imposed on modern power electronic systems. While both performance metrics are desired, for any specific application only one could be prioritized as common design practice. Namely, the EV chargers are in high demand to convert the ac grid power into dc that is suitable for Li-Ion batteries. Small size and low loss are two of the pillars of research in this field, where use of high efficiency is more desirable in off-board versions and high power density is more desired in on-board version [3], [4], [5], [6].

Using superior properties of wide band gap devices, e.g., high dielectric field breakdown (higher blocking voltage), high bandgap (smaller size), enhanced thermal conductivity (smaller thermal mitigation system and higher frequency) [7] combined with advanced power electronic system design methods, e.g., soft-switching (reduce switching loss), integrated magnetics (reduce core loss and size), and interleaving (reduce filter size), achieving both requirements simultaneously is feasible in a variety of topologies and applications [8], [9], [10], [11].

In a typical hard switched converter, more than half of the total losses are in the device [12], [13]. There are many mechanisms causing losses in an SiC device, e.g., voltage–current overlap, parasitic capacitors, reverse recovery of the parasitic diode, conduction loss, and ON state drop in the diode. Therefore, to achieve high efficiency (in high 90%) some sort of soft switching is inevitable [14], [15].

Multiple soft-switching mitigations exist in the literature, resonance/quasi resonance/multi resonance converter families [14], [15], [16] and active bridge families [17], [18] offer soft-switching as an inherent part of the converter topology. Active resonance/clamp circuits are added to existing circuits to initiate soft-switching during the switching transition [19], [20]. Alternatively, a solution frequently visited in the literature to enable soft-switching in an existing topology without additional circuit is extending the switching current to zero and reverse its direction. In the literature, this method is referred by using several different nomenclatures. Discontinuous conduction mode (DCM) is used in rectifier application because input current naturally follows the voltage without forced control and the power factor is high [21], [22], [23], [24], [25]. To avoid extended duty loss, boundary conduction mode or critical conduction mode (CCM) is used to fine tune the current ripple by either close loop (detecting zero crossing of the inductor's switching current) or adjusting the inductance for worst-case scenario on the line cycle current [26], [27]. Furthermore, in synchronous converters triangular conduction mode (TCM) is coined to emphasize the reversal of current direction [28], [29], [30]. In this article, all these conduction modes that extend the current to enable ZVS are collectively referred to as TCM.

Differential mode Ćuk rectifier (DMCR) is proven to be effective interfacing the grid and convert ac voltage to dc with

Manuscript received 16 November 2022; revised 6 February 2023; accepted 13 March 2023. Date of publication 6 April 2023; date of current version 19 May 2023. This work was supported by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award DE-AR0000903 in the CIRCUITS program monitored by Dr. Isik Kizilyalli. Recommended for publication by Associate Editor L. Peng. *(Corresponding author: Sudip K. Mazumder.)*

The authors are with the Department of Electrical and Computer Engineering, University of Illinois, Chicago, IL 60607-7101 USA (e-mail: mmoham65@uic.edu; mazumder@uic.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3265350.

Digital Object Identifier 10.1109/TPEL.2023.3265350

variable gain and smooth input/output currents [31]. Applying TCM switching operation to DMCR eliminated the turn-ON losses of the ac-side switch, however, by forcing the current to zero (or a predetermined negative current), its ripple (half of peak to peak) needs to be at least equal to the grid frequency average current. This is a significant increasement (100% of average) compared to CCM current ripple which is usually less than 10% of the average grid current. On top of that the ac-and dc-side decoupling capacitors need to handle elevated currents through them, which means the size and losses in the filter components will increase correspondingly. Unlike other conventional topologies, Ćuk converter's operation in TCM [21], [22] depends on combination of two inductor currents ripples, leading to increased turn-OFF loss and ON-state conduction loss. Therefore, DMCR is relatively more vulnerable to current ripple amplitude.

Interleaving each module into multiple (n) parallel and synchronously phase-shifted submodules can address these challenges on several fronts [32], [33], [34], [35]. The average inductor current is divided by number of interleaved modules, in doing so, extending the switch current to zero can be achieved by a lower ripple current (100/n %). The electromagnetic interference (EMI), sensor pollution, capacitor size, inductor loss, and excess conduction loss is also addressed to various degrees by this method. This solution adds certain complications that need to be handled. The increased number of sub-modules need to be implemented with appropriate hardware technology to maintain the power density. Integrated magnetics is often used in interleaved converters [32], [33], [34], [35], [36], [37], [38]. The effect of interleaving angle with duty variation (sub-module overlap) is studied in [39] for a 10 kW dc–dc converter. In [35] an integrated magnetic structure is proposed to contain all inductors of a three phase, 4x interleaved submodules in a single magnetic structure, reducing volume by 15%. The design and geometrical analysis of magnetic devices for integrated interleaved converters are explored in [33], [36], [37], and [38], attempting to optimize the design for maximum symmetry in the magnetic core as well as minimizing the ripple at the input/output ports of the magnetic device

The use of IM in conjunction to TCM is particularly appealing. The integrated magnetics can contain the size of the magnetic components in interleaved connection of TCM submodules. The increased size as explained earlier is direct effect of enlarged current ripple as well as indirectly through the interleaved mitigation. Aiming at improving efficiency/power density [30] proposes interleaved TCM rectifier where efficiency of 99% at 200 W and power density is 1100 $\mathrm{kW/m^3}$. Integrated magnetics with TCM is used in inductive power transfer chargers in a two stage converter in [40]. While the IM is used in the dc–dc stage of the rectifier it achieves 98.6% efficiency in the dc–dc module at 20 kW with power density of 9500 $\mathrm{kW/m^3}$. Use of IM in some TCM converter is delegated to the filter inductors, an example is presented in [41]. In [42], IM is used in an interleaved TCM SEPIC converter to manage the current ripple and maintain high efficiency acquired by the DCM. In this work, the rectifier archives efficiency of 96% at 500 W sourced from a 110 $\mathrm{V_{rms}}$ grid. The design example presented in the article would be to achieve power density $\rho_p \geq 6720\ \mathrm{kW/m^3}$ while maintaining efficiency of $\eta \geq 95\%$. Other specifications would be presented in Table I for a single submodule.

TABLE I
SPECIFICATIONS OF A SINGLE SUBMODULE IN A THREE PHASE ZVS-DMCR THAT CONTAINS 3 x SUBMODULES

Specification	Value
Power	6.67 kW
Voltage (Ac-side, Line- Line, RMS)	480 V
Current (Ac-side, RMS)	25 A
Voltage (Dc-side)	200–500 V
Current (Dc-side)	15–35 A
Switching frequency (Load-dependent)	50–100 kHz
Grid frequency	60 Hz

The contribution of this article is using a custom integrated interleaved magnetic in DMCR with TCM to maintain the power density while improving the efficiency. Unique challenges of TCM in DMCR is analyzed in conjunction with discontinuous modulation scheme (DMS) in three time scopes (grid frequency, switching frequency, and switching transitions). Informed by this analysis, the mechanisms in which the IIM and TCM affect one-another are identified and a design procedure for scalable integrated magnetics is proposed to house all inductors of a module in a single magnetic structure. This design is iterated by ensuring the ZVS at turn ON, minimizing the inductor losses caused by elevated current ripple with TCM, managing different types of couplings between indicators of a module to ensure symmetrical operation of interleaved submodules, and finally utilizing the flux cancellation to reduce the magnetic losses. In this article, the challenge of increased number of components in an interleaved topology, is further addressed by appropriate power module [43], custom gate-driver motherboard, integrated magnetics [31], [44], and open-loop ZVS control [45].

The rest of this article is organized as follows, In Section II, the TCM is introduced in DMCR topology with IIM. The operational modes are analyzed in low, high, and transition temporal scales. In Section III, a novel IIM is proposed to complement the ZVS based DMCR, which from now will be referred to as ZVS-DMCR. In Section IV, experimental design, and results for ZVS-DMCR is presented. Finally, Section IV concludes the work.

II. THREE-PHASE IIM BASED ZVS-DMCR USING TCM

The hard-switched DMCR is presented in [31] as a high power battery charger, where estimated loss break down of a DMCR module, based on experimental data, for the hard-switched converter shows that the ac-side device dominates the total loss of the ZVS-DMCR module. To overcome this problem, the ZVS-DMCR architecture is extended to n interleaved submodules per module where the carrier of each submodule is phase shifted by $360/n$. The circuit is shown in Fig. 1.

A. Low-Frequency Operation \Reviewed\Reviewed

The input current (ac-side) of the ZVS-DMCR is controlled by stands for proportional resonance (PR) compensators [46]

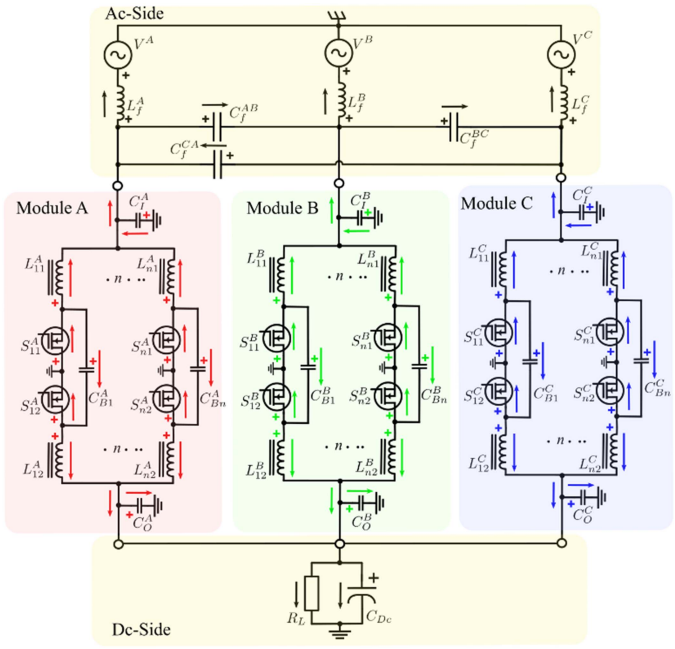

Fig. 1. ZVS-DMCR with integrated magnetics and n-interleaved submodules.

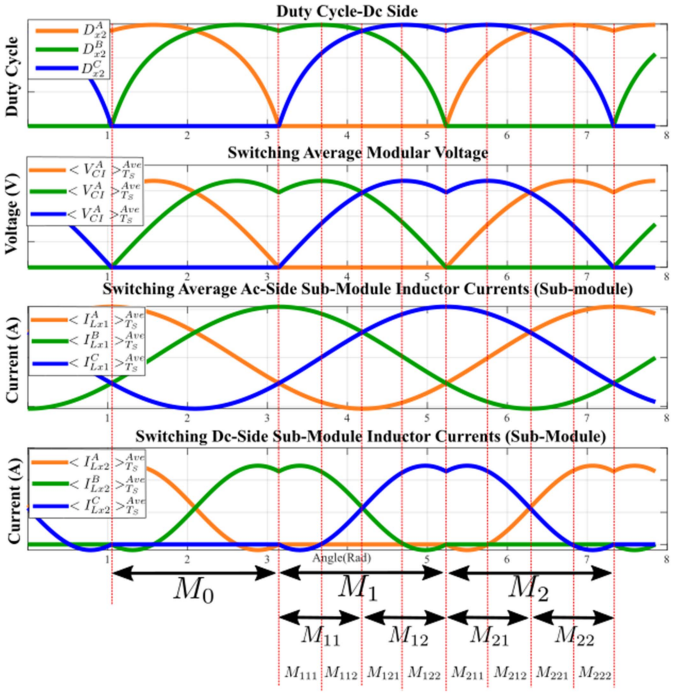

Fig. 2. LF (switching averaged) operation modes of the ZVS-DMCR (analytical model). These modules are presented for module C as reference.

and the switches are modulated using DMS [47]. These control and modulation are selected to improve efficiency and controllability of the ZVS-DMCR. In doing so, for the purposes of soft switching, the low-frequency (LF) modes, displayed in Fig. 2, are recognized. These modes are distinguished by the direction of the ac-side inductor current and the relative magnitude of the duty cycle of the module of interest. If the switching frequency

TABLE II
SWITCHING TRANSITIONS TYPE FOR AC-AND DC-SIDE SWITCHES DURING EACH LOW-FREQUENCY MODE FOR HARD (CCM) AND SOFT (TCM) SWITCHING

LF Mode	Angle	Cond. Type	$S^{ph}_{x1}[on]$	$S^{ph}_{x2}[on]$	$S^{ph}_{x1}[off]$	$S^{ph}_{x2}[off]$
M^{ph}_{111}	60°	CCM	Soft	Hard	Hard	Hard
		TCM	Soft	Soft	Hard	Hard
M^{ph}_{112}	60°	CCM	Hard	Soft	Hard	Hard
		TCM	Soft	Soft	Hard	Hard
M^{ph}_{121}	60°	CCM	Hard	Soft	Hard	Hard
		TCM	Soft	Soft	Hard	Hard
M^{ph}_{122}	60°	CCM	Hard	Soft	Hard	Hard
		TCM	Soft	Soft	Hard	Hard
M^{ph}_{211}	60°	CCM	Hard	Soft	Hard	Hard
		TCM	Soft	Soft	Hard	Hard
M^{ph}_{212}	60°	CCM	Hard	Soft	Hard	Hard
		TCM	Soft	Soft	Hard	Hard
M^{ph}_{221}	60°	CCM	Hard	Soft	Hard	Hard
		TCM	Soft	Soft	Hard	Hard
M^{ph}_{222}	60°	CCM	Soft	Hard	Hard	Hard
		TCM	Soft	Soft	Hard	Hard

is sufficiently higher than the grid frequency ($f_s \gg f_g$), then the number of the interleaved sub-modules are irrelevant in the LF scope. These modes occur because of the DMS-based switching and the three-phase DMCR topology regardless of HF modes of current conduction, e.g., interleaving, DCM, etc.

In Fig. 2, the LF modes are outlined for module-C waveforms, and they are as follows:

1) M_0 : Module C returns the LF current, S^C_{x1}(ON), S^C_{x2}(OFF) where, $x \in \{1, .., n\}$, $I^C < 0$, and $D^C_2 = 0$.
2) M_1 : Module C and A are switching differentially, S^B_{x1}(ON), S^B_{x2}(OFF), where $x \in \{1, .., n\}$, $I^B < 0$, and $D^C_2 \neq 0$.
   a) $M_{11} : D^A_2 > D^C_2$
      i) $M_{111} : I^C < 0$
      ii) $M_{112} : I^C > 0$.
   b) $M_{12} : D^A_2 < D^C_2$
      i) $M_{121} : I^A > 0$
      ii) $M_{122} : I^A < 0$.
3) M_2 : Module C and B are switching differentially, S^A_{x1}(ON), S^A_{x2}(OFF), where $x \in \{1, .., n\}$, $I^A < 0$, and $D^C_2 \neq 0$.
   a) $M_{21} : D^C_2 > D^B_2$
      i) $M_{211} : I^B < 0$
      ii) $ii) M_{212} : I^B > 0$.
   b) $M_{22} : D^C_2 < D^B_2$
      i) $M_{221} : I^C > 0$
      ii) $ii) M_{222} : I^C < 0$.

During M_0, the module of interest (i.e., module C), is not switching and it is being used to return differential current of the other two modules. During M_1 the leading modules is being used to return and during M_2 the lagging module takes that role. The significance of these modes is the direction of the current and polarity of the voltage changes that affect the natural ZVS of the synchronous switches in the Ćuk half bridge. The duration of each mode and the transition type is shown in Table II along with the ON/OFF transition type of high and low side switches in a submodule. The transition type is shown for hard (CCM) and

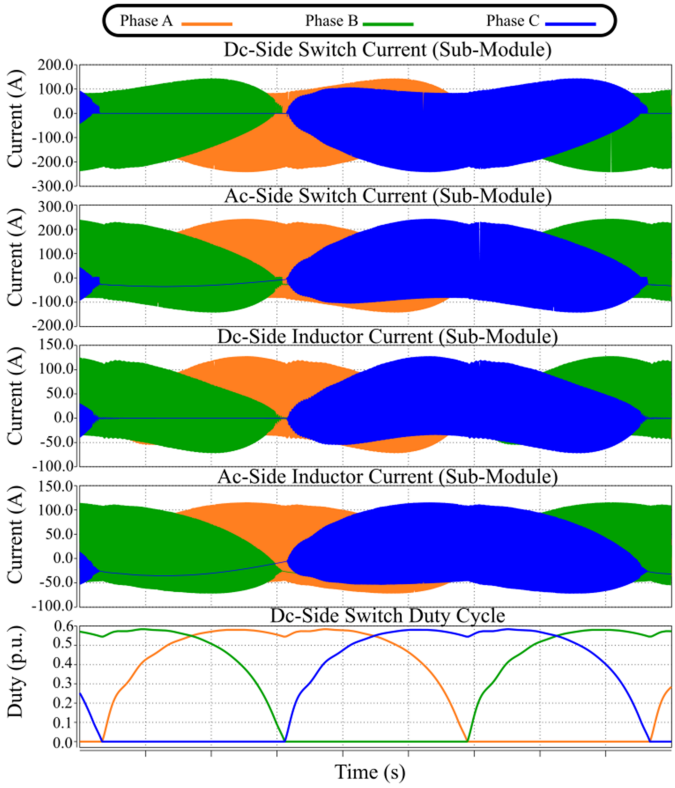

Fig. 3. SABER circuit simulation of the ZVS-DMCR with 3x interleaved submodules at $OP_1 : \{T_s = 20\,\mu\text{s},\ G^{\max} = 0.68,\ V^{ph} = 480\,\text{Vrms}, R_L = 4.167\,\Omega\}$.

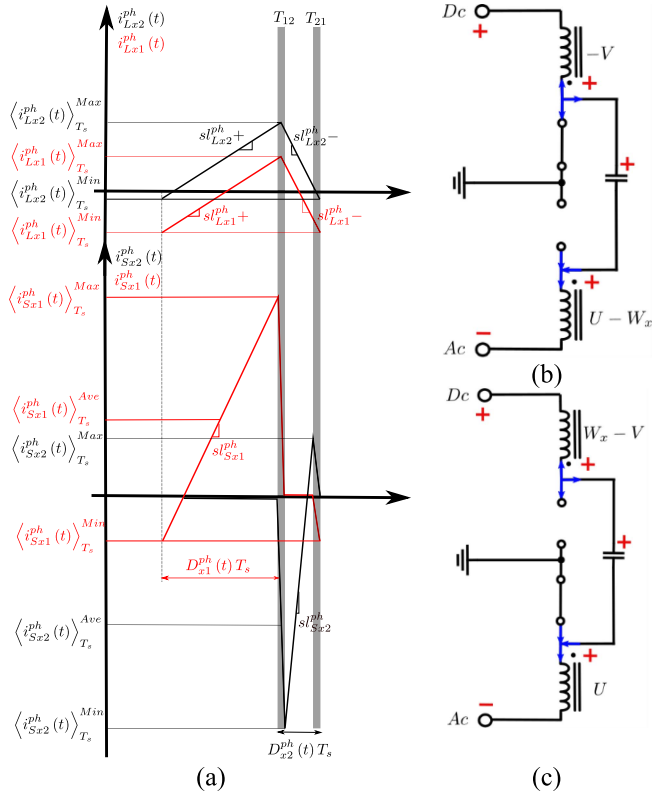

Fig. 4. High-frequency operation of a single submodule in the ZVS-DMCR. (a) AC- and DC-side inductor and switch currents. (b) High-frequency switching circuit HF_1. (c) High-frequency switching circuit HF_2.

soft (TCM) switching types. The shaded red are hard transitions, the shaded blue are soft transitions before applying TCM, and the green shaded are flipped transitions due to TCM. The input modular voltage is negative and output dc voltage is positive under all modes. It can be proven mathematically that the average current (LF) and current slope (high frequency) are in ac- and dc-side inductors are always in the same direction/polarity, i.e., $\langle i^{ph}_{Lx1}(t)\rangle^{\text{Ave}}_{T_s}\langle i^{ph}_{Lx1}(t)\rangle^{\text{Ave}}_{T_s} \geq 0$ and $\left(\frac{di^{ph}_{Lx1}(t)}{dt}\right)\left(\frac{di^{ph}_{Lx2}(t)}{dt}\right) \geq 0\,(ph \in \{A,B,C\}$ and $x \in \{1,\ldots,n\})$, where $\langle\blacksquare\rangle^{\text{Ave}}_{Ts}$ indicates switching average of the inductor currents. Therefore, by operating in TCM mode the switch current will follow the ac-plus dc-side currents. The SABER simulation for ac-and dc-side inductor and switches in TCM mode at LF scope is shown in Fig. 3.

B. High-Frequency Operation

The high-frequency (switching frequency) operation of the ZVS-DMCR in TCM follows the work that is done in papers [21] and [22]. The TCM operation in ZVS-DCMR is unique compared to other basic topologies, in the sense that switch current is the combination of two inductor currents ($i_{Sx}\,(t) = i_{Lx1}\,(t) + i_{Lx2}(t)$). Therefore, the TCM transition depends on the relative inductance of the ac- and dc-side inductors. Transition instance of the switch current from forward (drain to source) to reverse (source to drain) depends on the LF operating point.

The LF operating points (for both dc–dc (D_{2x}) and rectifier ($G^{\max}$)) is uniquely identified by $OP : \{T_s, D_{2x}\ or\ G, V^{ph}_m, \text{Load}\}$ (It should be noted since interleaving and magnetic integration change the current ripple as well and it is addressed Section III-A). Different operation points are defined to test the converter in both dc–dc module operation as well as rectifier operation. In doing so, the effect of TCM and IIM can be studied throughout multiple duty cycles, voltages, loads, switching periods, and gains. The conceptual waveforms of inductor and switch currents in TCM for a single submodule is shown in Fig. 4(a), where the circuit changes between Fig. 4(b) and (c) with duty cycles $D^{ph}_{x1}(t)$ and $D^{ph}_{x2}(t)$, respectively, $(ph \in \{A,B,C\}$ and $x \in \{1,\ldots,n\})$.

$\text{Sl}^{ph}_{Lx1+}(t)$, $\text{Sl}^{ph}_{Lx1-}(t)$, $\text{Sl}^{ph}_{Lx2+}(t)$, and $\text{Sl}^{ph}_{Lx2-}(t)$ refers rising and falling current slopes of the ac- and dc-side inductor, respectively. $\text{Sl}^{ph}_{Sx1}(t)$ and $\text{Sl}^{ph}_{Sx2}(t)$ refers to the current slopes of the ac- and dc-side switches, respectively, where

$$\text{Sl}^{ph}_{Sx1}\,(t) = \text{Sl}^{ph}_{Lx1+}\,(t) + \text{Sl}^{ph}_{Lx2+}\,(t) \tag{1}$$

$$\text{Sl}^{ph}_{Sx2}\,(t) = \text{Sl}^{ph}_{Lx1-}\,(t) + \text{Sl}^{ph}_{Lx2-}\,(t)\,. \tag{2}$$

Assuming resistive load (R_L), the slope of each inductor at any instance of line cycle depends on input voltage (V^{ph}_m), switching period (T_s), duty cycle ($D^{ph}_{x2}\,(t) = 1\text{-}D^{ph}_{x1}(t)$), and inductance matrix ($\bar{L}$). The state-space differential equations for

one module of ZVS-DMCR can be written as follows:

$$\overline{M_x} = \bar{K}\ .\overline{M_{dx}}. \tag{3}$$

In (3), the state-space equation of a single module (containing n sub-modules) is presented, where $\overline{M_x}$ is the voltage across inductors and current through capacitors, $\bar{K}$ is the capacitor and inductor matrix, and $\overline{M_x}$ is the time derivative matrix of inductor currents and capacitor voltages. Assuming that all capacitors are big enough that their voltages are fixed during switching period ($dV_{CI}^{ph}/dt = dV_{CO}^{ph}/dt = dV_{Bx}^{ph}/dt = 0$) and the voltage across these capacitors are $V_{CO}^{ph} = V, V_{CI}^{ph} = U$, and $V_{Bx}^{ph} = W_x$ during switching period. The voltage across ac (U)-and dc-side (V) capacitors are common for all submodules (see Fig. 1) but the voltage across the blocking (W_x) capacitor may be different if there is an overlap between the submodules. Therefore, (3) can be rewritten as follows:

$$\overline{M_v} = \left[\ V_{L11}^{ph}(t) \quad \dots \quad V_{Lx1}^{ph}(t) \quad V_{L12}^{ph}(t) \quad \dots \quad V_{Lx2}^{ph}(t)\ \right]^T \tag{4}$$

$$\overline{M_{di}} = \left[\ \frac{di_{L11}^{ph}(t)}{dt} \quad \dots \quad \frac{di_{Lx1}^{ph}(t)}{dt} \quad \frac{di_{L12}^{ph}(t)}{dt} \quad \dots \quad \frac{di_{Lx2}^{ph}(t)}{dt}\ \right]^T \tag{5}$$

$$\bar{\mathcal{L}} = \begin{bmatrix} L_{11}^{11} & \dots & L_{11}^{x1} & L_{11}^{12} & \dots & L_{11}^{x2} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ L_{x1}^{11} & \dots & L_{x1}^{x1} & L_{x1}^{12} & \dots & L_{x1}^{x2} \\ L_{12}^{11} & \dots & L_{12}^{x1} & L_{12}^{12} & \dots & L_{12}^{x2} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ L_{x2}^{11} & \dots & L_{x2}^{x1} & L_{x2}^{12} & \dots & L_{x2}^{x2} \end{bmatrix}. \tag{6}$$

In (4)–(6) the $\overline{M_v}$ matrix is reduced to contain only inductor voltages ($\overline{M_v}[2n \times 1]$), $\overline{M_{di}}$ is the derivation matrix ($\overline{M_{di}}$ $[2n \times 1]$) reduced to only contain the derivative of the inductor currents, and the coefficient matrix ($\bar{K}$) is reduced to inductance matrix ($\bar{\mathcal{L}}[2n \times 2n]$). In the inductance, the subscripts are the reference (victim) inductor, and the superscripts are the coupled (offender) ones in a mutual coupling relationship.

There can be $2n$ high-frequency modes in a module with n interleaved submodule of a ZVS-DMCR that are phase shifted by δ. The per unit phase shift for the xth submodules is $\delta_x = \frac{x}{n}\ \delta$. It should be noted that although the direction of inductor current changes the number of the switching networks is the same due to current bidirectional properties of the SiC MOSFET. There are 2^n unique permutations $\overline{M_v}$ matrix with n interleaved submodules, the occurrence and duration of which depends on duty cycle as it determines the overlap duration of submodules as shown in Fig. 5. The dc-side duty cycle is selected as reference (Ćuk' s half-bridge high-side is on the dc-side) and the ac-side is synchronous device on the low side. These modes have strong implications on the effect of interleaved module magnetic coupling, current sharing, and inductor current slope.

C. Electrical Circuit Analysis of the IIM

With n interleaved submodules there are three distinct types of magnetic coupling in the proposed IIM device that includes

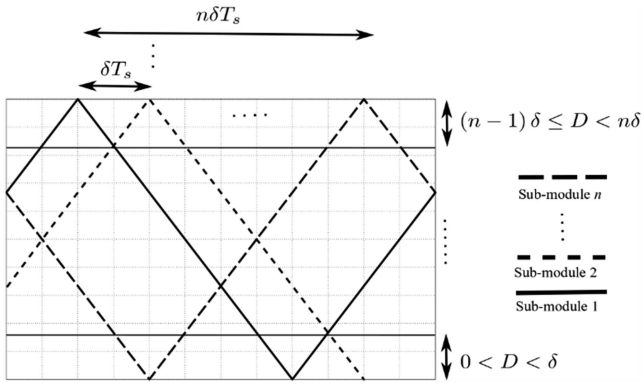

Fig. 5. Carrier signals of n interleaved submodules off set symmetrically by δ.

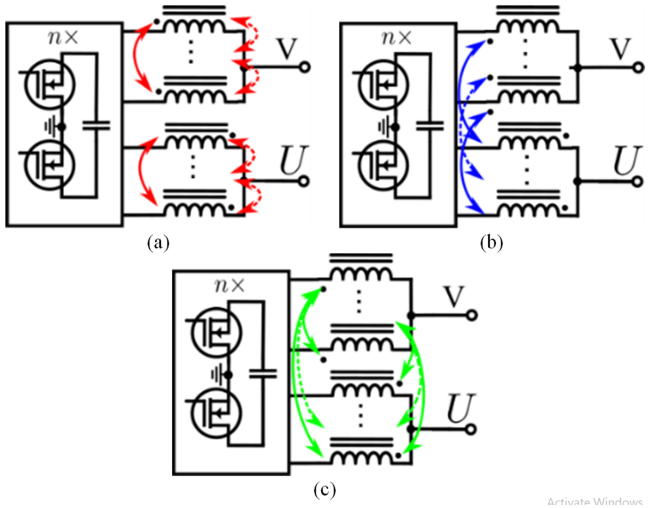

Fig. 6. Magnetic coupling type in the integrated interleaved device. (a) k_x coupling. (b) k_y coupling. (c) k_z coupling.

all inductors of a module. Fig. 6(a) shows the coupling between interleaved inductors of the same side (ac or dc). This is called intercoupling (with coupling factor k_x). Fig. 6(b) shows the coupling between ac-and dc-side inductors of the same ZVS-DMCR submodule. This is the conventional coupling in the Ćuk converter and will be called inner coupling (with coupling factor k_y). Finally, unwanted interaction of these two types of coupling results in a new type of coupling between inductors that are neither on the same side nor in the same submodule.

This type is called extra-coupling (with coupling factor k_z) and it is shown in Fig. 6(c). As explained in Section II-B, multiple unique voltage matrices across the inductors depend on the number of interleaved submodules. Electrically, the number of interleaved submodule will not change the general analysis, however, magnetically even, or odd number of submodules will impact the implementation in a two-dimensional magnetic design. Therefore, an example of 2 (even) and 3 (odd) interleaved submodules are analyzed herein.

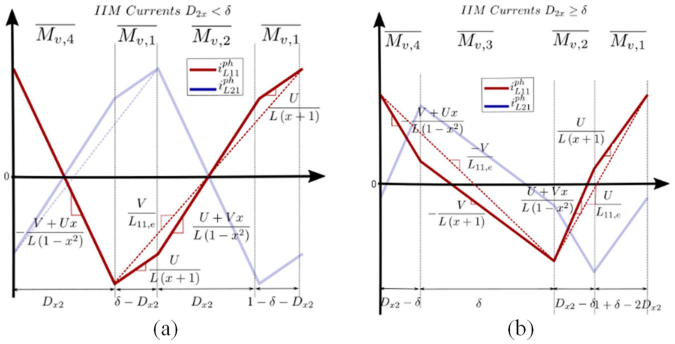

Fig. 7. Effect of k_x-coupling on the current ripple of the ZVS-DMCR with 2x interleaved submodules and the resultant effective inductance. (a) $D_{2x} < \delta$. (b) $D_{2x} \geq \delta$.

With 2x submodules, $n = 2, \delta = 1/2, L[4 \times 4], M_v[4 \times 1]$, and $M_{di}[4 \times 1]$. There are four unique M_v matrices as follows:

$$\begin{array}{c|c|c|c} \overline{M_{v,1}} & \overline{M_{v,2}} & \overline{M_{v,3}} & \overline{M_{v,4}} \\ \hline \begin{bmatrix} U \\ U \\ W_1 - V \\ W_2 - V \end{bmatrix} & \begin{bmatrix} U \\ U - W_2 \\ W_1 - V \\ -V \end{bmatrix} & \begin{bmatrix} U - W_1 \\ U - W_2 \\ -V \\ -V \end{bmatrix} & \begin{bmatrix} U \\ U \\ -V \\ W_3 - V \end{bmatrix} \end{array}. \quad (7)$$

These are permutations of the HF_1 and HF_2 modes shown in Fig. 4(b) and (c), respectively. The application of these four matrices obeys the following sequences depending on duty cycle. 1) $D_{x2} < \delta$, the combination of $\overline{M_{v,4}}$, $\overline{M_{v,1}}$, $\overline{M_{v,2}}$, and $\overline{M_{v,1}}$ with duration of D_{x2}, $\delta - D_{x2}$, D_{x2}, and $1 - \delta - D_{x2}$, respectively, is applied to the IIM. 2) $D_{x2} \geq \delta$ voltage matrices $\overline{M_{v,4}}$, $\overline{M_{v,3}}$, $\overline{M_{v,2}}$, and $\overline{M_{v,1}}$, with duration of $D_{x2} - \delta$, δ, $D_{x2} - \delta$, and $1 + \delta - 2D_{x2}$ respectively is applied to IIM.

In Fig. 7(a) and (b) the current ripples of the ac-side inductor in both interleaved submodules are shown for $D_{x2} < \delta$ and $D_{x2} \geq \delta$, respectively. To investigate the effect of k_x on the inductor ripples, $k_y = 0$, $k_z = 0$ is assumed. Effective inductances of positive and negative slopes can be derived as projected in Fig. 7. The effective inductances $L_{x1,e}$ and $L_{x2,e}$ are critically important since they are used in the determination and optimization of the resonance transition explained in Section II-D. $\overline{M_{v,4}}$ and $\overline{M_{v,1}}$ are the normal permutation of the Ćuk submodule without coupling (if $k_x = 0$), while $\overline{M_{v,2}}$ and $\overline{M_{v,3}}$ are emergent modes that are product of overlapping of interleaved submodules at the ac-and dc-side, respectively. These two new modes could produce either positive or negative slopes depending on their magnitude and sign of the coupling factor. The dc-side inductor currents $i^{ph}_{L12}(t)$ and $i^{ph}_{L22}(t)$ are not shown since in the absence of k_y they are identical to the ac-side inductors.

In the case of $3x$ submodules, $n = 3, \delta = 1/3, L[6 \times 6], M_v[6 \times 1]$, and $M_{di}[6 \times 1]$. There are eight unique M_v matrices as follows:

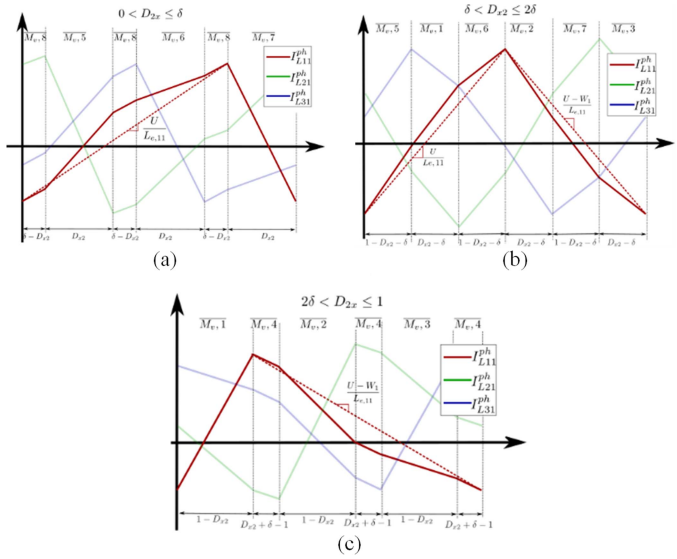

Fig. 8. The effect of k_x -coupling on the current ripple of the ZVS-DMCR with 2x interleaved submodules and the resultant effective inductance. (a) $0 < D_{2x} \leq \delta$. (b) $\delta < D_{2x} \leq 2\delta$ (c) $2\delta < D_{2x} \leq 1$.

$$\begin{array}{c|c|c|c} \overline{M_{v,1}} & \overline{M_{v,2}} & \overline{M_{v,3}} & \overline{M_{v,4}} \\ \hline \begin{bmatrix} U \\ U - W_2 \\ U - W_3 \\ W_1 - V \\ -V \\ -V \end{bmatrix} & \begin{bmatrix} U - W_1 \\ U \\ U - W_3 \\ -V \\ W_2 - V \\ -V \end{bmatrix} & \begin{bmatrix} U - W_1 \\ U - W_2 \\ U \\ -V \\ -V \\ W_3 - U \end{bmatrix} & \begin{bmatrix} U - W_1 \\ U - W_2 \\ U - W_3 \\ -V \\ -V \\ -V \end{bmatrix} \\ \hline \overline{M_{v,5}} & \overline{M_{v,6}} & \overline{M_{v,7}} & \overline{M_{v,8}} \\ \hline \begin{bmatrix} U \\ U - W_2 \\ U \\ W_1 - V \\ -V \\ W_3 - V \end{bmatrix} & \begin{bmatrix} U \\ U \\ U - W_3 \\ W_1 - V \\ W_2 - V \\ -V \end{bmatrix} & \begin{bmatrix} U - W_1 \\ U \\ U \\ -V \\ W_2 - V \\ W_1 - V \end{bmatrix} & \begin{bmatrix} U \\ U \\ U \\ W_1 - V \\ W_2 - V \\ W_3 - V \end{bmatrix} \end{array}. \quad (8)$$

Matrices defined in (8) are applied in sequence depending on the duty cycle.

1) $D_{x2} < \delta$, the combination of $\overline{M_{v,8}}$, $\overline{M_{v,5}}$, $\overline{M_{v,8}}$, $\overline{M_{v,6}}$, $\overline{M_{v,8}}$, and $\overline{M_{v,7}}$ with duration of $\delta - D_{x2}$, D_{x2}, $\delta - D_{x2}$, D_{x2}, $\delta - D_{x2}$, and D_{x2}, respectively.
2) $\delta < D_{x2} \leq 2\delta$ voltage matrices $\overline{M_{v,3}}$, $\overline{M_{v,1}}$, $\overline{M_{v,6}}$, $\overline{M_{v,2}}$, $\overline{M_{v,7}}$, and $\overline{M_{v,3}}$ with duration of $1 - D_{x2} - \delta, 2\delta + D_{x2} - 1, 1 - D_{x2} - \delta, 2\delta + D_{x2} - 1$, and $1 - D_{x2} - \delta$, respectively.
3) $D_{x2} > 2\delta$, voltage matrices $\overline{M_{v,1}}$, $\overline{M_{v,4}}$, $\overline{M_{v,2}}$, $\overline{M_{v,4}}$, $\overline{M_{v,3}}$, and $\overline{M_{v,4}}$, with duration of $1 - D_{x2}, D_{x2} + \delta - 2$, $1 - D_{x2}$, $D_{x2} + \delta - 2$, $1 - D_{x2}$, and $D_{x2} + \delta - 2$, respectively.

The graphical representation of these three cases and corresponding intervals with their slopes and effective inductances are shown in Fig. 8(a)–(c).

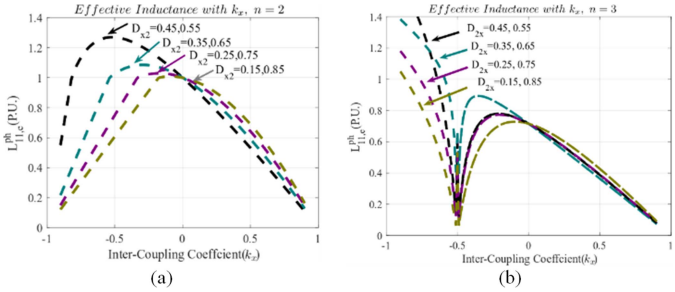

Fig. 9. Effect of the intercoupling coefficient (k_x) on the effective perunit inductances ($L^{ph}_{x1,e}(p.u.), L^{ph}_{x2,e}(p.u.)$) with variation in duty cycle for (a) 2x and (b) 3x- interleaved submodules.

The variation of effective inductance (per unit $L_{\text{Base}} = L_{ii}, i \in \{1, \ldots, 2n) \exists\ k_x = k_y = k_z = 0$) with k_x -coupling is shown in Fig. 9(a) and (b) for 2x and 3x interleaved submodules, respectively. These figures are drawn for $L_{11,e}$, however, since it is per unit and independent of time it will apply for all other inductors in the IIM. The effective inductance is calculated by numerically solving (3) initial conditions from the LF operation point, and boundary conditions from (7) or (8). The inductor current ripple is calculated from variation of inductor current during switching period ($\langle i^{ph}_{Lx1}(t)\rangle^{p2p}_{T_s}$ and $\langle i^{ph}_{Lx2}(t)\rangle^{p2p}_{T_s}$). So

$$L_{x1,e} = \frac{\left(1 - D^{ph}_{x2}(t)\right) \mathrm{V_m^{ph} T_s}}{\left\langle i^{ph}_{Lx1}(t)\right\rangle^{p2p}_{T_s}} \tag{9}$$

$$L_{x2,e} = \frac{\left(1 - D^{ph}_{x2}(t)\right) V^{ph}_{m} T_s}{\left\langle i^{ph}_{Lx2}(t)\right\rangle^{p2p}_{T_s}}. \tag{10}$$

In both *2x* and *3x* the higher intercoupling coefficients (k_x), in positive direction result in reduced effective inductance with stronger trends with higher *n*. Higher negative coupling ($k_x < -0.25$) are associated with nonlinear effective inductance that will result in unstable control response as well as unreliable ZVS regions. In the case of $n = 3$, there is a local extremum at $k_x = -0.5$ that should be avoided. Therefore, the most desirable region is around zero ($-0.1 < k_x < 0.1$), this will indicate that k_x coupling needs to be minimized in the integrated magnetic design.

The k_y coupling is independent of duty cycle and increasing it in the direction of flux cancellation increases the effective inductance linearly. This coupling is not affected by the number of interleaved sub-modules. Sufficient treatment of this coupling is presented in [44] and further discussion is avoided.

The existence of k_x and k_y coupling in an integrated magnetic inadvertently results in a third type of coupling between opposite side inductors of interleaved submodules. This is called extra-coupling (k_z coupling). This type of coupling depends on the value of k_x as well as k_y and is approximately (exactly if flux leakage through air is zero) their product ($k_z \leq k_x k_y$). In the operation of the ZVS-DMCR, the duty cycle changes according to the modulation scheme as shown in Fig. 2, therefore the k_x coupling need to be minimized while the k_y coupling compensate for the reduced effective inductance making the k_z approximately around the same values.

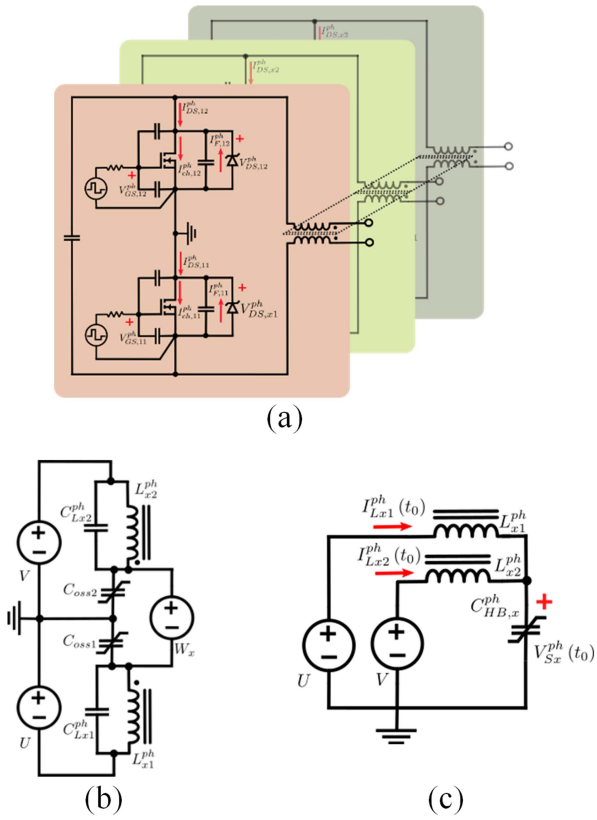

Fig. 10. (a) Detailed circuit of a single interleaved ZVS-DMCR module switching cell. (b) Equivalent circuit of a single ZVS-DMCR submodule switching cell during transition from mode HF1 to HF2 (T_{12}) and vice versa (T_{21}). (c) Simplified equivalent circuit when the switching transition time is much smaller than the switching period.

D. Soft-Switching Operation

The mechanism of soft-switching in ZVS-DMCR is through discharging the output capacitance of the incoming SiC MOSFET device before the turn-ON gate signal is applied to it. By doing this, the current will rise with zero voltage across the switch (it is actually equal to the forward drop of the parallel diode), this reduce/eliminate overlap time between voltage and current.

The detailed switching cell of a single module in the ZVS-DMCR is shown in Fig. 10(a) along with the equivalent circuit of a ZVS-DMCR submodule during switching transitions (T_{12} and T_{21} shaded areas in Fig. 4) in Fig. 10(b). During switching transition of Ćuk converter the ac- and dc-side inductor resonate with the parasitic capacitance connected to the mid-point of the half bridge. Since C^{ph}_I, C^{ph}_O, and C^{ph}_{Bx} are much larger compared with the parasitic capacitance of the half-bridge ($C^{ph}_{HB,x}$) they behave like a fixed voltage source across the half-bridge during the transition as shown in the equivalent circuit in Fig. 10(c). The equivalent parasitic capacitance of the half-bridge can be

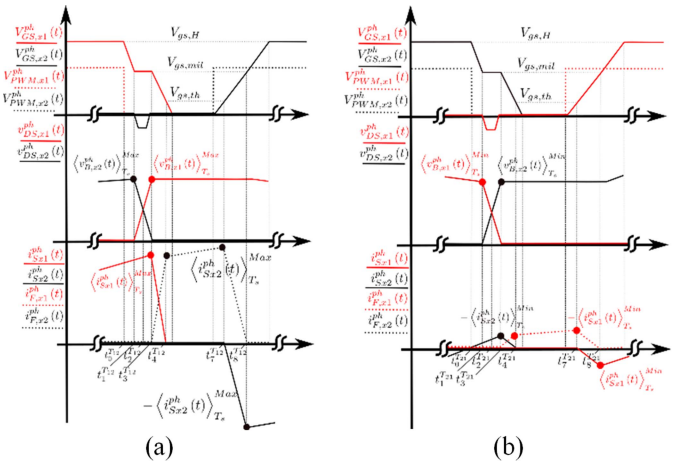

Fig. 11. SiC MOSFET voltage and current conceptual waveforms during TCM switching transition. (a) Transition event T_{12}. (b) Transition event T_{21}. Both of these transition events are shaded grey in Fig. 4(a).

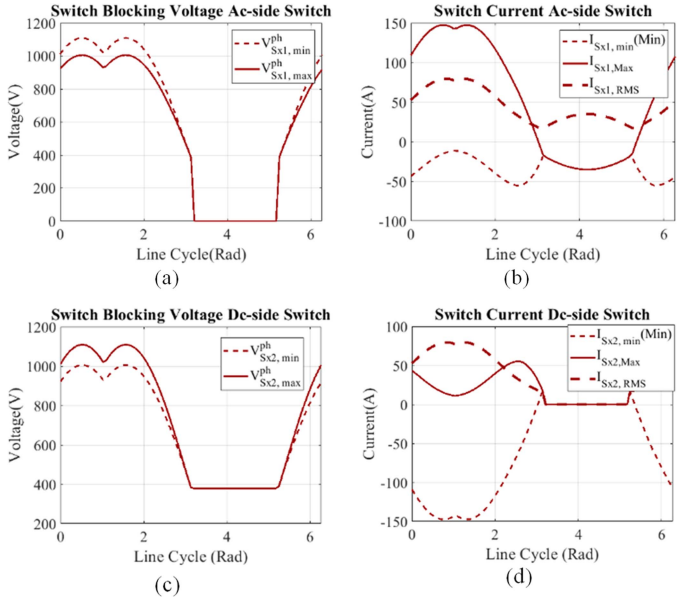

Fig. 12. Initial condition for voltage and current at the onset of the switching transitions at the operation point, OP_2 : $\{T_s = 20\ \mu\text{s}, G^{\max} = 0.68, V^{ph} = 480\ \text{V}, R_L = 4.167\ \Omega\}$. (a) AC-side switch voltage. (b) AC-side switch current. (c) DC-side switch voltage. (d) DC-side switch current.

calculated as follows:

$$C^{ph}_{HB,x} = C^{ph}_{oss1}\left(V^{ph}_{Sx1}\right) + C^{ph}_{oss2}\left(V^{ph}_{Sx2}\right) + C^{ph}_{Lx1} + C^{ph}_{Lx2}. \tag{11}$$

In (11), $C^{ph}_{oss1}(V^{ph}_{Sx1})$ and $C^{ph}_{oss2}(V^{ph}_{Sx2})$ are the voltage dependent capacitance of ac- and dc-side devices. C^{ph}_{Lx1} and C^{ph}_{Lx2} are parasitic capacitance of the ac- and dc-side inductors. Using the charge equivalent method presented in [48] for the voltage dependent capacitances, (11) can be rewritten as follows:

$$C^{ph}_{HB,x} = 2C^{ph}_{Qeq}(W_x) + 2C^{ph}_{Lx}. \tag{12}$$

In the Ćuk half-bridge unlike other basic converters the resonance is aided by two inductors instead of one. The device waveforms of a single submodule [see Fig. 10(b)] during switching transitions (T_{12} and T_{21}) are shown in Fig. 11. It should be noted that these conceptual waveforms are drawn in piecewise linear form for better comprehension. The actual voltage and current transition during TCM are governed by the following differential equations:

$$C^{ph}_{HB,x}(W_x)\ \frac{dv^{ph}_{sx2}}{dt} = i^{ph}_{Lx1} + i^{ph}_{Lx2} \tag{13}$$

$$L_{x1,e}\ \frac{di^{ph}_{Lx1}}{dt} = -V^{ph}_{Sx2} + W_x - V \tag{14}$$

$$L_{x2,e}\ \frac{di^{ph}_{Lx2}}{dt} = -V^{ph}_{Sx2} + U. \tag{15}$$

In (13)–(15) $L_{x1,e}$ and $L_{x2,e}$ [from (9) and (10)] are effective inductance of ac-and dc-side of submodule *x,* and $C^{ph}_{HB,x}$ is the switching cell parasitic capacitance [from (12)]. Using superposition, the resonance equation can be solved for each source while the other one is shorted (nulled). These equations can be solved numerically with the initial conditions of the $v^{ph}_{Sx2}\ (t_1^{T_{12}}) = V^{ph}_{Bx,\max}$, $i^{ph}_{Lx1}\ (t_7^{T_{12}}) = I^{ph}_{Lx1,\max}$, and $i^{ph}_{Lx2}\ (t_7^{T_{12}}) = I^{ph}_{Lx2,\max}$ at turn-ON transition of S_{x2} (and turn-OFF transition of S_{x1}) conceptually described in Fig. 11(a). Similarly, the initial condition for the turn-OFF transition of S_{x2} (turn-ON transition of S_{x1}), conceptually described in Fig. 11(b), is $v^{ph}_{Sx2}\ (t_1^{T_{21}}) = V^{ph}_{Bx,\min}$, $i^{ph}_{Lx1}\ (t_7^{T_{21}}) = I^{ph}_{Lx1,\max}$, and $I^{ph}_{Lx2}\ (t_7^{T_{21}}) = I^{ph}_{Lx2,\max}$. Between $t_3^{T_{12}}(t_3^{T_{21}})$ and $t_7^{T_{12}}(t_7^{T_{21}})$ inductor and switch current keep rising (falling) with the same slope since the switch network does not change during this time. However, if the transition times (rise and fall) is much smaller than the switching period the maximum and minimum inductor and switch current does not change significantly and equivalent circuit for one submodule can be redrawn as shown in (b). The voltage across the equivalent parasitic capacitance of the half-bridge is the blocking capacitor voltage. All these initial condition along the line cycle for OP_2 : $\{T_s = 20\ \mu\text{s}, G^{\max} = 0.68, V^{ph} = 480\ \text{V}, R_L = 4.167\ \Omega\}$ is shown in Fig. 12(a) and (b) for the ac-side device and Fig. 12(c) and (d) for the dc-side device. Appropriate deadtime and reverse current for each switching operating point needs to be ensured according to these initial conditions. In Fig. 13(top) the require negative current (with fixed $T_{db} = 0.05T_{sw}$) is shown to fully discharge the $C^{ph}_{HB,x}$ compared to the available negative current at OP_3 (worst-case scenario). Since in this converter the reverse current makes up an insignificant portion of the inductor (switch) current ripples a fixed frequency is used across the line cycle corresponding to the peak required negative current. In doing so all the complications related to variable switching frequency is avoided (complex double modulation control, complicated EMI spectrum, extended subharmonic losses, etc.). The frequency however is changed discretely depending on the ZVS-DMCR operating condition. In Fig. 13(bottom) an example of discrete changes to switching frequency for various output power.

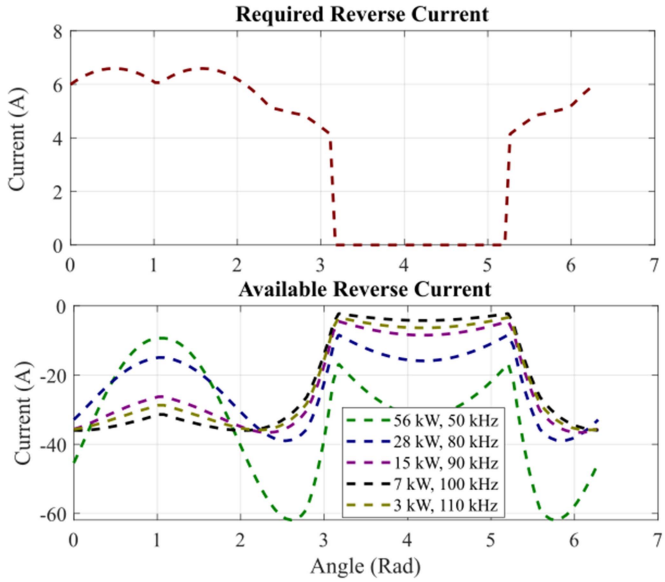

Fig. 13. The ZVS requirements in the low-frequency line cycle. The available reverse current at $OP_3 : \{T_s = 209\,\mu s$ (for the bottom figure), $G^{\max} = 0.68$, $V^{ph} = 480$ V, $R_L = 460\,\Omega\}$.

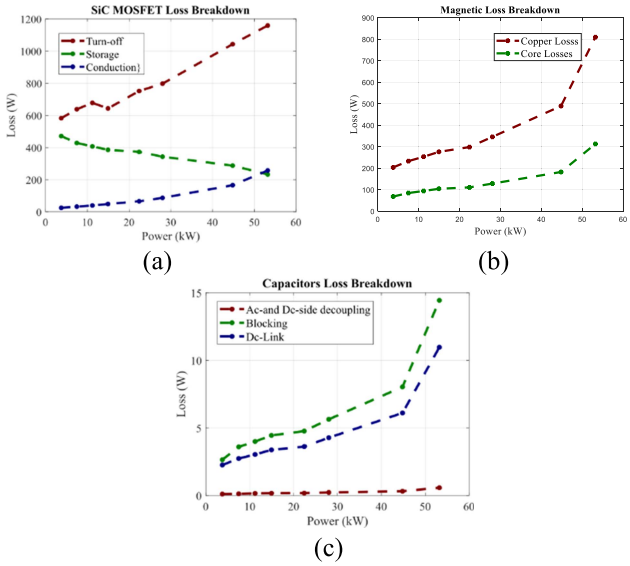

Fig. 14. Loss breakdown of ZVS-DMCR in rectifier operation point $OP_3 : \{ T_s = 209\,\mu s, G^{\max} = 0.68, V^{ph} = 480$ V, $R_L = 460\,\Omega\}$ with load change. (a) SiC MOSFET loss. (b) Magnetic loss. (c) Capacitor loss.

E. Loss Breakdown

To evaluate the improvement the impact of the soft switching as well as the IIM in the overall loss of the PES a loss analysis is conducted on the magnetics, semi-conductor devices, and capacitors. Other loss components, e.g., gate driver loss, PCB losses, and cable losses are insignificant compared to the overall power of the PES. This analysis is conducted with the specifications given in Table I as general parameter.

1) Semiconductor Device: The semiconductor device used in ZVS-DMCR is 1.7 kV six pack SiC MOSFET (MSCSM170TAM15CTPAG). The loss analysis is conducted with assumptions relevant to this device.

Multiple publications have address SiC MOSFET losses in details, in this section, the methodology for the analysis is adopted from papers [12], [48], [49], and [50]. There are three major components of device loss analyzed distinctly in this section, namely, turn-OFF overlap loss ($P_{\text{Off},VI}$), storage loss (P_{oss}), and conduction loss (P_{cond}). Turn-ON overlap loss ($P_{\text{On},VI}$) and reverse recovery loss (P_{rr}) are assumed to be negligible due to application of ZVS. In this section, the notation and waveforms of the switching transition presented in Section II-D is adopted. The losses are calculated based on the LF initial condition for each switching transition event. These initial condition for switch voltage and current is presented in Fig. 12 after calculating the loss for each event the final loss for the ZVS-DMCR is calculated by averaging all loss events over the LF cycle. Overlap losses can be written as follows:

$$P^{ph}_{sx1,\text{off}} = \frac{1}{2}\left\langle f_s \left(t^{T_{12}}_{fi} + t^{T_{12}}_{rv}\right) V^{ph}_{Bx,\max} I^{ph}_{chx1,\text{off}} \right\rangle^{\text{Ave}}_{T_g} \tag{16}$$

$$P^{ph}_{sx1,\text{on}} = \frac{1}{2}\left\langle f_s \left(t^{T_{21}}_{ri} + t^{T_{21}}_{fv}\right) V^{ph}_{Fx1} I^{ph}_{chx1,\text{on}} \right\rangle^{\text{Ave}}_{T_g} \tag{17}$$

$$P^{ph}_{sx2,\text{off}} = \frac{1}{2}\left\langle f_s \left(t^{T_{21}}_{fi} + t^{T_{21}}_{rv}\right) V^{ph}_{Bx,\min} I^{ph}_{chx2,\text{off}} \right\rangle^{\text{Ave}}_{T_g} \tag{18}$$

$$P^{ph}_{sx2,\text{on}} = \frac{1}{2}\left\langle f_s \left(t^{T_{12}}_{ri} + t^{T_{12}}_{fv}\right) V^{ph}_{Fx2} I^{ph}_{chx2,\text{on}} \right\rangle^{\text{Ave}}_{T_g}. \tag{19}$$

In (16)–(19), $t^{T_{12}}_{fi} = t^{T_{12}}_{4} - t^{T_{12}}_{3}, t^{T_{12}}_{ri} = t^{T_{12}}_{8} - t^{T_{12}}_{7}, t^{T_{12}}_{rv} = t^{T_{12}}_{fv} = t^{T_{12}}_{3} - t^{T_{12}}_{1}$ are transition times from T_{12} and $t^{T_{21}}_{fi} = t^{T_{21}}_{4} - t^{T_{21}}_{3}, t^{T_{21}}_{ri} = t^{T_{21}}_{8} - t^{T_{21}}_{7}, t^{T_{21}}_{rv} = t^{T_{21}}_{fv} = t^{T_{21}}_{3} - t^{T_{21}}_{1}$ are transition times from T_{21} in Fig. 11. $I^{ph}_{chx1,\text{on}}$ and $I^{ph}_{chx2,\text{on}}$ are channel currents of the ac-and dc-side switches in turn-ON transition and $I^{ph}_{chx1,\text{off}}$ and $I^{ph}_{chx2,\text{off}}$ are channel currents of ac-and dc-side switches in the turn-OFF transition. Second-order charge equation of the device introduced in [50] are solved iteratively with the datasheet curves of the SiC MOSFET and the designed gate driver values that are tested experimentally. The datasheet values can be found in [43] and the gate driver parameters are, $R_{g.\text{int}} = 1.96\,\Omega$, $R_{g,\text{ext}} = 2.96\,\Omega, V_{gs,H} = 17$ V, $V_{gs,L} = -4$ V, and $I_{g,\max} = 10$ A. V^{ph}_{Fx1} and V^{ph}_{Fx2} are forward drop of the SiC MOSFET'S anti-parallel diode [in (17) and (19) it is assumed that the negative current provided to discharge the parasitic capacitance of the half-bridge is high enough that the diodes are turned ON]. f_s is the switching frequency and $\langle \blacksquare \rangle^{\text{Ave}}_{Tg}$ indicates average function over the grid period (T_g).

The storage losses of the SiC MOSFET can be complicated to calculate. Following the example of [50] the losses due to charge/recharge of the C_{oss} could be 20% of the total charge energy. In this calculation the energy equivalent capacitance [48] of the device is used

$$P^{ph}_{oss} = (20\%)\,\frac{1}{2}\left\langle 2 f_s C^{ph}_{Eeq} \left(V^{ph}_{Bx,\max}\right)\left(V^{ph}_{Bx,\max}\right)^2 \right\rangle^{\text{Ave}}_{T_g}. \tag{20}$$

In (20), $C_{Eeq}^{ph}(V_{Bx,\max}^{ph})$ is the energy equivalent capacitance of the submodule half bridge at $V_{Bx,\max}^{ph}$. The reverse recovery in a PIN diode occurs when it is conducting current in the forward direction immediately before it is blocking voltage. It depends on datasheet parameters of the diode as well as the magnitude of the forward current and reverse voltage [50]. In TCM converter such scenarios will not occur because the diode always transfers the current to the device during the turn-ON period of both devices.

The conduction loss is calculated by calculating the RMS of the switch current and using the $R_{ds}(on)$ of the device at ambient temperature ($T = 25$ °C), using the following equation:

$$P_{\text{cond}}^{ph} = R_{ds,\text{on}}\left(\left\langle\left\langle i_{Sx1}^{ph}\right\rangle_{T_s}^{RMS^2}\right\rangle_{\text{Tg}}^{\text{Ave}} + \left\langle\left\langle i_{Sx2}^{ph}\right\rangle_{T_s}^{\text{RMS}^2}\right\rangle_{\text{Tg}}^{\text{Ave}}\right) \tag{21}$$

In (21) $\langle\blacksquare\rangle_{Ts}^{\text{RMS}}$ is the RMS of the switch current over the switching period. All of these losses are shown in Fig. 14 along the ZVS-DMCR power level with variation of load current at OP_3 : $\{T_s = 209\ \mu\text{s}, G^{\max} = 0.68, V^{ph} = 480\ V, R_L = 460\ \Omega\}$. The switching frequency is designed for each discrete power level to ensure ZVS at the worst operation condition on the line scale, therefore it is assumed that the turn-ON loss is zero for both switches at all times which comes at the price of the more conduction loss.

2) Integrated Interleaved Magnetics: The inductor losses are calculated for integrated interleaved design as optimized in Section III. The analytical initial condition for the IIM switching cycle is adopted from Section II-A and the current waveforms is derived from electrical analysis of the IIM in Section II-C. The specifications used for the current waveforms are according to the minimum inductance required for TCM presented in (9) and (10). The flux balance and swing inside the magnetic core is calculated using the optimized design and the reluctance model introduced in Section III. The core losses are calculated using the Nanocrystalline material's manufacturer datasheet curves. The loss profile with operation point of DMCR is shown in Fig. 14(c).

3) Capacitor Losses: The design/selection of the high-frequency capacitors that have to endure a high current ripple at the ac- and dc-sides of a module is critical. The analytical waveforms of blocking and ac-/dc-side capacitors with $3x$ interleaved submodules with the coupling matrix presented in (14) are shown in Fig. 15(a). Due to symmetrical interleaving ($\delta = 1/n$) the ripples are canceled in the module level and the capacitors experience canceled ripples at T_s/n periods. These waveforms are calculated assuming perfect interleaving and using the model presented in Section II-C. This assumption is verified by experimental measurements shown in Fig. 15(b). Moreover, ac-and dc-side capacitors experience the same high-frequency current ripples as shown in Fig. 15(a), since they both have equivalent inductance and symmetrical voltage, thanks to the ZVS-DMCR topology. It should be noted that while the HF current ripple is equal, the LF voltage across them are different, the ac capacitor is biased by the modular voltage following the duty cycle's shape (see Fig. 2), while the dc-side biased by the dc battery voltage. Interleaving on both ends of the converter will improve the electromagnetic compatibility of the converter as well as reducing the size of the capacitors used in the converter. The specifications for the experimental capacitors C_I^{ph} and C_O^{ph} are shown in Table III.

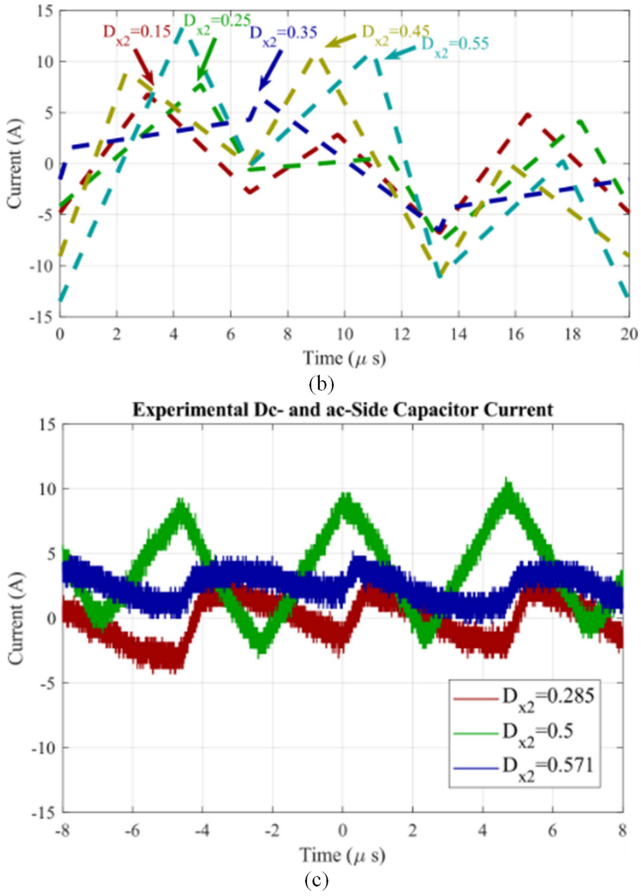

Fig. 15. Variation of the capacitor ripple waveforms with duty cycle along the line cycle used for designing the capacitors. (a) Analytical AC-and DC-side capacitor currents. (b) Analytical blocking capacitor. (c) Experimental AC- and DC-side capacitor current. All captured at several instances of the line cycle (LF) and plotted simultaneously.

TABLE III
SPECIFICATIONS OF THE ZVS-DMCR EXPERIMENTAL CAPACITORS

Parameter	C_I^{ph}	C_O^{ph}	C_{Dc}	C_B^{ph}
Type	Ceramic	Film	Electrolytic	Film
# Parallel	7	6	12	4
Capacitance	0.98 µF	30 µF	4000 µF	2.24 µF
ESR	0.22 mΩ	1.5 mΩ	33.1 mΩ	0.35 mΩ
ESL	0.1 nH	4.16 nH	N.A.	4.5 nH
Max HF Ripple	395 A @ 100 kHz	213 A @ 10 kHz	2.75 A @ 100 Hz	840 A @ 100 kHz
Max Bias Voltage	1200 V	1100 V	600 V	1600 V
Volume	~5.1 cm^3	~19 cm^3	~439 cm^3	~104 cm^3

The displacement current through the blocking capacitor is also shown in Fig. 16 informed by the modes presented in Section II-C and the specifications of the physical components is shown in Table III for each submodule. This is one of the critical components of the ZVS-DMCR and needs to be designed/selected carefully. It needs to transfer the energy from

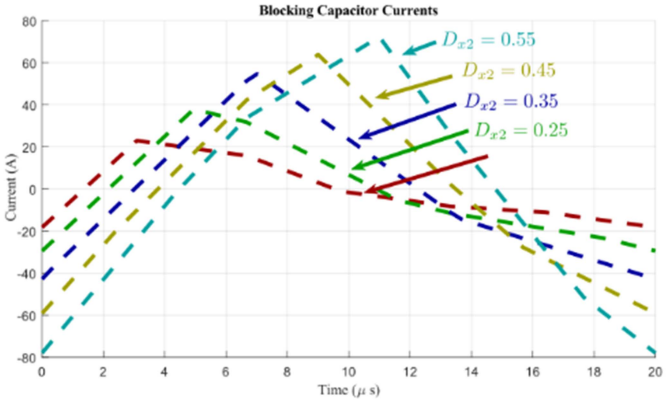

Fig. 16. Analytical blocking capacitor (C_B^{ph}) currents with variation in duty cycle representing its evolution along the line-cycle.

input to output side while maintaining the voltage across the Ćuk half bridge, while charging and discharging the parasitic capacitance of the half-bridge through the inductors. Therefore, it needs to have low ESR/ESL while blocking high voltage and maintain its capacitance under line cycle variation.

III. Integrated Interleaved Magnetics Design

In the context of the analyzed converter an IIM is proposed to fabricate all inductor of each module is a single magnetic structure. The purpose of this approach is 1) leverage the symmetrical topology of Ćuk converter for magnetic integration that increase both efficiency and power density and 2) integrate all the inductors that are added to the converter through interleaving to avoid increasing the size of the magnetics while maintaining TCM. In doing so, the increased number of inductors from added submodules are managed simultaneous while efficiency improved through TCM. In this section a step-by-step design process is introduced for the IIM to materialize the idea for n interleaved submodules. A flowchart is presented in Fig. 17 to illustrate all steps in a single repeatable algorithm. A design example process is presented with a 3x interleaved submodules with a numerical example in each step. That being said the general idea can be extended to higher number of submodules.

A. Reluctance Analysis

The purpose of this magnetic device, as it was discussed in Section II-C, is to integrate $2n$ inductors (with three distinct types of coupling) while maintaining high current ripple from TCM operation. As discussed therein, the coupling between windings on the same side of interleaved submodules need to be limited ($-0.1 < k_x < 0.1$) to avoid effective inductance reduction, while it is desired to maximize k_y. Windings of ac-and dc-side inductors of the same submodule are wound on the same limb nonoverlapped to achieve a tight coupling, hence the vertical limbs. The degree in which each limbs shares flux with the other is governed by interlimb links and airgaps that will control k_x. Finally, two C-shape leakage paths are devised to avoid flux crowding in a single limb.

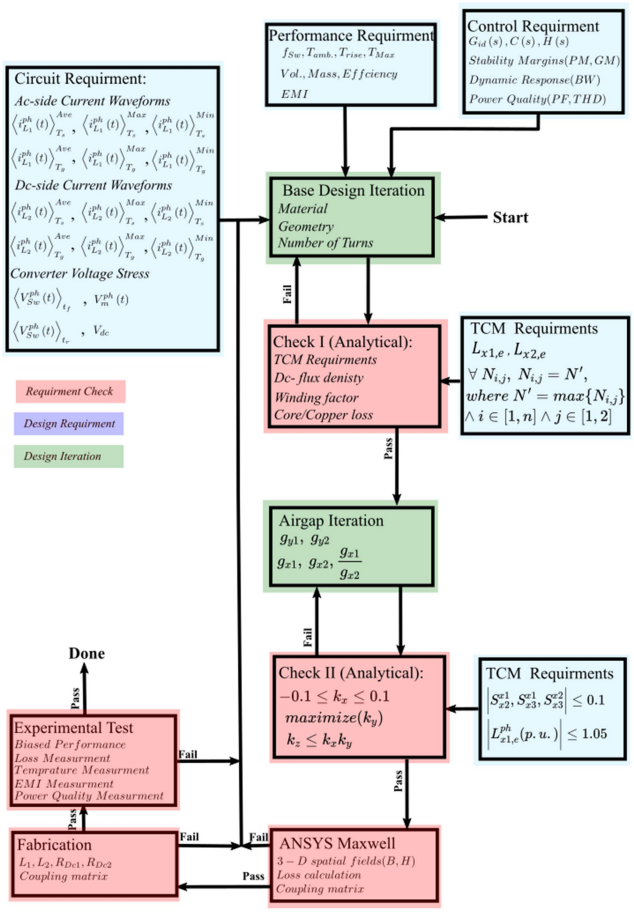

Fig. 17. Integrated magnetics design algorithm for ZVS-DMCR.

TABLE IV
Properties of the Nanocrystalline Alloy Used in the Design

Parameter	Value
Resistivity	1.2 $\mu\Omega$m
Saturation Flux Density	1.23 T
Density	7300 Kg/m^3
Loss (At 100 ℃, 100 kHz, 200 mT)	~300 kW/m^3
Initial Permeability (At 100 kHz)	$\geq$ 60000
Ribbon Thickness	17.78 μm
Curie Temperature	570 ℃

Nanocrystalline core material is used in this design through its high saturation flux density and relative permeability. The implementation of discrete-distributed air gaps to sustain the high current ripple will reduce the permeability significantly, therefore having high zero bias permeability is important in this design. The properties of the material used for this design is shown in Table IV.

The geometry and physical dimensions shown in Fig. 18(a) is proposed for IIM. This topography maintains maximum possible design symmetry in a two-spatial dimensions for magnetic design (x and y) while offering modularity for expanding number of submodules (any number of submodules can be added or removed). This geometry is symmetrical in all three cartesian coordinate direction as it is shown in Fig. 18(b). The

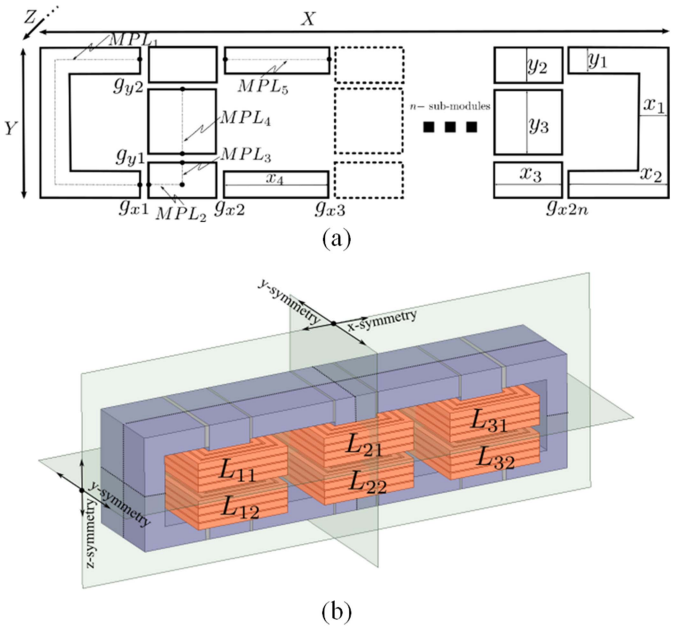

Fig. 18. Proposed magnetic geometry for the IIM. (a) Physical marking of dimensions. (b) Demonstration of spatial symmetry.

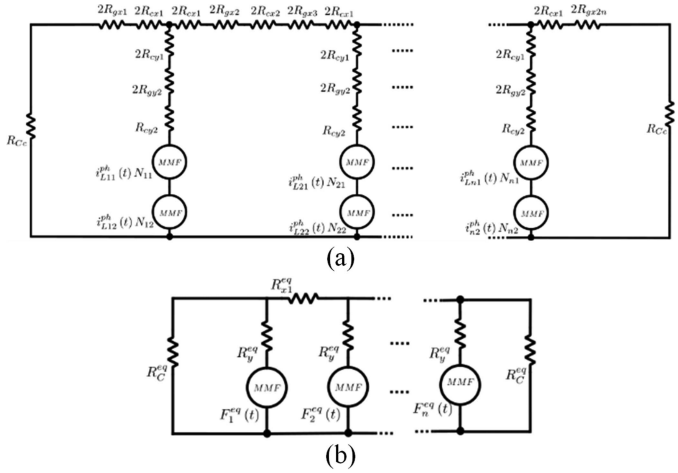

Fig. 19. (a) Reluctance circuit of the integrated interleaved magnetics with n-interleaved submodules. (b) Simplified equivalent circuit.

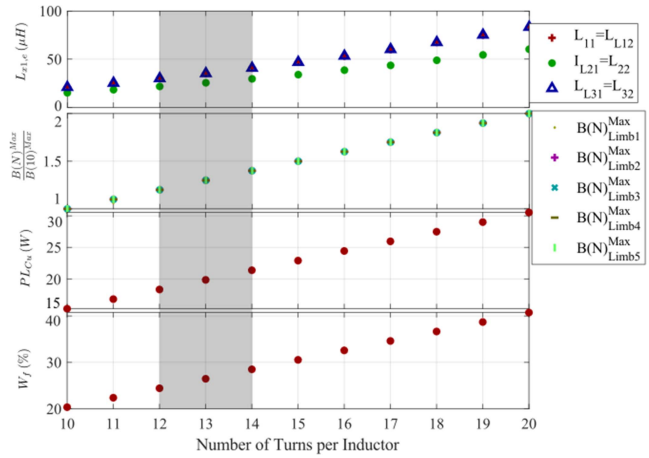

Fig. 20. Variation of the key IIM specifications with variation in number of turns and desired range of turns. (Top) graph shows the effective inductance of the submodules ($L_{x1,e} = L_{x2,e}$), (upper mid) shows the ratio of maximum flux density for N number of turns to the lowers $N = 10$ $\left(\frac{B(N)^{\text{Max}}}{B(10)^{\text{Max}}}\right)$, (lower mid) shows core losses (PL_{Cx}), (bottom) shows the percentage of the window areas of the IIM occupied by copper (W_f).

C-shape core pieces (without windings) of both ends of the IIM contain the field within the IIM serving as flux relief and leakage path. Central limbs ($n(=3)$ piece) houses both ac- and dc-side inductor windings of a single submodule while the horizonal limbs are used to control the coupling between the interleaved submodules. The IIM with *n* interleaved submodules includes *n* central limbs, *4(n+1)* horizontal airgaps, *2n* vertical airgaps, *3* unique vertical size variables, *2n* coils (windings), *n+1* winding windows, and $0.5(n+1)(n+2)$ reluctance loops. The total length, height, and depth are represented by *X*, *Y*, and *Z*, respectively. There are five unique mean path length (*MPL*) types, $MPL_1 = 2x_2 - x_1 + 2y_2 + y_3 - y_1$, $MPL_2 = 0.5x_3$, $MPL_3 = 0.5y_2$, $MPL_4 = y_3$, and $MPL_5 = x_4$ as marked on Fig. 18(a). The total box dimensions (ignoring the airgaps) are $(2x_2 + (n-1)x_4 + nx_3, y_3 + 2y_2, Z)$. The design is only changes in the *X* dimension when adding submodules and the other two remains fixed.

The reluctance circuit for this magnetic device is shown in Fig. 19(a). The reluctance of the *C*-shape piece on both ends is $R_{Cc} = \frac{MPL_1}{\mu_r \mu_0 y_1 Z}$, two unique horizonal core pieces have the reluctance of $R_{cx1} = \frac{MPL_2}{\mu_r \mu_0 y_2 Z}$ and $R_{cx2} = \frac{MPL_5}{\mu_r \mu_0 y_1 Z}$, two unique vertical core pieces have the reluctances of $R_{cy1} = \frac{MPL_3}{\mu_r \mu_0 x_3 Z}$ and $R_{cy2} = \frac{MPL_4}{\mu_r \mu_0 x_3 Z}$. Vertical airgap reluctances are $R_{gy1} = \frac{g_{y1}}{\mu_0 x_3 Z}$ and $R_{gy2} = \frac{g_{y2}}{\mu_0 x_3 Z}$, horizontal airgap reluctances are $R_{gx1} = \frac{g_{x1}}{\mu_0 x_1 Z}$, …, $R_{gx2n} = \frac{g_{x2n}}{\mu_0 x_1 Z}$ which are the main design control for the intercoupling (k_x) between interleaved submodules. A simplified equivalent is shown in in Fig. 19(b), where, $R^{eq}_C = R_{Cc} + 2(R_{gx1} + R_{cx1})$, $R^{eq}_y = R_{cy2} + 2R_{cy1} + R_{gy1} + R_{gy2}$, $R^{eq}_{x1} = 4R_{cx1} + 2(R_{gx2} + R_{cx2} + R_{gx3})$, and $F^{eq}_x(t) = N_{x1}\, i^{ph}_{Lx1}(t) + N_{x2} i^{ph}_{Lx2}(t)$. The k_y coupling between ac-and dc-side of the same submodule is positive for flux cancellation.

The minimum and maximum inductance to maintain ZVS and avoid extra losses for the operation frequency range (20–9 μs) can be calculated from (9) and (10). The limit is determined by the worst operating point in the OP_3 to be $35\ \mu\text{H} \le L \le 40\ \mu\text{H}$. The effective inductance seen by each winding (with all the coupling considered), in the reluctance equivalent circuit, is inversely proportional to the Thevenin reluctance seen from that winding when other MMF sources are shorted (nulled). For 3x submodules

$$R^{\text{th}}_{11} = \left[\left[\left(R_{\text{aux}} \parallel R^{\text{eq}}_y\right) + R^{\text{eq}}_x\right] \parallel R^{\text{eq}}_c\right] + R^{\text{eq}}_y \quad (22)$$

$$R^{\text{th}}_{21} = \left(R_{\text{aux}}/2\right) + R^{\text{eq}}_y \quad (23)$$

$$R_{\text{aux}} = \left(R^{\text{eq}}_c \parallel R^{\text{eq}}_y\right) + R^{\text{eq}}_x. \quad (24)$$

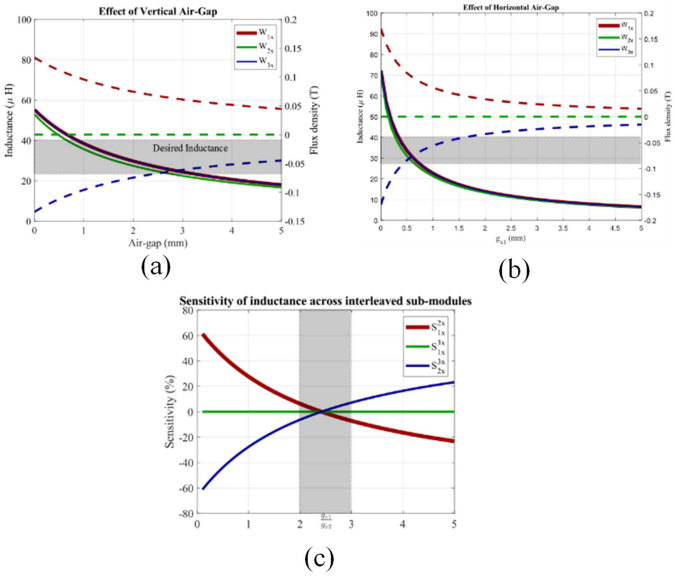

Fig. 21. Inductance variation in the IIM proposed structure with (a) vertical and (b) horizonal airgap. (c) The sensitivity of inductance of each submodules with the changes in vertical to horizontal air gap.

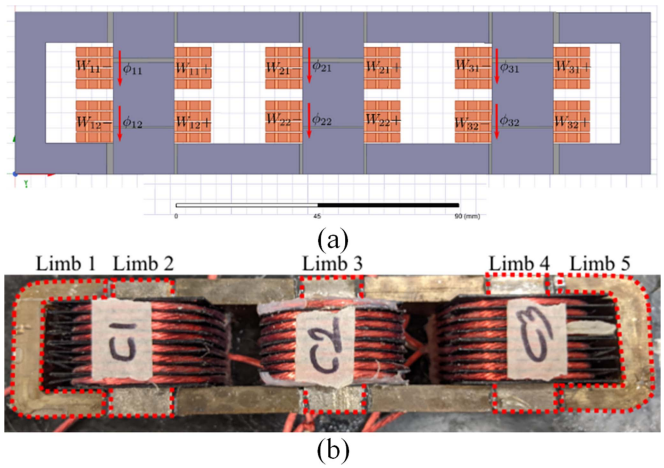

Fig. 22. (a) 3-D model of the IIM core and winding in MAXWELL. (b) Experimentally fabricated IIM.

The rest of the winding have equivalent inductance equal to either (21) or (23), i.e., $R_{11}^{\text{th}} = R_{12}^{th} = R_{31}^{\text{th}} = R_{32}^{\text{th}}$ and $R_{21}^{\text{th}} = R_{22}^{\text{th}}$ With (*X, Y, Z*) limits demanded by the packaging and maintaining power density (with specifications presented in Table I) the following is selected for the physical dimensions of the IIM referenced to Fig. 18(a), $x_1 = 10$ mm, $x_2 = 30$ mm, $x_3 = 20$ mm, $x_4 = 40$ mm, $y_1 = 10$ mm, $y_2 = 10$ mm, $y_3 = 21$ mm, and $Z = 40$ mm.

B. Winding

The number of turns is constrained by the fill factor and the desired effective inductance under load to realize the TCM operation (the later determined in Section III-A to be, $35\ \mu\text{H} \leq L \leq 40\ \mu\text{H}$). Assuming the custom core structure analyzed in Section III-A and defaulting all air gaps of the magnetic geometry to 1 mm, the number of turns is determined. To maintain

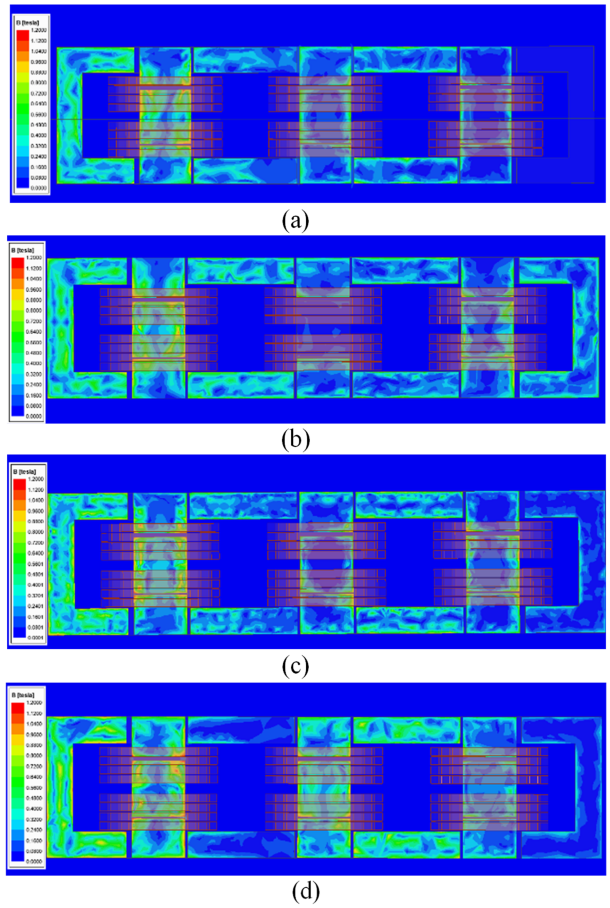

Fig. 23. Flux density distribution at four different instances on the line cycle simulated with FEA in Maxwell. (a) $D_{2x} = 0.25$. (b) $D_{2x} = 0.35$. (c) $D_{2x} = 0.45$. (d) $D_{2x} = 0.55$.

maximum symmetry in magnetic fields while adhering to the inherent symmetry of the Ćuk converter number of turns are desired to be equal in all windings. This is further motivated by the ZVS strategy utilized here, in which, the current ripple of both ac-and dc-side needs to be approximately equal to ensure negative current in all LF operation modes (this is evident in Figs. 2 and 3 where the direction of the current change in LF modes). This means, $N_{11} = N_{21} = N_{31} = N_{12} = N_{22} = N_{32} = N$. According to the previous analysis, *N* can be initialized with the following:

$$N = \sqrt{L_{x1,e} R_{11}^{\text{th}}} \tag{25}$$

$$N' = \sqrt{L_{x1,e} R_{21}^{\text{th}}}\ . \tag{26}$$

In (25) and (26), N and N' shows the number of turns to achieve the desired inductance in the middle limb and the side limbs, respectively. However, as stated earlier, to maximize the symmetry in it, it is desired to keep the number of turns equal for all windings. Therefore, the number of turns are designed on a spectrum in a healthy tradeoff with losses, maximum flux density, and winding factor. The variation of these parameters is shown with changing N from 10 to 20 [inspired by (25) and

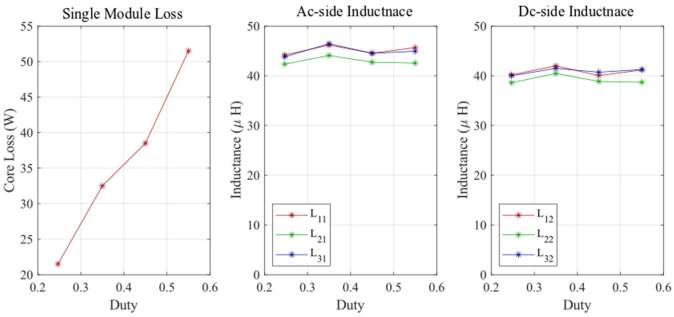

Fig. 24. IIM losses and inductance with variation of duty cycle along the line cycle.

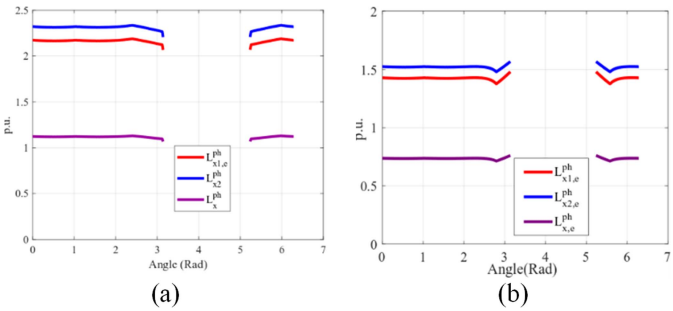

Fig. 25. Effective inductance of AC-and DC-side inductors with inductance matrices presented in (14) and (15) for (a) 2x and (b) 3x interleaved submodules, respectively.

(26)], which is approximated in the desired properties for IIM, in Fig. 20. The flux density is shown as per unit of the first number for N to disassociate its value from operation point $OP_4(\ T_s = 17.5\ \mu\text{s}, D_{2x} = 0.5, V_{\text{dc}} = 500\ \text{V},\ R_L = 15\ \Omega)$. Litz wire ($475\ \times\ AWG\#40$) is selected to minimize ac copper losses at highest switching frequency and maximize the window area used (Litz wire design details of the design are omitted for sake of brevity).

C. Airgap Tuning and Optimization

It is highly desirable to have equal effective inductances for all interleaved submodules to avoid current sensor in each limb as well as balanced flux distribution in the core. Aside from having highly symmetrical magnetic structure and switching converter, the vertical air gaps heavily affect the effective inductance of the submodule as well as the flux density in the limb. Effect of variation of g_{y2} when all horizontal air gaps are fixed at 1 mm and $g_{y1} = 0.5$ mm, with winding inductance and flux density is shown in Fig. 21(a) for one module at $OP_5(\ T_s = 12\ \mu\text{s}, D_{2x} = 0.5, V_m^{ph} = 500\ \text{V}, R_L = 4.167\ \Omega)$.

The vertical airgap of 2 mm is selected with distribution of $g_{y1} = 0.5$ mm, $g_{y2} = 1.5$ mm to keep both the flux density and effective inductance within the desired grey area. Increasing the airgap too much is not desirable regardless of converging inductance size since it will generate strong field near the windings resulting in excessive gap losses and inducing eddy fields in the windings [51]. Due to x-axis symmetry, effective inductance of

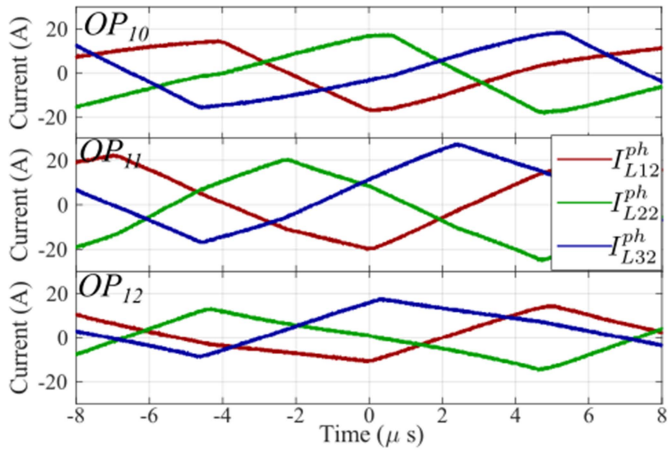

Fig. 26. Experimental DC-side inductor current ripples of the IIM at three different operating points along the LF cycle. $OP_{10}(T_s = 14\,\mu\text{s}, D_{2x} = 0.285, V_m^{ph} = 300\ \text{V}, I_{\text{Load}} = 5\ \text{A})$, $OP_{11}(\ T_s = 14\ \mu\text{s},\ D_{2x} = 0.5, V_m^{ph} = 350\ \text{V},\ I_{\text{Load}} = 5\ \text{A})$, $OP_{12}(\ T_s = 14\ \mu\text{s}, D_{2x} = 0.642, V_m^{ph} = 125\ \text{V},\ I_{\text{Load}} = 5\ \text{A})$.

W_{1x} and W_{3x} is the same, however W_{2x} is in the middle and sees a different higher equivalent Thevenin reluctance according to Fig. 21(a) [earlier quantified in (25) and (26)]. This introduces a higher degree of inductance variability across interleaved submodules when n is odd.

The horizontal airgaps affect the flux sharing ratio between the submodule or k_x, when treated in Section II-C, the best design is $(-0.1 < k_x < 0.1)$. The immediate magnetic loops to the left and right of all MMF generating sources need to contain equal amount of airgap so that all the windings have equal inductances. In doing so, and to protect the side C-sections from overheating, all the side air gaps are considered twice as long as the ones in between, $g_{x1} = 2g_{x2}$. With this adjustment the variation of inductance and dc-flux density in all the winding limbs are shown with respect to horizontal air gap length in Fig. 21(b). The sensitivity of the inductance, e.g., $S_{1x}^{2x} = \frac{L_{1x,e} - L_{2x,e}}{L_{1x,e}}$ is plotted in Fig. 21(c) to evaluate the optimum region for the ratio of g_{x1} and g_{x2} in maintaining equal inductances for all submodules.

To verify the desired effect of these dimension, a physical model of IIM is reconstructed using MAXWELL. The model of the IIM with three interleaved submodules is shown in Fig. 22(a). In this figure, the air gaps are, $g_{x1} = 2$ mm, $g_{x2} = 1$ mm, $g_{y1} = 0.5$ mm, and $g_{y2} = 1.5$ mm. The simulation is done for one switching cycle with interleaved current imported to ANSYS from the analytical model described in Section III-A.

Four LF operating points on the ZVS-DMCR is selected to evaluate the effect of magnetic fields distribution in the magnetic device. These operating points are OP_6 : $\{\ T_s = 20\ \mu\text{s}, D_{2x} = 0.25, V_m^{ph} = 151\ \text{V}, R_L = 4.167\ \Omega\}$, OP_7 : $\{\ T_s = 20\ \mu\text{s}, D_{2x} = 0.35, V_m^{ph} = 249\ \text{V}, R_L = 4.167\ \Omega\}$, OP_8 : $\{\ T_s = 20\ \mu\text{s}, D_{2x} = 0.45, V_m^{ph} = 377\ \text{V}, R_L{=}4.167\Omega\}$, OP_9 : $\{\ T_s = 20\ \mu\text{s}, D_{2x} = 0.55, V_m^{ph} = 563\ \text{V}, R_L{=}4.167\ \Omega\}$ to emulate the ZVS-DMCR LF operating points at rated power presented in Fig. 2. The magnetic flux density distribution for these operation points is captured at T_{12} (Maximum current

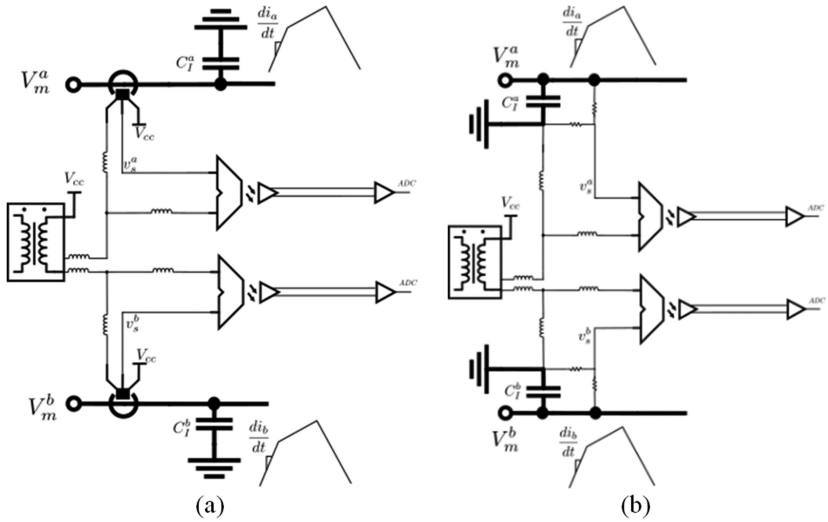

Fig. 27. Sensing scheme and grounding for minimum noise on the feedback signal to DSP. (a) Current sensors. (b) Voltage sensors.

TABLE V
EXPERIMENTAL INDUCTANCE AND SENSITIVITY OF THE 3X INTERLEAVED IIM IN THREE OPERATING POINTS

	OP_{10}	OP_{11}	OP_{12}
$L_{12,e}$	36.14 µH	56.19 µH	41.97 µH
$L_{22,e}$	32.25 µH	52.80 µH	39.06 µH
$L_{32,e}$	33.70 µH	54.20 µH	41.36 µH
S_{12}^{22}	10.75 %	06.03 %	06.94 %
S_{12}^{32}	06.74 %	03.53 %	01.47 %
S_{22}^{32}	04.30 %	02.58 %	05.55 %

Note: $OP_{10}(T_s = 14\ \mu s,\ D_{2x} = 0.285,\ V_m^{ph} = 300\ V,\ I_{Load} = 5\ A)$, $OP_{11}(T_s = 14\ \mu s,\ D_{2x} = 0.5,\ V_m^{ph} = 350\ V,\ I_{Load} = 5\ A)$, $OP_{12}(T_s = 14\ \mu s, D_{2x} = 0.642, V_m^{ph} = 125\ V,\ I_{Load} = 5\ A)$.

for the submodule of interest) is shown in Fig. 23(a)–(d) for OP_6–OP_9, respectively. The core-loss and inductance variation of the IIM under variety of bias condition of ZVS-DMCR is shown in Fig. 24 derived from MAXWELL.

To investigate the effect of the duty cycle variation with the DMS on the effective inductance, ac-and dc-side per unit effective inductance during switching transition is shown in Fig. 25(a) and (b) for 2x- and 3x- interleaved submodules along the line cycle. The effective inductance when only two submodules are excited is higher relative to three, due to symmetry in even number of fluxes as opposed to odd number. Also, the amount of overlap between interleaved submodules are significantly lower in 2x compared to 3x that results in reduced effective inductance as presented in Fig. 9.

IV. EXPERIMENTAL VERIFICATION

The experimental setup for the ZVS-DMCR is designed for the three module and 3x submodules (total nine submodules) with specifications presented in Table I. In this section, unique hardware design challenges relevant to the proposed system is explored along with mitigation methods. Experimental results of 3x and 2x submodules in rectifier operation is presented in a variety of operation points.

A. Experimental Fabrication and Testing of IIM

The IIM is fabricated in LESES as shown in Fig. 22(b). The experimental measurements of the coupling matrix using 4192A LF Impedance Analyzer is shown as follows for 6 (3x) and 4 (2x) interleaved submodules

$$\overline{K_{3x}} = \begin{bmatrix} 1 & 0.212 & -0.023 & 0.821 & 0.205 & -0.022 \\ 0.212 & 1 & 0.206 & 0.199 & 0.670 & 0.195 \\ -0.023 & 0.206 & 1 & -0.023 & 0.198 & 0.808 \\ 0.821 & 0.199 & -0.023 & 1 & 0.210 & -0.021 \\ 0.205 & 0.807 & 0.198 & 0.210 & 1 & 0.203 \\ -0.022 & 0.195 & 0.808 & -0.021 & 0.203 & 1 \end{bmatrix} \tag{27}$$

$$\overline{K_{2x}} = \begin{bmatrix} 1 & -0.023 & 0.821 & -0.022 \\ -0.023 & 1 & -0.023 & 0.808 \\ 0.821 & -0.023 & 1 & -0.021 \\ -0.022 & 0.808 & -0.021 & 1 \end{bmatrix}. \tag{28}$$

The coupling matrix in both cases shows very small k_x (-0.02 ± 0.002) as designed in Section II-C between inductors of the submodule 1 and 3 in both (27) and (28). In 2x-interleaving the windings of second submodule is disconnected, while in 3x-interleaving k_x between submodule 2-3 and 2-1 is not as low as 1-3 (0.2 ± -0.02). This is due to the tradeoff made in Section III-C to attain ratio of $\left(\frac{g_{x1}}{g_{x2}} = 2\right)$. The ratio is selected on the lower end of the desired range of Fig. 21(c) to reduce the size of the airgap in an attempt to avoid creating a strong field region near the gaps. In doing so, the IIM has $\pm 5\%$ flux sharing asymmetry between submodule 2 and submodules 1 and 3.

The IIM with 3x submodules is tested experimentally to study the effect of the second submodule k_x inequality on the inductor current ripple as presented in Fig. 26. In this figure, the dc-side inductor currents are ac coupled (average is removed) and the operation points are $OP_{10}(T_s = 14\ \mu s,\ D_{2x} = 0.285,\ V_m^{ph} = 300\ V,\ I_{Load} = 5\ A)$, $OP_{11}(T_s = 14\ \mu s,\ D_{2x} = 0.5, V_m^{ph} = 350\ V,\ I_{Load} = 5\ A)$,

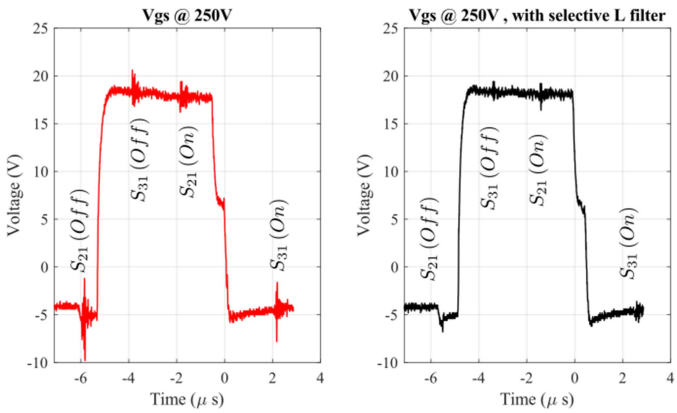

Fig. 28. Mitigation of the PWM signal interference between interleaved submodules by selective filtering.

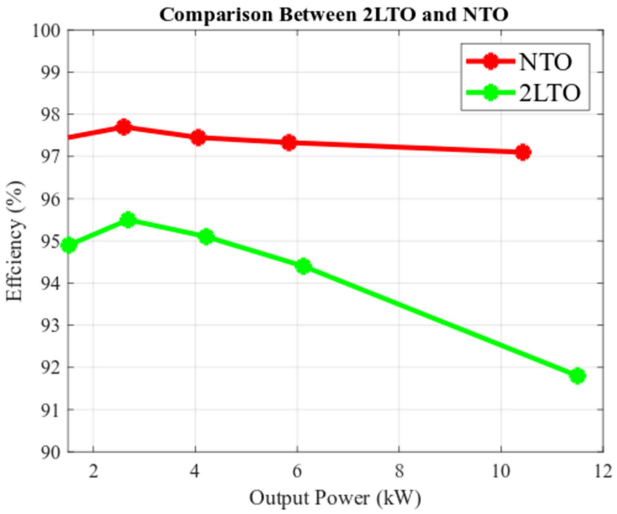

Fig. 29. Experimental efficiency comparison between NTO (no turn-OFF level) and 2LTO (two level turn OFF).

$OP_{12}(T_s = 14\ \mu\text{s}, D_{2x} = 0.642, V_m^{ph} = 125\ \text{V},\ I_{\text{Load}} = 5\ \text{A})$. These operation points are selected to study the dynamic current sharing (current ripple) symmetry of the interleaved submodules with fixed load current (current controlled with battery emulator) while input voltage/duty cycle is varied. The experimental effective inductances for all inductors with all three cases and their corresponding sensitivity as defined in Section III-C is shown in Table V.

B. Hardware Implementation

The design of the experimental setup for the ZVS-DMCR operating in TCM presents several challenges compared to noninterleaved CCM-DMCR. The magnetics are the prominent recipients of the elevated current ripple in the TCM that was treated extensively earlier.

Second is the power stage board layout and power module to realize 3x submodules in the same size as a single half bridge. The six pack MOSFET module (MSCSM170TAM15CTPAG) that

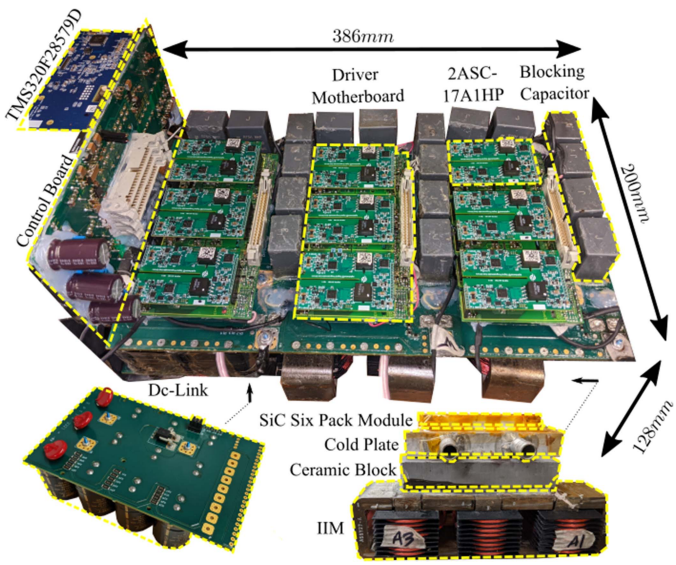

Fig. 30. Experimental setup of the ZVS-DMCR with design specifications presented in Table I.

is commercially available is used that has the same footprint as the standard half bridge (62 mm) SiC MOSFET modules. A multilayer high copper weight PCB is used to alleviate the implementation of the multimodule setup.

The third is driving high voltage power SiC MOSFETS in a small footprint. A gate driver motherboard is designed to customize the layout and gate current delivery to the device's gate.

Finally, the elevated noise level through high d*i*/d*t* created through TCM creates differential noise through parasitic inductances in the circuit. This noise interferes with the sensor feedback signals as well as the pulsewidth modulation (PWM) [52]. Isolated grounding scheme is used with dedicated return path for each signal to reduce these interference as shown in Fig. 27(a) and (b) for current and voltage feedback, respectively. Fig. 27 shows differential operation of modules A and B where both are high-frequency switching (M_0 in Fig. 2). Magnetically isolated power supply is used to supply V_{cc} to the sensors to avoid noise current interference of the power stage. The feedback signal is optically isolated and traced back differentially to the DSP (TMS320F28379D) to avoid capacitive noise coupling of the feedback signal with power board switching. Multiple differential mode and common mode filters are placed in the analog signal chain to eliminate extra noises picked up by imbalance (DM) and parasitic capacitances.

The PWM signal is similarly filtered, and several features of the gate driver is used to avoid false turn ON and noisy V_{gs}. Fig. 28 shows the elimination of the crosstalk interference between interleaved drivers in a submodule by selective conductive EMI filtering through *L* and *C* links. As it is shown in this experiment, two-level turn OFF (2LTO) from the 2ASC-17A1HP [53] gate driver is used to reduce the conducted noise, however, this slows down the device significantly which results in elevated turn-OFF losses. An efficiency comparison with (2LTO) and without (NTO) using this method is shown in Fig. 29. In practice,

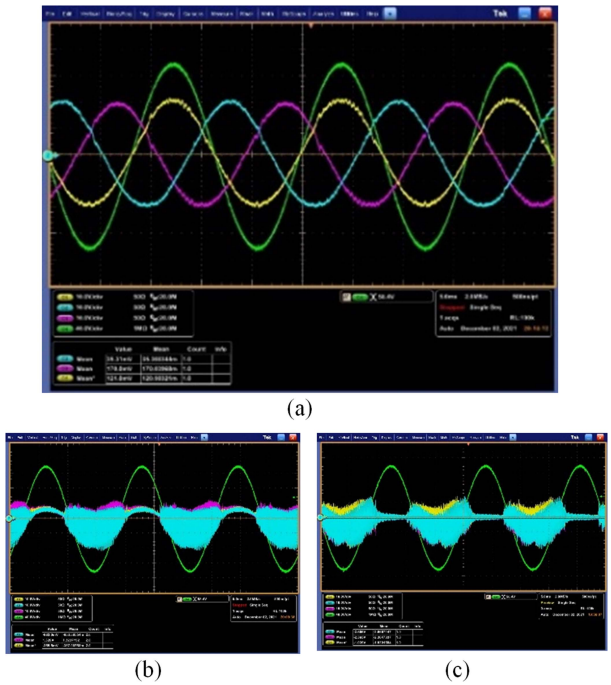

Fig. 31. Experimental results for ZVS-DMCR with 3x interleaved submodules at $OP_{13}:\{T_s=10\ \mu s,\ G_x=0.68, V_m^{ph}=175$ Vrms, $R_L=9.65\ \Omega\}$. (a) Phase A current (Yellow, 10 $\frac{\text{A}}{\text{div}}$), phase B current (Blue, 10 $\frac{\text{A}}{\text{div}}$), phase C current (purple, 10 $\frac{\text{A}}{\text{div}}$), and phase a line to neutral voltage (Green, 10 $\frac{\text{V}}{\text{div}}$). (b) AC-side inductor currents, I_{L11}^A (Yellow, 10 $\frac{\text{A}}{\text{div}}$), I_{L21}^A (Blue, 10 $\frac{\text{A}}{\text{div}}$), I_{L31}^A (Purple, 10 $\frac{\text{A}}{\text{div}}$), phase A line to neutral voltage (Green, 40 $\frac{\text{V}}{\text{div}}$). (c) DC-side inductor currents, I_{L12}^A (Yellow, 10 $\frac{\text{A}}{\text{div}}$), I_{L22}^A (Blue, 10 $\frac{\text{A}}{\text{div}}$), I_{L32}^A (Purple, 10 $\frac{\text{A}}{\text{div}}$), phase A line to neutral voltage (Green, 40 $\frac{\text{V}}{\text{div}}$).

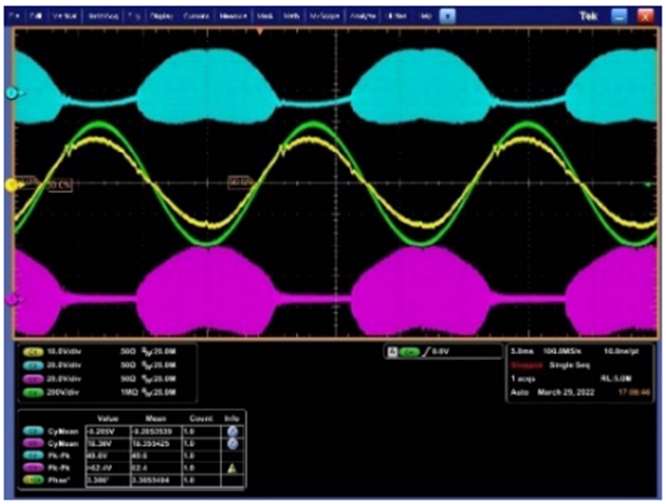

Fig. 32. Experimental results for ZVS-DMCR with 3x interleaved submodules at $OP_{15}:\{T_s=14\ \mu s,\ G_x=0.68,\ V_m^{ph}=480$ V, $R_L=12\ \Omega\}$. Phase A currents, (Yellow, 10 $\frac{\text{A}}{\text{div}}$), I_{L11}^A (Blue, 20 $\frac{\text{A}}{\text{div}}$), I_{L12}^A (Purple, 20 $\frac{\text{A}}{\text{div}}$), phase A line to neutral voltage (Green, 200 $\frac{\text{V}}{\text{div}}$).

a tradeoff between the turn-OFF speed and the efficiency must be made. Alternatively, the tradeoff favoring noise reduction can be done against power density instead of efficiency. The latter was shown in Fig. 29 where former can be realized adding turn-OFF snubbers to store the energy and slow down the switching transitions. There are a lot of literature on this subject [1], [2],

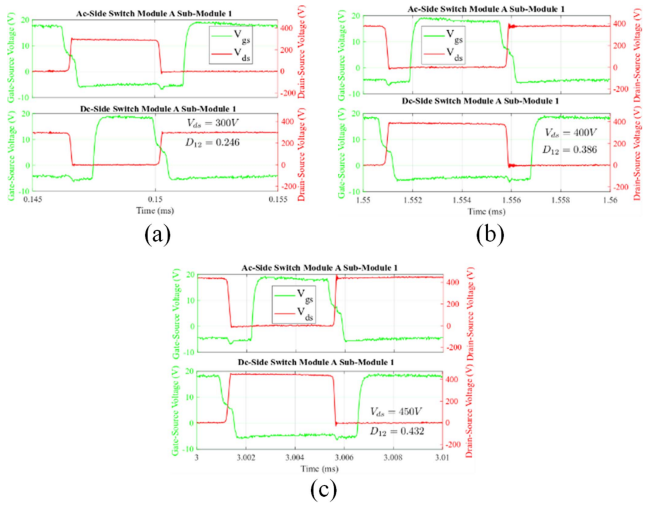

Fig. 33. Demonstration of the ZVS in the 3x interleaved submodules in rectifier operation at $OP_{14}:\{\ T_s=10\ \mu s,\ G_x=0.68,\ V_m^{ph}=175\ \text{V},\ R_L=9.65\ \Omega\}$. Three instances along the line cycle are captured and zoomed in the switching cycle. The ac-and dc-side V_{gs} and V_{ds} are shown for submodule 1 of phase. (a) $V_{ds}=300\ \text{V}, D_{x2}=0.246$. (b) $V_{ds}=400\ \text{V}, D_{x2}=0.386$. (c) $V_{ds}=450\ \text{V}, D_{x2}=0.432$.

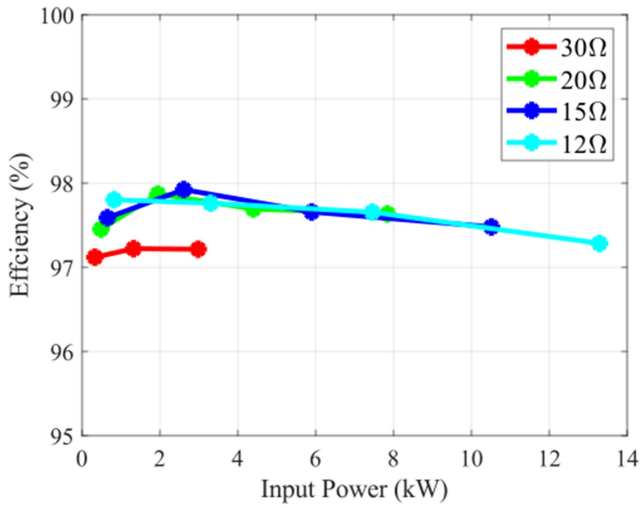

Fig. 34. Efficiency of the 2x interleaved submodules with power level. Four level loads are shown.

[8], [9], [10], [11], [13] and so no further discussion is dedicated to this tradeoff since it is beyond the scope of this article.

C. Converter Experimental Results

The experimental setup for the ZVS-DMCR system containing control board, IIM, gate driver motherboard as well as power stage is shown in Fig. 30 with specifications mentioned in Table I. In the following the IIM is evaluated experimentally followed by the treatment of the ZVS-DMCR in single module mode as well as rectifier mode.

Using TCM, the ZVS-DMCR is tested for 3x submodules per module at $OP_{13}:\{T_s=10\ \ \mu s, G_x=0.68, V_m^{ph}=175\ \text{V}, R_L=9.65\ \Omega\}$. Fig. 31(a) shows three phase current and phase A voltage, Fig. 31(b) shows the ac-side inductors current, and Fig. 31(c) shows the dc-side

inductor currents. Peak current control using PR compensators is used to control the input current with DMS. Similarly, for the 2x submodules, ac-and dc-side inductors along with one phase current and its voltage is presented in Fig. 32 at OP_{14} : $\{ T_s = 14\ \mu\text{s},\ G_x = 0.68, V_m^{ph} = 480\ \text{Vrms}, R_L = 12\ \Omega\}$.

The experimental demonstration of C_{oss} discharge is shown corresponding to OP_{15} : $\{ T_s = 10\ \mu\text{s},\ G_x = 0.68, V_m^{ph} = 175\ \text{Vrms}, R_L = 9.65\ \Omega\}$ in Fig. 33(a)–(c). The V_{ds} (drain–source blocking voltage) is dropped to zero before V_{gs} (gate-source voltage) switches high. The efficiency of a ZVS-DMCR module with 2x submodules is shown in Fig. 34 up to rated power per submodule.

V. Conclusion

In this work, by utilizing TCM and IIM, a ZVS-DMCR system is proposed to improve the efficiency and power density simultaneously. Interleaved submodules are used to reduce the current ripples on the ac-and dc-side capacitors and divide the rated inductor and switch currents on both sides by the number of submodules. By eliminating the turn-ON losses of the ac-side switch, the main loss component is removed/reduced and the efficiency is improved across load. It is shown that the increased number of components have not impacted the power density negatively compared to noninterleaved CCM-DMCR. This fit is achieved by addressing the magnetics through proposing an IIM, combing all the magnetic components of a module ($2n$) into a single device. By analyzing the IIM in detail, couplings are tuned through geometrical dimensions of the custom nanocrystalline core and airgaps in a proposed scalable structure, so that the flux cancellation between ac-and dc-side inductor is exploited to improve efficiency and power density. This is when the inner coupling across the submodule is minimized to avoid its adverse effect. The analysis is verified by circuit and finite-element simulations. Finally, parametric, and temporal results from the experimental setup are presented to verify the performance of ZVS-DMCR. Experimental results are presented for 2x and/or 3x submodules in rectifier and single module operation.

Acknowledgment

The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

References

[1] T. Friedli, M. Hartmann, and J. W. Kolar, "The essence of three-phase PFC rectifier systems–Part II," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 543–560, Feb. 2014.

[2] J. W. Kolar and T. Friedli, "The essence of three-phase PFC rectifier systems Part I," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 176–198, Jan. 2013.

[3] M. Safayatullah, M. T. Elrais, S. Ghosh, R. Rezaii, and I. Batarseh, "A comprehensive review of power converter topologies and control methods for electric vehicle fast charging applications," *IEEE Access*, vol. 10, pp. 40753–40793, 2022.

[4] H. Tu, H. Feng, S. Srdic, and S. Lukic, "Extreme fast charging of electric vehicles: A technology overview," *IEEE Trans. Transp. Electrific.*, vol. 5, no. 4, pp. 861–878, Dec. 2019.

[5] M. A. H. Rafi and J. Bauman, "A comprehensive review of DC fast-charging stations with energy storage: Architectures, power converters, and analysis," *IEEE Trans. Transp. Electrific.*, vol. 7, no. 2, pp. 345–368, Jun. 2021.

[6] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2151–2169, May 2013.

[7] Rohm Semiconductor, Kyoto, Japan, SiC Power Devices and Modules, Application Note Rev.003," 2020.

[8] J. Lu et al., "A modular-designed three-phase high-efficiency high-power-density EV battery charger using dual/triple-phase-shift control," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 8091–8100, Sep. 2018.

[9] Z. Wu, Z. Wang, Y. Zhang, W. Xu, C. Chen, and Y. Kang, "A high efficiency and high power density DC transformer topology with output regulation capability," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8232–8247, Jul. 2022.

[10] B. Li, Q. Li, and F. C. Lee, "High-frequency PCB winding transformer with integrated inductors for a bi-directional resonant converter," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6123–6135, Jul. 2019.

[11] B. Whitaker et al., "A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2606–2617, May 2014.

[12] H. Akagi, T. Yamagishi, N. M. L. Tan, Y. Miyazaki, S. I. Kinouchi, and M. Koyama, "Power-loss breakdown of a 750-V 100-kW 20-kHz bidirectional isolated DC-DC converter using SiC-MOSFET/SBD dual modules," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 420–428, Jan./Feb. 2015.

[13] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Muhlethaler, T. Nussbaumer, and J. Minibock, "Extreme efficiency power electronics," in *Proc. 7th Int. Conf. Integr. Power Electron. Syst.*, Nuremberg, Germany, 2012, pp. 1–22.

[14] "STMicroelectronics, AN2644 Application note, An introduction to LLC resonant half-bridge converter," 2008.

[15] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Trans. Power Electron.*, vol. 3, no. 2, pp. 174–182, Apr. 1988.

[16] Y. Gu, Z. Lu, L. Hang, Z. Qian, and G. Huang, "Three-level LLC series resonant DC/DC converter," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 781–789, Jul. 2005.

[17] S. Inoue and H. Akagi, "A bidirectional DC-DC converter for an energy storage system with galvanic isolation," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2299–2306, Nov. 2007.

[18] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Jan./Feb. 1991.

[19] S. Gupta and S. K. Mazumder, "A novel modulation scheme for isolated PWM active-clamp Cuk DC/DC converter," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14966–14980, Dec. 2022.

[20] B. R. Lin and C. L. Huang, "Zero voltage switching active clamp buck-boost stage Cuk converter," *IET Elect. Power Appl.*, vol. 1, no. 2, pp. 173–182, 2007, doi: 10.1049/iet-epa:20060157.

[21] D. Maksimovic and S. Cuk, "A unified analysis of PWM converters in discontinuous modes," *IEEE Trans. Power Electron.*, vol. 6, no. 3, pp. 476–490, Jul. 1991.

[22] S. Ćuk, "Discontinuous inductor current mode in the optimum topology switching converter," in *Proc. IEEE Power Electron. Spec. Conf.*, 1978, pp. 105–123. doi: 10.1109/PESC.1978.7072344.

[23] D. S. L. Simonetti, J. Sebastion, and J. Uceda, "The discontinuous conduction mode Sepic and Cuk power factor preregulators: Analysis and design," *IEEE Trans. Ind. Electron.*, vol. 44, no. 5, pp. 630–637, Oct. 1997.

[24] P. Barbosa, F. Canales, J.-C. Crebier, and F. C. Lee, "Interleaved three-phase boost rectifiers operated in the discontinuous conduction mode: Analysis, design considerations and experimentation," *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 724–734, Sep. 2001.

[25] M. M. Jovanović and Y. Jang, "State-of-the-art, single-phase, active power-factor-correction techniques for high-power applications - An overview," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3. pp. 701–708, Jun. 2005.

[26] Z. Huang, Z. Liu, F. C. Lee, and Q. Li, "Critical-mode-based soft-switching modulation for high-frequency three-phase bidirectional AC-DC converters," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3888–3898, Apr. 2019.

[27] L. Huber, B. T. Irving, and M. M. Jovanović, "Effect of valley switching and switching-frequency limitation on line-current distortions of DCM/CCM boundary boost PFC converters," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 339–347, Feb. 2009.
[28] Q. Huang, R. Yu, Q. Ma, and A. Q. Huang, "Predictive ZVS control with improved ZVS time margin and limited variable frequency range for a 99% efficient, 130-W/in 3 MHz GaN totem-pole PFC rectifier," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 7079–7091, Jul. 2019.
[29] B. Cougo, H. Schneider, and T. Meynard, "High current ripple for power density and efficiency improvement in wide bandgap transistor-based buck converters," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4489–4504, Aug. 2015.
[30] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, Feb. 2014.
[31] M. Mohamadi, N. Kumar, S. K. Mazumder, and A. Gupta, "High power design challenges for differential-mode EV universal battery supercharger," *IEEE Trans. Ind. Appl.*, vol. 58, no. 5, pp. 5568–5581, Sep./Oct. 2022.
[32] B. C. Barry, J. G. Hayes, and M. S. Rylko, "CCM and DCM operation of the interleaved two-phase boost converter with discrete and coupled inductors," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6551–6567, Dec. 2015.
[33] D. Zhang, F. Wang, R. Burgos, R. Lai, and D. Boroyevich, "Impact of interleaving on AC passive components of paralleled three-phase voltage-source converters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1042–1054, May/Jun. 2010.
[34] R. Mayer, M. B. E. Kattel, and S. V. G. Oliveira, "Multiphase interleaved bidirectional DC/DC converter with coupled inductor for electrified-vehicle applications," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2533–2547, Mar. 2021.
[35] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "An integrated inductor for parallel interleaved three-phase voltage source converters," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3400–3414, May 2016.
[36] F. Forest, T. A. Meynard, J.-J. Huselstein, D. Flumian, C. Rizet, and A. Lacarnoy, "Design and characterization of an eight-phase-137-kW intercell transformer dedicated to multicell DC-DC stages in a modular UPS," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 45–55, Jan. 2014.
[37] P. Zumel, O. García, J. A. Cobos, and J. Uceda, "Magnetic integration for interleaved converters," in *Proc. 18th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2003, vol. 2, pp. 1143–1149, doi: 10.1109/apec.2003.1179360.
[38] E. Labouré, A. Cuniére, T. A. Meynard, F. Forest, and E. Sarraute, "A theoretical approach to InterCell transformers, application to interleaved converters," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 464–474, Jan. 2008.
[39] S. Lu, M. Mu, Y. Jiao, F. C. Lee, and Z. Zhao, "Coupled inductors in interleaved multiphase three-level DC-DC converter for high-power applications," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 120–134, Jan. 2016.
[40] R. Bosshard and J. W. Kolar, "All-SiC 9.5 kW/dm 3 on-board power electronics for 50 kW/85 kHz automotive IPT system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 419–431, Mar. 2017.
[41] S. Ohn et al., "A scalable filter topology for n-parallel modular three-phase AC-DC converters by an arrangement of coupled inductors," *IEEE Trans. Power Electron.*, vol. 37, no. 11, pp. 13358–13367, Nov. 2022.
[42] C. Shi, A. Khaligh, and H. Wang, "Interleaved SEPIC power factor preregulator using coupled inductors in discontinuous conduction mode with wide output voltage," *IEEE Trans. Ind. Appl.*, vol. 52, no. 4, pp. 3461–3471, Jul./Aug. 2016.
[43] Microchip Technology Inc, Chandler, AZ, USA, "Triple phase leg SiC MOSFET power module product overview," MSCSM170TAM15CTPAG, 2021.
[44] M. Mohamadi, S. K. Mazumder, and N. Kumar, "Integrated magnetics design for a three-phase differential-mode rectifier," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10561–10570, Sep. 2021.
[45] L. Huber, B. T. Irving, and M. M. Jovanović, "Open-loop control methods for interleaved DCM/CCM boundary boost PFC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1649–1657, Jul. 2008.
[46] H. Soni, S. K. Mazumder, A. Gupta, D. Chatterjee, and A. Kulkarni, "Control of isolated differential-mode single- and three-phase Ćuk inverters at module level," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8872–8886, Oct. 2018.
[47] S. Mehrnami, S. K. Mazumder, and H. Soni, "Modulation scheme for three-phase differential-mode Ćuk inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2654–2668, Mar. 2016.
[48] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.
[49] Y. Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical loss model of power MOSFET," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 310–319, Mar. 2006.
[50] D. Christen and J. Biela, "Analytical switching loss modeling based on datasheet parameters for MOSFETS in a half-bridge," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3700–3710, Apr. 2019.
[51] C. R. Sullivan and R. Y. Zhang, "Simplified design method for Litz wire," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 2667–2674, doi: 10.1109/APEC.2014.6803681.
[52] E. B. Joffe and K.-S. Lock, *Grounds for Grounding : A Circuit-to-System Handbook*. Piscataway, NJ, USA: IEEE Press, 2010.
[53] S. P. Features and K. D. Features, "Augmented high performance SiC core 1," pp. 1–19, 2019.

Moien Mohamadi (Student Member, IEEE) received the M.Sc. degree in electrical engineering from Isfahan University of Technology, Isfahan, Iran, in 2017. He is currently working toward the Ph.D. degree, with his dissertation title as High frequency magnetics and soft-switching for differential-mode electric vehicles superchargers with the Laboratory for Energy and Switching-Electronics Systems, University of Illinois at Chicago, Chicago, IL, USA.

He has been working in power electronics research and development since 2014. He is currently involved in the research on highly efficient and compact fast battery charger. His research interests include optimal design and hardware realization of highly efficient and compact power electronics converter, high-frequency magnetic design, optimization, and hardware realization, and soft-switching power electronics.

Mr. Mohamadi has been a member of PES community since 2014.

Sudip K. Mazumder (Fellow, IEEE) received the Ph.D. degree in electrical and computer engineering from Virginia Tech, Blacksburg, VA, USA, in 2001.

He has been the President of NextWatt LLC, Kanhangad, India, since 2008 and a Professor with UIC, Chicago, IL, USA, since 2001. He has more than 30 years of professional experience and has held research and development and design positions in leading industrial organizations and has served as a technical consultant for several industries. He has also made original contributions to the areas of control of power-electronic systems at the semiconductor device level for numerous and wide-ranging applications in commercial and defense space; high-frequency-link power electronics, including hybrid-modulation-based pulsating-dc-link inverter and differential-mode-converter (ac/ac, dc/ac, ac/dc) topologies for applications encompassing but not limited to renewable and alternative energy, electric vehicles, solid-state transformer, energy storage, and offshore wind; discretized high-frequency and Boolean energy and data transfer; and optically-controlled power semiconductor devices [including optical emitter turn-off thyristor, heterojunction devices, high-gain bipolar devices, and hybrid and monolithic photoconductive semiconductor switches (PCSS)] and power electronics.

Dr. Mazumder was named a Fellow of the American Association for the Advancement of Science (AAAS), in 2020, and a Fellow of the Asia-Pacific Artificial Intelligence Association (AAIA) in 2022. He serves as the Editor in Large for the IEEE TRANSACTIONS ON POWER ELECTRONICS since 2019 and served as an IEEE Distinguished Lecturer between 2016 and2019. He has been serving as an Administrative Committee Member for IEEE PELS, since 2015. He has also been serving as a Member-at-Large for IEEE PELS, since 2020. He has served as the Chair for the IEEE PELS Technical Committee on Sustainable Energy Systems, from 2015 to 2020. He serves as the General Chair for IEEE PEDG Conference in 2023. At UIC, he was a recipient of the Distinguished Researcher Award in Natural Sciences and Engineering, in 2020, the Inventor of the Year Award, in 2014, and the University Scholar Award, in 2013. He was also the recipient of several IEEE Awards, including the Prize Paper Award from the TPEL and the IEEE International Future Energy Challenge Award, the U.S. Office of Naval Research (ONR) Young Investigator Award, and the U.S. National Science Foundation (NSF) CAREER Award.