Overview of Wide/Ultrawide Bandgap Power Semiconductor Devices for Distributed Energy Resources

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***Abstract*— This article provides an overview of power semiconductor devices (PSDs) for the distributed energy resource (DER) system. To begin with, an overview of electrically triggered SiC and gallium nitride (GaN) devices followed by a brief narration of ultrawide bandgap (UWBG) PSDs and, subsequently, an overview of optically activated PSDs encompassing photoconductive semiconductor switch (PCSS) and optical bipolar PSDs are provided. Finally, an overview of PSD packaging and reliability is captured.**

***Index Terms*— Devices, electrical, materials, optical, packaging, reliability, ultrawide bandgap (UWBG), wide bandgap (WBG).**

I. Introduction

A DISTRIBUTED energy resource (DER) is any resource in the distribution system that produces electricity and is not otherwise included in the formal North American Electric Reliability Corporation (NERC) definition of the bulk electric system (BES) [1]. DERs include any non-BES resource located solely within the boundary of any distribution utility and distribution provider, including the following: distributed generation, behind-the-meter generation, energy storage facility, DER aggregation, microgrid, virtual power plant, cogeneration, and emergency/standby/back-up generation [1]. The power and voltage ranges for the DERs vary considerably ranging from below 1 to below 69 kV and a few kilowatts to several megawatts. As such, the power semiconductor devices (PSDs) that serve as the actuators for the DER power electronics need to encompass a wide range of voltage and power levels. Conventional silicon (Si) power devices have dominated DER power electronics due to their low cost, excellent starting material quality, ease of processing, good performance with low loss, and proven reliability. Recently, PSDs based on wide bandgap (WBG) semiconductors [e.g., SiC and gallium nitride (GaN)] and ultrawide bandgap (UWBG) semiconductors (e.g., Ga_2O_3, diamond, and nitrides), as outlined in Sections II and III, are also emerging that evince potential for efficient PSDs for medium- and high-voltage DERs.

The main advantages of WBG and UWBG devices are the increase in blocking voltage and the enabling of high-frequency switching, which they are capable of relative to traditional Si devices. High-voltage blocking directly enables higher voltage operation of the power conversion system and could enable simple topologies to be utilized for MV applications that now require either modular, multilevel converters or single-stage converters with serially connected switches. This simpler topology would enable cost reduction in MV power conversion and increased reliability due to a lower component count. In addition, the use of WBG and UWBG devices enables the operation of the system at higher switching speeds. This has a twofold benefit. The first is a reduced requirement for passive energy storage components. This reduces the size, weight, and cost of the power converter with applications, including, but not limited to, solid-state transformer, integration wind-cycloconverter system, and high-frequency-link power conversion. This can introduce significant benefits in the balance of system cost due to savings in shipping the unit and the installation, especially if this can be done without the use of a crane or other machinery. The higher switching frequency also enables higher control bandwidth in the system, which can enable new forms of system-level control. Since the

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transient response of the power electronic system is determined via controls and not physics (as in a traditional rotating machine), new modes of operation are enabled through nearly arbitrary subtransient response. This can have outsized benefits to system contingency by, for example, allowing the DER to replicate the inertia of a rotating mass in a contingency event.

Furthermore, while the traditional approach to the realization of such PSDs for DERs has been based dominantly on electrical triggering, new research has begun to show the potential of optical triggering in PSDs. This is captured in Section IV, including the benefits of low latency, rapid switching, immunity to electromagnetic interference (EMI) noise, and uniformity of device triggering for high-voltage scaling without incurring complexities of floating gate drivers. In addition, other emerging applications leveraging the ultrafast performance of optical PSDs, such as GaN photoconductive semiconductor switch (PCSS) operating in the nonlinear mode, are being investigated for rapid fault isolation.

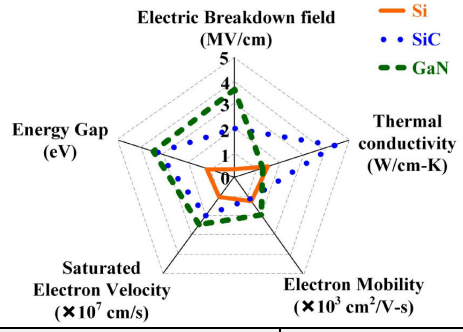
Yet another issue pertains to packaging, as detailed in Section V. WBG semiconductors (SiC and GaN) due to their enhanced performance and superior material properties compared to traditional Si power devices have become the ultimate choice for future high-performance energy conversion. Since traditional device packaging becomes a limiting factor in fully harnessing the benefits offered by the advanced PSDs, improved and advanced packaging structures are necessary to bridge the gap between WBG devices and their applications [2], [3], [4], [5], [6].

A final issue, as outlined in Section VI, relates to the reliability of the PSDs. Methodologies to ensure reliable WBG products were proposed and reported in the literature [7] and discussed in WBG and reliability conferences and workshops. For GaN-based power devices, time-dependent-dielectric-like breakdown, dynamic ON-state resistance due to trapping effects, and hard switching are among the key topics that are currently in focus by the research and development community. A significant knowledge base has been accumulated since 2005. For SiC-based power devices, power cycling, humidity robustness, bipolar degradation, gate oxide reliability, and bias temperature instabilities are among the hot topics. Test and screening procedures need to be adapted and extended to account for different material properties, higher fields, crystal defects, and a more complex MOS system.

II. WBG Power Semiconductor Devices

A. SiC Devices

WBG PSDs are currently in production for high-power/-temperature applications. SiC is ideally suited for power switching due to its high saturated drift velocity, its large bandgap, its excellent thermal conductivity, and its high critical field strength. For power devices, the tenfold increase in critical field strength of SiC relative to Si allows high-voltage blocking layers to be fabricated significantly thinner than those of comparable Si devices. This reduces device ON-state resistance, and the associated conduction and switching losses while maintaining the same high-voltage blocking capability. Lower switching losses allow for high-frequency operation,



Properties	Materials		
	Si	SiC (4H)	GaN
Electric breakdown field (MV cm^{-1})	0.3	2.2	3.3
Energy gap (eV)	1.12	3.26	3.39
Saturated electron velocity (x 10^7 cm s^{-1})	1	2	2.5
Electron mobility (x 10^3 cm^2 V^{-1} s^{-1}	1.4	0.95	0.8-1.7
Thermal conductivity (W cm^{-1} K^{-1})	1.5	4.5	4

Fig. 1. Graphical comparison of Si, SiC, and GaN material properties.

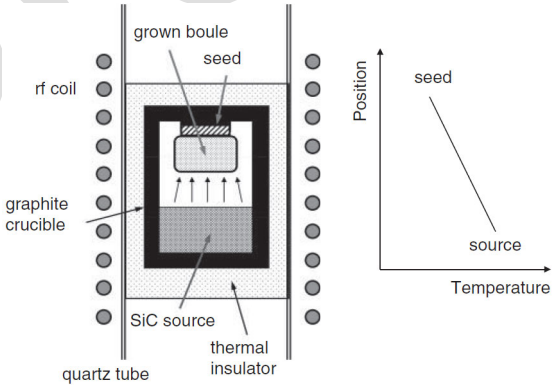


Fig. 2. Schematic description of crucible for seeded sublimation growth of SiC substrates.

which minimizes the size and weight of a system's passive components. The low specific ON-state resistance enables high-current operation at a relatively low forward voltage drop at a given breakdown voltage. Also, the WBG of SiC allows operation at high temperatures, where conventional Si devices fail, with low leakage and reduced cooling system requirements. A graphical summary of Si-, SiC-, and GaN-relevant material properties is shown in Fig. 1 [6].

To exploit SiC's compelling material properties in power devices, significant efforts started in the 1980 s to develop high-quality low defect SiC substrates and epitaxy. Today, 150-mm SiC wafers are primarily used in the production of SiC devices. 200-mm wafers were demonstrated in 2015 and are expected to become commercially available shortly. It should be noted that conventional SiC substrate growth is more complex than that of Si requiring the use of large seeds and high process temperatures. SiC is mainly grown by the seeded sublimation technique, as schematically shown in Fig. 2.

The raw material, SiC powder, is placed at the bottom of a graphite crucible. A seed wafer is placed at the top of the crucible, which is heated by RF coils to a temperature of ~2500 °C. The seed wafer is kept at a lower temperature than

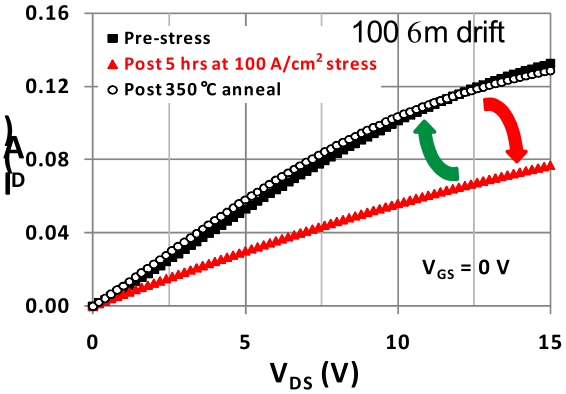


Fig. 3. BPD-related JFET ON-state degradation and recovery by annealing at 25 °C.

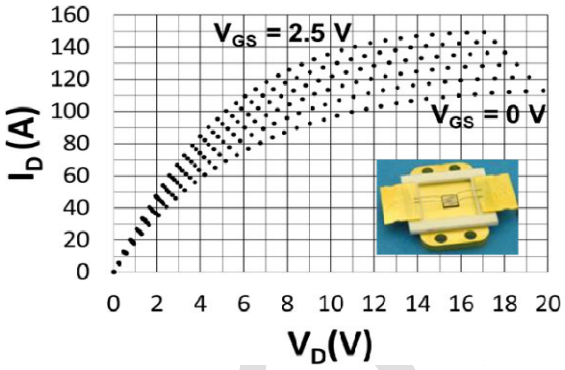


Fig. 4. ON-state drain current versus voltage characteristics of a single 1680-V, 0.143-cm^2 packaged JFET at a gate bias range of 0–2.5 V in steps of 0.5 V at a temperature of 25 °C.

the SiC powder, and the sublimed SiC species condensate and crystallize on the seed wafer. Reported sublimation growth rates are in the order of 0.5–2 mm/h. Increasing the growth rate can have the undesirable side effect of increased structural defect inclusion in the boule. SiC material's hardness, which is comparable to that of diamond, makes sawing and polishing SiC substrates slow and costly relative to Si. The epitaxial active SiC device layer is grown by chemical vapor deposition (CVD) in horizontal or planetary reactors at about 1550 °C. The epitaxial growth is done on 4° off-cut substrates to maintain the polytype stability of the substrate. SiC epitaxial growth is well established and strives to minimize defect propagation from the substrate to the epitaxial layer.

Historically, killer defects limiting yield have been polytype inclusions and micropipes. These have been practically eliminated in commercial wafers. Micropipe density, which is detrimental to device operation, is typically below 0.1 cm^{-2}. The remaining structural defects are threading screw dislocations (300–600 cm^{-2}) that can increase reverse voltage leakage, threading edge dislocations (2000–5000 cm^{-2}) that are considered benign, and basal plane dislocations (BPDs) (500–3000 cm^{-2}), which leads to device degradation under bipolar current flow. Although threading dislocations do result in measurable disturbances of epitaxial layer surface morphology, the practical effects of these disturbances on device performance and reliability are minimal [8]. BPDs are the major remaining "killer" defect impacting bipolar SiC devices and unipolar devices that conduct bipolar current during their operational cycle [9]. BPDs can be present in the starting SiC wafer and can also be generated during the high-temperature ion-implantation process. Interestingly, transistor BPD-related electrical characteristics degradations can be fully reversed by annealing at 350 °C, while nondegraded characteristics remain unaffected by the annealing (see Fig. 3) [10].

Numerous well-established processes from Si technology have been successfully transferred to SiC. However, SiC material properties necessitate the development of specific processes, whose parameters must be optimized and qualified. SiC is inert against chemical solvents, and only dry etching is practical. Conventional thermal diffusion is not realistic in doping SiC due to its high melting point and the low diffusion constant of dopants within SiC; heated ion implantation must be performed followed by a 1600 °C–1800 °C anneal for SiC recrystallization and implant activation. The high value of the SiC/metal barrier results in rectifying metal contacts. Post-metal deposition anneal is required for ohmic contact formation. Unlike Si wafers, those of SiC are transparent. This complicates critical dimension scanning electron microscope (CD-SEM) and metrology measurements as the focal plane is determined with the use of an optical microscope. SiC-specific metrology/inspection tools are now becoming available from multiple vendors. The relative lack of flatness of SiC wafers, compared to that of Si, can complicate photolithography and other processing particularly as high-temperature processes can further degrade wafer flatness rendering wafers unusable. Finally, the poor SiC/SiO_2 interface quality reduces inversion layer mobility, and passivation techniques are utilized to improve the SiC/SiO_2 interface quality. SiC process integration technology has made significant advancements, and optimizations are continuing. Today, SiC diodes and transistors are commercially available from multiple vendors.

To effectively compete with Si, large-area reliable and rugged SiC devices must be produced at a competitive cost. Early proof-of-concept work paved the way for investments that contributed to SiC commercialization. In 2008, a 1680-V SiC JFET with an active area of 0.143 cm^2 and an ON-state current capability of 50 A was the largest transistor reported to date (see Fig. 4) [11].

Specialized edge termination structures, such as multiple junction termination extensions and floating guard rings, were fabricated and maximized high-voltage performance [12]. Ruggedness and reliability demonstrations build confidence in SiC system insertion: a SiC JFET subjected to over 2.4 million 1200-V hard-switching events at 13 times its 150 °C rated current showed no electrical characteristics degradations (see Fig. 5) [13]. SiC Schottky barrier diodes, planar and trench MOSFETs, and JFETs are commercially available as discrete components in the voltage range of 650–3300 V from several U.S., European, and Asian suppliers. Suppliers also provide modules with multiple transistors and high currents. The 3.3-kV MOSFETs became commercially available from a large manufacturer in 2022. Historically, a 1200-V SiC MOSFET, released by Cree in 2011, was the first commercial

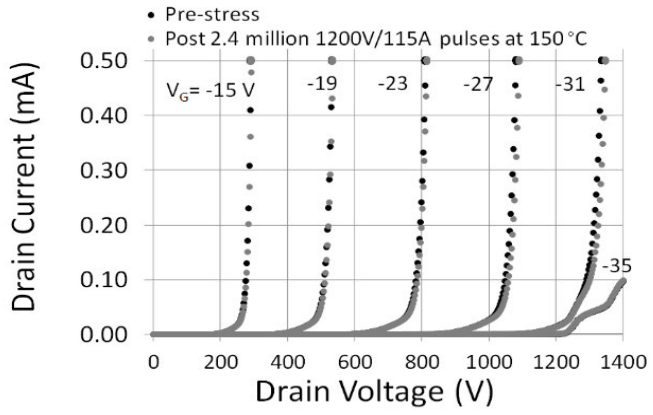


Fig. 5. Blocking voltage JFET curves before (black circles) and after (gray circles) more than 2.4 million hard-switching events at 150 °C and at 13 times the JFET's rated current. The blocking voltage characteristics are measured at 25 °C and are unchanged.

SiC transistor [14]. Today, the SiC MOSFET is the dominant SiC switch used in power electronics.

SiC power transistors have been commercially available since 2011 and have steadily gained market share. However, high device cost and reliability/ruggedness concerns are barriers in their mass adoption. In several applications, such as PV systems, insertion of SiC reduces overall system cost compared to Si even though SiC devices cost two to three times more than their Si counterparts. This is due to the passive and cooling system simplifications enabled by SiC high-frequency operation. Still, reducing SiC device costs is highly desirable. The SiC wafer represents 45%–65% of the overall SiC device cost, a consequence of the unique substrate fabrication specifics outlined in the discussion of Fig. 2. A SiC device cost reduction of over 20% is expected with the transition from 150- to 200-mm substrates. Further cost reductions can occur with SiC device manufacturing in fabs alongside Si. SiC devices fabricated in large Si volume fabs exploit economies of scale that lower costs. Through repurposing mature fully depreciated 150- and 200-mm Si fabs, SiC power devices can be manufactured with the relatively small investments necessary to support unique SiC processing steps, such as high-temperature implantation and anneal, and ohmic contact formation. Minimizing fabrication cost by exploiting the mature Si volume production assumes that the fab is loaded close to capacity with standard Si and SiC processes running on the same line. In addition, aggregating the demand for SiC substrates and epilayers in a few volume fabs contributes to lower material costs. Lower fabrication costs in a fully depreciated Si+SiC "capacity" loaded fab, coupled with decreased material costs, lead to significant price reductions for SiC devices. This approach offers a new opportunity for outdated Si fabs that have not kept up with the channel length reductions of the last two decades to continue manufacturing legacy Si parts while ramping up SiC fabrication that requires relatively modest 0.3-μm design rules [15].

Material and fabrication improvements improve device yields and reliability. More planar wafers, reduction of BPDs and process-generated defects, and higher quality gate oxides that reduce threshold voltage instability are all being addressed. Valuable data are being accumulated over years of field operation and are analyzed to drive device optimization. Independent facilities that perform reliability analyses of SiC devices have been established and contribute to "SiC user confidence" [16].

SiC devices are made more rugged by leveraging design tradeoffs to increase short-circuit time, which could also have the negative outcome of increased resistance. By making use of intelligent and fast gate drives with prognostic and diagnostic functions, the circuit can be cut off within the short circuit capability of the device enabling safe operation that rivals those of Si [17], [18].

Finally, a workforce well-trained in SiC power electronics is the key to creating the large device demand that will spur mass manufacturing with its cost-lowering benefits. Entities such as PowerAmerica carry out university-/industry-applied collaborative projects, offer industry-driven WBG short courses and tutorials, and match students with internship opportunities [19]. These activities train the existing workforce and prepare future SiC technologists, ensuring accelerated deployment of SiC power electronics.

In summary, SiC system advantages over Si are summarized in bullet form as follows.

1) The large bandgap and critical electric field allow for high-voltage devices with thinner layers lowering resistance and associated conduction losses. This reduces capacitance enabling efficient higher frequency operation with reduced-size passive components.
2) The large bandgap results in low intrinsic carrier concentration minimizing leakage and facilitating robust high-temperature operation.
3) The large thermal conductivity allows for high-power operation with simplified cooling management.

B. GaN Devices

1) Lateral GaN: Present Advantages: GaN high electron mobility transistors (HEMTs) grown on Si substrates have advanced rapidly for low-voltage (typically <650 V) and high-frequency (up to 1 MHz and, in some cases, greater) power conversion applications [20]. Relatives of RF transistors, their chief advantage is perhaps their growth on inexpensive, large-diameter Si substrates and their resulting compatibility with CMOS fabs. The increase in the distance between the gate and the drain in lateral devices will limit the application and use of GaN lateral devices for DER due to the cost increase resulting from the die size increase with increasing breakdown voltage. Nevertheless, lateral devices offer features that are well-suited for low-power applications (<10 kW). The 2-D electron gas (2DEG) of the GaN HEMT lateral device offers an outstanding low-resistive path for the charge carriers and bidirectionality. Lateral devices also have the advantage that the device current does not run parallel to extended defects in the epi growth, possibly making the achievement of the reliability related to these defects easier than for vertical devices. Finally, the lateral nature of the device facilitates the integration of multiple

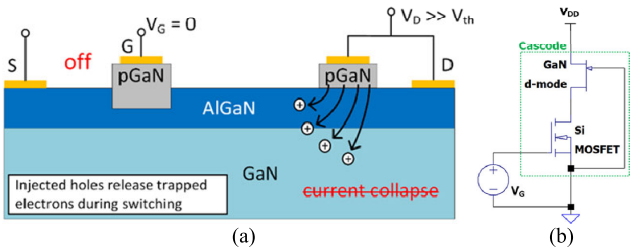


Fig. 6. Examples of (a) HD-GIT in an enhancement-mode configuration with a p-GaN gate and (b) circuit schematic for the setup of a cascode configuration with a depletion-mode GaN HEMT and an enhancement-mode Si MOSFET.

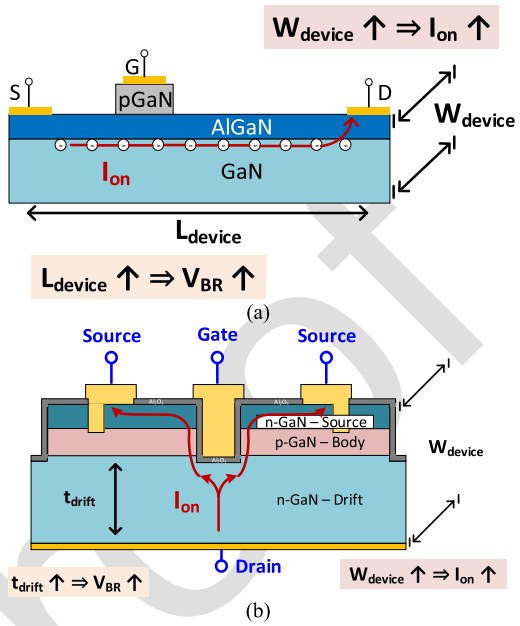


Fig. 7. Depictions of voltage and current scaling rules for both (a) lateral (HEMT) and (b) vertical (trench MOSFET) device architectures.

devices together within a single die and can enable the initial building of some logic functionality [21]. Although the logic would be limited to RTL or nMOS type, the complexity of the logic is only required to enable basic safety and drive functionalities. Thus, many low-power applications can take advantage of the integration benefit when the size/volume of the final product is of importance.

For those low-power applications where the total converter volume and weight are major driving factors, the performance of these lateral GaN power switches is second to none. Combining a much higher switching frequency (a 5–10× improvement over SiC devices) and lower ON-resistance due to the 2DEG channel creates a platform for significantly reducing the volume of passive components and the required heatsinking volume. In the past few years, the industry has been tasked with overcoming the reliability challenges associated with the poor reliability of normally-off GaN devices. There have been two prevailing commercial strategies for creating that normally-off capability for GaN HEMTs: a p-GaN gate or a cascode configuration. The p-GaN gated device is the only true enhancement-mode configuration between the two, and substantial progress has been made in reducing dynamic R_{on} and increasing reliability for this device type. Advanced structures, such as the hybrid drain gate injection transistor (HD-GIT) [see Fig. 6(a)], have been demonstrated to fully eliminate current collapse phenomena [22], [23], [24]. However, depletion-mode HEMTs have inherently lower ON-resistance; since gate reliability of GaN HEMTs can be an issue and is not considered as mature as their Si counterparts, a cascode combination [25] of a d-mode GaN HEMT with an e-mode Si MOSFET becomes an effective combination [circuit example shown in Fig. 6(b)]. At this time, several companies provide normally-off GaN FETs that are qualified to the stringent automotive standard (AEC-Q101), demonstrating that the challenges of reliability concerns for lateral GaN devices have been effectively mitigated.

2) Future of GaN for High-Power Applications: Vertical Versus Lateral Architectures: DERs push the need for high-voltage, high-current, and compact power conversion systems. While small to medium levels of power generation may be appropriate applications for lateral GaN devices, larger power conversion systems (e.g., 100 kW–1 MW) require higher voltage devices with ratings of 1200 V or more [26]. This is required to minimize conduction loss, which is a significant factor in power conversion. Conduction losses are driven by high current levels, so, by pushing to a higher conversion voltage for a given power level, current is reduced, and conduction loss is, in turn, minimized. Given these requirements, it is apparent that a vertical GaN device architecture is more suited to the higher power range of DER applications compared to a lateral architecture. Vertical device architectures allow for more efficient scaling to high-power levels by decoupling the current and voltage scaling into the x/y- and z-dimensions, respectively. In a lateral device, scaling to high voltage requires increasing the length from drain to gate, hence increasing the total area of the device. Likewise, increasing the current rating requires increasing the width of the device, also resulting in an increased area [see Fig. 7(a)]. High-voltage and high-current lateral devices become costly due to the large die area requirements as the current and voltage ratings increase. In contrast, in vertical device scaling, the voltage requires an increase in drift layer thickness (in the z-direction), which makes voltage scaling independent of the device area [see Fig. 7(b)]. In this way, vertical devices can be scaled to high power by decoupling the voltage scaling from the area of the die.

Both lateral and vertical GaN device types have the potential to carve out a space in the DER application sector, with lateral device architectures occupying more of the low-power space and vertical architectures occupying the high-power space. With that in mind however, at present, lateral GaN power transistors have reached a sufficient level of maturity for these devices to be considered for use in DER power conversion applications, while vertical GaN remains quite immature.

3) Vertical GaN: Device Types, Processing Challenges, and Future Development: Vertical GaN power devices are still relatively immature, with extremely limited commercial demonstrations and only a handful of research groups demonstrating successful device operation. However, the commercial availability of 2- and 4-in native GaN substrates has spurred

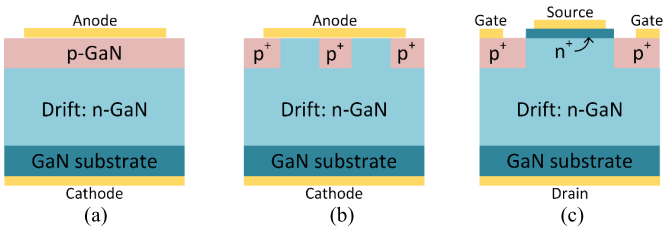


Fig. 8. Example architectures for (a) p-n diodes, (b) JBS diodes, and (c) JFETs.

interest and investment in this area, and significant progress has been made in recent years. A foundry process for vertical GaN p-n diodes is under development in the research community [27], and there has been a commercialization effort for junction field-effect transistors (JFETs) based on a vertical GaN architecture (see NEXGEN Power Systems [28]). However, neither p-n diodes nor JFETs are ideal device candidates for DERs. The p-n diodes [see Fig. 8(a)] have a large turn-on voltage and, as a result, are subject to reduced efficiency. A more suitable device is a junction barrier Schottky (JBS) diode [see Fig. 8(b)], which exhibits a low turn-on voltage like a Schottky diode but has a high reverse blocking voltage like a p-n diode. On the other hand, a major drawback for JFETs [see Fig. 8(c)] compared to MOSFETs is that a JFET is typically a normally-on device, which is a reliability and safety concern for most power electronic converters, while MOSFETs can be normally-off [29]. However, JBS diodes and MOSFETs pose unique challenges in terms of fabrication in GaN, including selective-area doping and electric field control within the device for both breakdown and reliability. As this field of research matures, the availability of these more advanced and complicated device types that are more suited to DER applications will increase, but, for now, it is limited to less-sophisticated and less-desirable devices, such as p-n diodes and JFETs.

Vertical GaN device development faces some critical challenges in developing robust high-voltage power devices. To achieve high breakdown voltages, proper attention should be paid to electric field management in the device, and electric field hotspots at the periphery of the device should be minimized. While there are several established edge termination methods for managing high fields in SiC devices, the most popular approaches rely on ion-implanted structures to spread the field. These edge termination methods for Si and SiC devices pose a challenge in GaN due to limitations in selective-area doping. Activation of implanted species in GaN, specifically the p-type dopant [Mg], requires high annealing temperatures approaching or exceeding 1300 °C, which causes the decomposition of GaN at atmospheric pressure. As a result of challenges with selective-area doping, creating some of these more complicated device architectures requires complex epitaxy employing etch-and-regrowth methods. Despite these concerns, vertical GaN p-n diodes have been demonstrated with blocking voltages over 5 kV [30], showing great potential for future devices. There is more work to be done to push the blocking voltage higher, and achieving ultralow doping in the drift region is no small task. Compensating defects in the epitaxy are a roadblock to creating drift regions with doping levels below 1×10^{15} cm^{-3} although progress is being made in this area to enable vertical GaN devices capable of >5-kV blocking capability. As development efforts continue and demonstrations of >5-kV GaN devices appear in the near future, the promise of vertical GaN for higher power DER applications will grow stronger. For today, vertical GaN remains significantly behind SiC, and its development will take time to reach maturity.

When considering the development and eventual adoption of vertical GaN, these devices must broadly compete with existing SiC devices or be relegated to niche applications (e.g., 20-kV surge arrestor [31]). In direct comparison, vertical GaN is expected to maintain all the general material-specific advantages over SiC: higher critical electric field, higher mobilities, higher saturation velocity, and so on. For specific structures, such as vertical GaN MOSFETs, three times higher channel mobilities are expected [32]. However, due to challenges with selective area doping, the MOSFET cell pitch for GaN may always lag behind SiC, which would make the advantage of GaN less compelling. In addition, for the extreme end of voltage and current, the lack of conductivity modulation and high-level injection effects in GaN makes SiC more attractive. Conductivity modulation is a useful tool to lower resistance in ultrathick (>200 μm) epi layers, which cannot be achieved in GaN due to low carrier lifetimes. As more innovation occurs in the vertical GaN space, we may see additional solutions that improve the value proposition of vertical GaN.

In summary, an overview of the value proposition of vertical GaN is given as follows.

1) At the material and device levels, GaN retains several of the advantages of SiC summarized earlier.
2) In terms of materials, compared to SiC, vertical GaN yields modest material-based advantages (critical e-field, bulk mobility, and saturation velocity) and disadvantageous thermal performance.
3) Compared to SiC MOSFET, vertical GaN yields three times higher channel mobility that translates to a significant advantage for ON-resistance for voltage classes under 2 kV. In addition, for the latter, cell pitch is likely less favorable even with further maturation of GaN technology, and conductivity modulation and high level of injection are found lacking (which is disadvantageous for 10 kV and beyond).
4) Compared to lateral GaN (HEMTs), vertical GaN scales better for high voltage (>1.2 kV) and high current (>100 A). However, for the vertical GaN, the lack of a 2DEG implies that the operational switching frequency is likely ten times lower (50 kHz versus 500 kHz).

III. Ultrawide Bandgap Devices

A. Advantages of UWBG PSDs Compared to SiC and GaN

The UWBG PSDs are an emerging class of materials that are loosely defined as having bandgaps larger than that of GaN, i.e., $E_G > 3.4$ eV. A comprehensive review of the UWBGs has been published, which describes many of the key issues for this

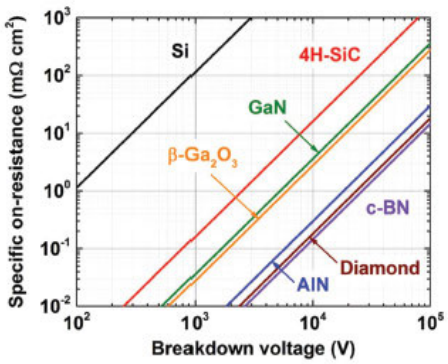


Fig. 9. Unipolar figure of merit for selected WBG and UWBG semiconductors. Reproduced from [33] with permission.

class of materials [33] (see Fig. 9), in addition to reviews specific to several UWBG materials [34], [35], [36]. Furthermore, the Office of Science within the U.S. Department of Energy has recently established an Energy Frontier Research Center focused on UWBG semiconductors, targeting their use in the future electricity grid [37]. While many materials fall into this category, the most mature are aluminum GaN (AlGaN), diamond (the cubic form of carbon), and beta gallium oxide (b-Ga_2O_3; other crystal structures are also possible). In addition, related UWBG materials include $(Al_xGa_{1-x})_2O_3$, cubic boron nitride (c-BN), transition-metal nitrides, and the II-IV nitrides. The UWBG semiconductors may have an advantage over SiC and GaN largely due to the scaling of their critical electric field for avalanche breakdown, which is generally accepted to follow a power law in bandgap $E_C \sim E_G^m$ [38] (with m around 2) although the exact value of the exponent is the subject of debate [39]. This leads not only to the ability to fabricate PSDs with higher breakdown voltages (possibly many tens of kilovolts), but UWBG devices would also have lower ON-resistance for a given blocking voltage, as dictated by the unipolar figure of merit [40]. This essentially is the same advantage that SiC and GaN have over Si but extended to the next generation of materials. This is illustrated in Fig. 9. From the FOM, a diamond shows the potential to be an ideal material for high-power electronics, as the combination of ultrahigh breakdown field and high thermal conductivity is rare in a semiconductor. Diamond diode projects have demonstrated an increase in power density by at least 30× compared to that of SiC and GaN.

B. Challenges for UWBG Semiconductors

While the UWBG materials have great potential, they are still immature, and numerous challenges exist related to their growth and processing, not to mention the eventual scaling of their fabrication to economical large-scale production. While native AlN, diamond, and Ga_2O_3 substrates are available, only for the latter are these substrates routinely produced in large diameters at low process cost. Indeed, the availability of high-quality, n-type Ga_2O_3 substrates (due to their ability to be grown from the melt) is one reason that devices made from this material have been heavily researched. While there is nothing fundamental that should stop single-crystal diamond substrates from scaling, the efforts have been painstakingly slow. This raises concerns about the potential use of diamond as a scalable semiconductor. However, it should be noted here that foundries are coming up with ambitious but practical solutions that can handle small-size wafers [41].

Beyond substrates, a key challenge for all UWBG semiconductors is impurity doping, which is asymmetric, meaning that doping of one type is much more difficult to achieve than doping of the other type. This is because the dopant atom of one type is typically very deep in the bandgap. For AlGaN, p-type doping is difficult across the entire compositional range [42], and for AlN ($E_G \approx 6.2$ eV), it is practically impossible, as the Mg dopant is 0.5 eV deep in the gap and, hence, is a deep level rather than a shallow dopant. Even n-type doping is difficult for Al compositions x greater than about 0.85. For diamonds, the situation is the opposite, with n-type doping being extremely difficult to achieve. Finally, Ga_2O_3 cannot be p-type doped at all, eliminating the possibility of fabricating bipolar devices.

Other challenges exist as well. For example, ohmic contacts are extremely difficult to form on UWBG semiconductors due to the high potential barrier that forms between the semiconductor and most metals [43]. This can conversely be advantageous when forming Schottky gates to HEMTs and similar structures. In alloyed materials such as AlGaN, alloy scattering reduces low-field mobility. However, this too can be advantageous because, even though the mobility and, consequently, the current density are low, they are also insensitive to temperature, enabling stable operation over a wide temperature range [44]. Alloying can also reduce the thermal conductivity in AlGaN, and the thermal conductivity of β-Ga_2O_3 is quite low due to its complex crystal structure.

C. UWBG Device Results

Despite the challenges outlined above, various devices have been demonstrated in several of the UWBG semiconductors. For Ga_2O_3, this has been largely enabled by the availability of large-area n-type substrates as noted above, and demonstrated device types include Schottky diodes, MOSFETs, and MESFETs [35], [36]. In Al-rich AlGaN, most device demonstrations to date have been HEMTs and related structures although some vertical devices, such as p-n and Schottky diodes, have also been reported [34]. Diodes have also been demonstrated in diamonds [45], in addition to lateral transistors using surface doping. Recent advances in diamonds have demonstrated n-type doping by phosphorus. In addition, p-type diamond is readily available, and these two successful doping schemes establish the potential of vertical p-n-p and p-n-i-p power devices based on homoepitaxial diamond layers. The ARPA-E SWITCHES effort demonstrated p-i-n diodes blocking up to 1 kV [46]. The NASA HOTTech program led to the demonstration of high-temperature operation (up to 650 °C) of diamond diodes [47], checking yet another important box that will impact power electronics. In general, all these devices are research prototypes, and more work is needed on the fundamentals of the UWBG materials and their processing into devices before they can be considered practical

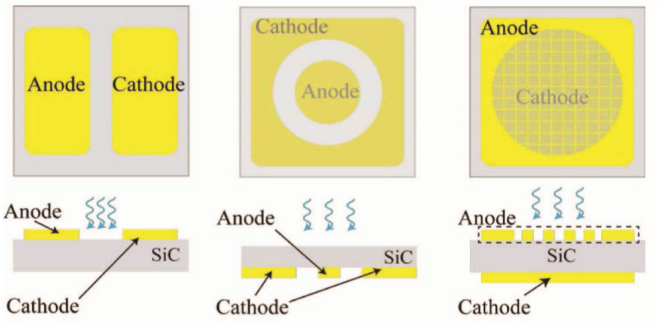


Fig. 10. PCSS in (a) lateral or in-line, (b) radial, and (c) vertical geometry configuration [48].

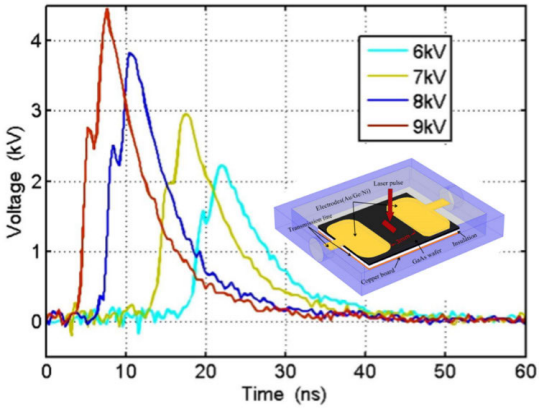


Fig. 11. Quenched high-gain PCSS operation [54].

contenders for use with DERs. Nevertheless, if they mature sufficiently, they will hold great promise for very dramatic improvements in distributed energy systems.

IV. Optically Activated PSDs

A. Photoconductive Semiconductor Switch

PCSS technology has been under development for several decades, beginning with Si, then GaAs, and recently with WBG and UWBG materials. These devices are typically made of semi-insulating semiconductors that are triggered using an incident light pulse, typically from a laser, although electron beams have been reported in the case of diamonds. PCSS can be split into two broad categories: linear and high gain. In a linear PCSS, one electron is created per absorbed photon, and the device conducts current in an ohmic behavior when illuminated. In a high-gain PCSS, an avalanching process is typically employed, and many electrons are created per incident photon. Linear PCSSs have the advantage of greater control and reliability, while high-gain PCSSs reduce light requirements. Furthermore, PCSS is classified as *intrinsic* or *extrinsic*. An intrinsic PCSS uses above band gap light to create carriers, while an extrinsic PCSS uses below band gap light to generate carriers from deep-level dopants. In general, the strengths of PCSS devices can be summarized as follows: 1) simultaneous triggering of multiple PCSS using the same optical source (minimal jitter); 2) arbitrary high voltage and current are achieved (at the cost of increased laser size); and 3) extremely fast turn-on and turn-off times compared to comparably rated electronic devices.

Several geometries have been tested for varying applications, including lateral, radial, vertical with top illumination, and edge with side illumination. The first three geometries are outlined in Fig. 10. There are also vertical geometries with edge illumination, in which the optical input is fed through the side of the PCSS. The most widely implemented mode of PCSS is the linear operation, characteristic of linear output with input optical power. Table I summarizes PCSS linear mode operation from the literature with metrics encompassing ON-time (Ton), leakage current (Ileak), peak current (Imax), maximum blocking voltage (Vmax), and current slew rate (*dI/dt*). SiC PCSS shows exceptional power handling capability, while GaAs PCSS show exceptional turn-on times capable of sub-ns.

TABLE I
Survey of PCSS Operating in the Linear Mode

Ref.	Material	Geometry	Ton [ns]	Ileak [nA]	Imax [kA]	Vmax [kV]	dI/dt [kA/µs]
[48]	6H SiC	Vertical	2	10	1.5	17	> 100
[49]	4H SiC	Lateral/In-line	10	300	0.2	10	20
[50]	4H SiC	Radial	4	4000	1	30	> 100
[51]	GaAs	Lateral/In-line	0.2	NR	0.25	1.7	1250
[52]	GaAs	Lateral/In-line	80	NR	3	30	37
[53]	GaN	Lateral/In-line	0.16	NR	0.02	40	> 100

Additional modes of operation have been explored in PCSS to achieve higher output power for a given input optical power. These high-gain modes of operation involve negative differential mobility (NDM) materials, whereby, after a certain electric field, the mobility drops rather than increases. NDM leads to the formation of charge carrier domains called Gunn domains that result from a field screening effect causing an accumulation of charge that can propagate throughout the material until it is collected at the opposing contact. The lock-on mode of operation is a phenomenon, whereby the switch voltage persists even after optical excitation has ceased and is independent of the charge voltage if it is above the lock-on entry threshold, which is very close to the NDM threshold. Lock-on devices typically have low reliability, repeatability, and longevity due to destructive current filaments, which almost always accompany lock-on. Avalanche mode of operation occurs close to the semiconductor breakdown field allowing high gain due to impact ionization. PCSS operation and reliability in the avalanche mode are not well documented. The high-gain modes of operation are outlined in Table II, where GaN values are predicted by numerical simulation and not experimentally demonstrated. In Table II, the threshold is the field required for the mobility to begin decreasing, and the entry threshold is the field required to initiate lock-on behavior, while the closed state field is required to maintain it, and the avalanche entry threshold is the field required for the avalanche to begin.

A literature survey of high-gain PCSS is summarized in Table III. In addition to the parameters from Table I, we include latency, which relates to the time needed for the nonlinear mode to take effect after triggering. GaAs

TABLE II
DIFFERENT OPERATION MODES OF HIGH-GAIN PCSS

Mode	Fields across switch	GaAs	InP	GaN
NDM	Threshold [kV/cm]	3.5	10	~150
Lock-on	Entry threshold [kV/cm]	3.5-8	15	150 (predicted)
	Closed-state field [kV/cm]	~4-8	14	138 (predicted)
Avalanche	Entry threshold [kV/cm]	~20-25	~500	~5000
	Closed-state field [kV/cm]	Like lock-on	Unknown	Unknown

TABLE III
SURVEY OF PCSS OPERATING IN THE NONLINEAR MODE

Ref.	Material	Mode	Geometry	Latency [ns]	Ton [ns]	Ileak [nA]	Imax [kA]	Vmax [kV]	dI/dt [kA/us]
27	GaAs	Lock-on	In-line	Small	0.3	NR	0.7	3.5	2300
		Avalanche		0.5-50	0.44		NR	35	NR
45	GaAs	High-gain*	In-line	5-20	3	NR	0.09	4.5	30
46	GaN	Lock-on+	1D model	NR	0.16	NR	0.02	40	> 100

* High-gain mode is passively quenched before lock-on can initiate
+ Numerical study, not experimentally demonstrated

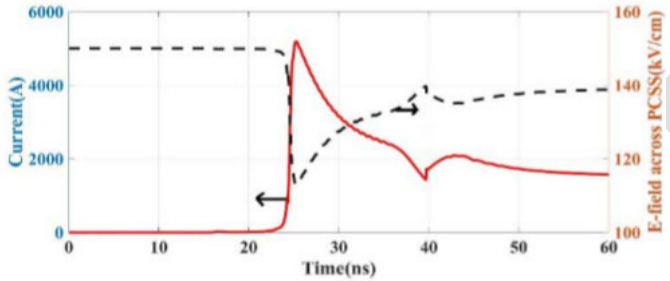


Fig. 12. Theoretical numerical study of lock-on in GaN from [55], [56], and [72].

can achieve exceptional turn-on times in both lock-on and avalanche modes. Shi et al. reported rapid quenching of the lock-on mode enabling high gain without the effects of current filamenting, as shown in Fig. 11. GaN is also predicted to have exceptionally fast turn-on times in the lock-on mode, as shown in Fig. 12.

UWBG materials offer the potential for substantially improved performance with reduced illumination intensity. However, due to their exceptionally wide band gaps, no practical laser sources exist for band-to-band illumination. Of these materials, diamond is the most studied, but reports are sparse. Polycrystalline diamond has been illuminated with both visible and ultraviolet illumination but is likely not suitable for high-power applications due to its poor electronic properties. Single-crystal diamond has been illuminated with an electron beam, analogous to the laser but also impractical. Recently, Hall et al. demonstrated an N-doped diamond PCSS with comparable responsivity compared to SiC.

B. GaN PCSS

GaN is a promising WBG material [30], [57], [58] and offers important expected improvements in power device performance, including lower switching losses [59], higher frequency operation [60], and higher power density, leading to systems with lower size, weight, and power (low-SWaP). For GaN PCSS devices, researchers have evaluated GaN as a candidate material and find it highly motivating because of the advantageous material characteristics, including increased breakdown fields of ~3 MV/cm, large electron peak drift velocity of >2.5 E7 cm/s, the high volumetric heat capacity of ~3 J/cm^{3}K, and large simulated photoconductive power gain of ~30 TW/J [61]. Researchers have successfully predicted and/or demonstrated GaN PCSS operating in the linear mode [62], [63], [64] using Fe- or C-doped GaN material to render the material semi-insulating for increased blocking voltages in the OFF-state. Early PCSS devices were used to generate THz or near THz radiation. These devices, fabricated in lateral and vertical geometries, demonstrated fast switching times of ≤10 ns, often limited by circuit and/or laser trigger performance with results indicating the carrier recombination lifetime to be <1 ns [53], and investigated the change in material resistivity between the ON- and OFF-states (greater than 10^8) to evaluate the prototype switches [53], [65]. Lateral device geometries used surface electrodes spaced with varying gap distances of tens of micrometers less than 2 mm with designs, including constant gaps, annular, and interdigitated configurations.

Vertical devices were made using large, mm size, and top and bottom contacts on thick (~0.4 mm) semi-insulating substrate materials. These important results, while promising, often demonstrated lower than predicted voltage holdoff performance based on material parameters likely due to material or surface defects, electric field design, or device fabrication-induced imperfections limiting the performance. With continued efforts, material improvements, and fabrication and design improvements [66], [67], the linear mode switch performance has improved with demonstrated higher holdoff fields as high as 1.6 MV/cm being demonstrated [68]. In addition, experiments were conducted to understand and predict the wavelength-dependent behavior of the triggering mechanism showing the expected band-edge absorption mechanism of the material and including studies looking at subbandgap triggering for extrinsic (defect-induced) carrier generation in the material. Optical trigger sources used in these studies were typically Nd:YAG lasers with frequency modifications, and the wavelengths used included near or above bandgap (266–355 nm) and below bandgap (532 nm) energies with the largest photoresponse in linear switches seen with near or above bandgap wavelengths. Pulse energies in the mJ range were used, and energy densities were not systematically reported and hence difficult to compare.

Previous GaAs-based PCSS was demonstrated in the nonlinear operating mode in both linear [69] and vertical geometries [70], where current flows after the termination of the external optical source. This has obvious implications for the switching mode efficiency as the requirements on the optical triggering energy are greatly reduced. Because of the advantageous material characteristics of GaN, the possibility of nonlinear or high-gain mode operation of GaN PCSS devices is of particular interest to scale switch voltages and power densities, especially when compared to GaAs devices.

To date, no SiC-based nonlinear PCSS operation has been observed and may be related to the indirect bandgap of the material. The GaN PCSS nonlinear mode was predicted [56] with simulations showing the effect of trap or defect-related mechanisms for semi-insulating GaN, including native defects, such as gallium or nitrogen vacancies, which can act as acceptors or donors, and impurity-related defects, including C, Fe, or Mn, which act as acceptors to compensate the material resulting in high resistivity. The performance of the simulated switch is highly dependent on the energy level of the trap states and the trap density. However, the lowest fields predicted to observe nonlinear behavior, ∼150 kV/cm, corresponded to the presence of mid-gap states. This is needed in trap-to-band impact ionization processes and corresponds well to the intentional impurities in semi-insulating GaN materials.

The first reported experimental demonstration of nonlinear GaN PCSS operation was observed with lateral devices having 0.6-mm gap spacings, showing the characteristic indicators of the nonlinear mode, such as nonlinear GaAs devices [71]. These include persistent conductivity after the optical signal is terminated, observation of nondamaging filamentary current channels, and ON-state lock-on fields across the device. Observations of nonlinear device operation were seen in semi-insulating materials with mid-gap traps with either Mn or Fe doping, and the threshold fields for the nonlinear operation were ∼25 kV/cm, far below the surface breakdown fields of the device, and remaining lock-on fields of 3 kV/cm. Optical trigger energies of ∼30 μJ at 532 nm were used to trigger the nonlinear operation and were significantly lower than linear switch reports. Surface effects may also contribute to device operation as the nonlinear effect was not observed with the devices submerged in Fluorinert FC-70. More work is currently underway to understand the device performance and develop models to explain the physical mechanism of the GaN-based switch, which may be significantly different than the GaAs device switch operation.

Based on the successful demonstration of linear and nonlinear GaN PCSS devices, future work is focused on improving the device design and performance for voltage and current scaling to realize the GaN material advantages while improving and evaluating device reliability to be considered for field use. Perhaps, the most important to the realization of GaN PCSS devices is understanding the implications of available compact optical triggering sources to enable applications that are space-, weight-, and cost-sensitive.

Considerable work was done in GaAs devices [70], [72] to improve and understand reliability, and similar efforts are underway for the improvement of GaN devices. The main factors that influenced device lifetime in GaAs devices included electrical circuit properties containing the switch, the optical trigger properties, and the PCSS switch properties, themselves. Circuit properties governed the operating voltage and current of the PCSS, the pulsed waveform characteristics, and the design of the materials and peak electric field near the PCSS device. Optical trigger properties include the trigger source energy, energy density, pulse duration, and wavelength. The PCSS influencing factors included the physical layout of the switch, material properties, including intentional impurities (doping) design and surface coatings, and electrical contact design, including electrode configuration, metallization scheme, and contact polarity. Traditional circuit design for PCSS characterization typically uses a pulsed and/or switched voltage source to apply the electric field across the device carefully synchronized with the optical trigger, and the PCSS performance is determined by the device performance combined with the impedance of the rest of the circuit. Novel designs are also being proposed and simulated to improve the PCSS performance including monolithically integrated PCSS and electrical power switch structure to improve the photoelectric-conversion efficiency compared to a traditional dc charged PCSS device [73].

While understanding the switch characteristics is critical to improving device performance, the fielded applications for GaN PCSS devices will be ultimately limited by the availability of compact optical triggers. For example, one potential application for the ultrafast, nonlinear GaN switch is in the current commutation portion of a solid-state dc circuit breaker being developed under the ARPA-E BREAKERS program [74]. The proposed circuit breaker includes a normally-on leg through which the current from the system is conducted, a normally-off leg that is used to commute current from the system during a detected fault, and a shunt leg where the energy is dumped during a fault. The normally-on leg is composed of WBG semiconductor SiC transistor networks with balancing passive components all controlled by microprocessor-based controls and sensing electronics. The parallel, normally-off leg consists of the nonlinear GaN PCSS switch and a serially connected capacitor, and the shunt leg consists of an energy-absorbing element, such as a metal-oxide varistor. When a fault is detected, the normally-on leg is turned off coordinated with a synchronized dc biasing and triggering of the GaN PCSS to commute current from the system through the PCSS. Potential applications for this circuit breaker include opportunities, such as ship-based electrical systems, where size and weight are of critical importance, necessitating optimized designs for packaging, thermal management, and integration of a compact optical trigger source. Since the GaN PCSS performance depends on the optical trigger wavelength and energy, commercially available sources will be important, as well as the PCSS design. Intrinsic switches will need to be optically triggered with short (ns scale), high-energy (μJ–mJ) pulses from at or above bandgap sources with wavelengths of ∼365 nm or shorter where low-cost, compact trigger options are limited. Alternatively, extrinsic switches can be triggered using optical wavelengths below the bandgap where optical source availability is more common including semiconductor-based laser diode options.

C. Optical Bipolar PSDs

While PCSS devices have seen significant research across different material bases, optical bipolar PSDs have shown promise for power-electronic applications [75]. This encompasses light-triggered thyristor (LTT) [76]. One of the key advantages of the LTT is the high electrical gain of the thyristor that significantly reduces the requirement for optical

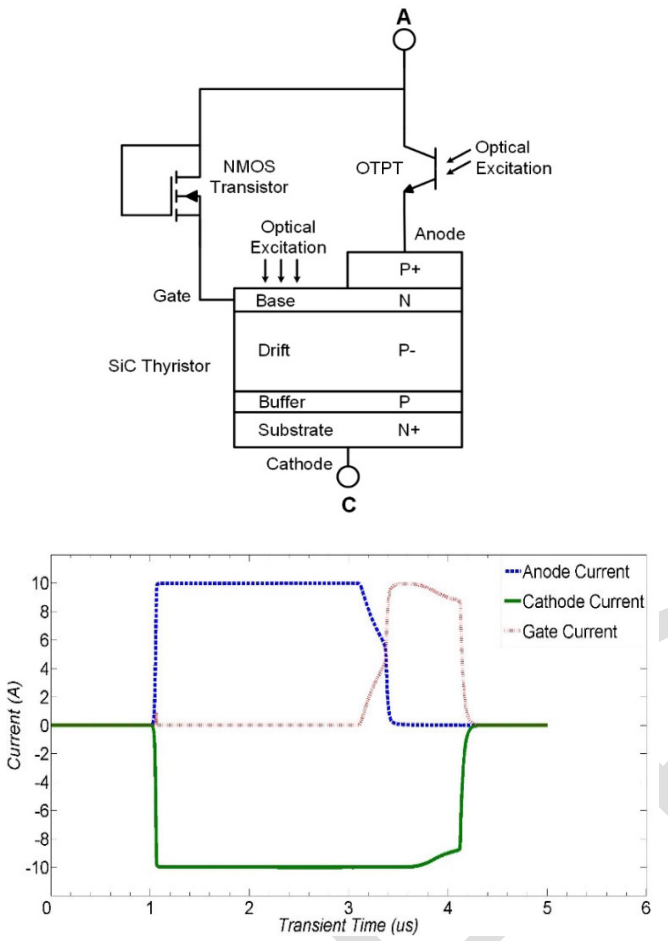


Fig. 13. Structure of an optical ETO and currents for the optical thyristor for one switching cycle.

power, which has economy of scale implications for WBG optical thyristors [77] However, the high gain of the LTT comes at the price of slow turn of time since the thyristor is a latched device.

More recently, an optical emitter-turn-off thyristor (optical ETO) [78], [79], [80] has been outlined that overcomes this limitation of the LTT. Mojab and Mazumder [81] outline how this operational mechanism for controlling a single optical ETO can be extended for higher voltages using a series of two (or more) devices. As shown in Fig. 13, this is achieved using a low-voltage optically triggered power transistor (OTPT) [82], as shown in Fig. 14, and a low-voltage MOSFET that works mutually exclusively to turn the main optical power thyristor off using unity gain turn-off mechanism. While the optical bipolar PSDs outlined above serve as the main high-voltage power device, the low-voltage optical bipolar device can also be utilized for driving high-voltage field effect transistors. Mazumder [75] and Mazumder and Sarkar [83], for instance, illustrate how two low-voltage OTPTs can be used to control the charging and discharging switching dynamics of a SiC MOSFET. Similarly, optically triggered bipolar OTPT-based cascoded SiC JFET [84] has also been realized. Other structures based on GaN are also described in reference therein.

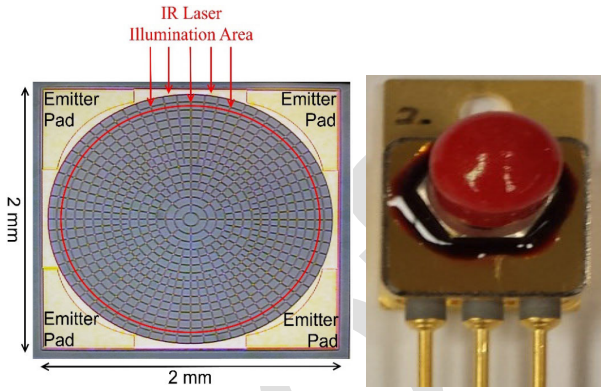


Fig. 14. Vertical experimental OTPT device geometry and actual package.

Fig. 15. Packages from the left to the right: XM3, HM, LinPak, and XHP.

V. Packaging

A. Wirebonded Modules

Commercially available wirebonded packages are optimized for Si devices rated for 650-V, 1.2-kV, 1.7-kV, 3.3-kV, and 6.5-kV applications. These modules are mainly available from Infineon, Vincotech, On Semiconductor, and Hitachi/ABB. Infineon offers IGBT half-bridge modules for all these voltage levels. Infineon offers 62-mm C-Series, EconoDUAL, PrimePACK,[1] and pressfit EasyPACK 1B and 2B modules packages for 650-V, 1.2-kV, and 1.7-kV applications [85], [86], as well as XHP and IHV module platforms for 3.3- and 6.5-kV applications [87], [88]. Hitachi and ABB provide 62Pak and LoPak1 62-mm package platforms for 1.7-kV applications, and LinPak and HiPak packages for 3.3- and 1.7-kV applications [89], [90]. Vincotech has an EconoDUAL package in a 62-mm platform for the 1.2-kV IGBT module. SiC module manufacturers, such as Wolfspeed and Rohm, have utilized the 62-mm module platform and introduced HM [91] series and BSM [92] series for both 1.2- and 1.7-kV applications. Moreover, in the same 62-mm platform, CREE has its WAB [93] package for the same 1.2- and 1.7-kV applications. XM3 is a more compact package design for a 1.2-kV application [94]. Wolfspeed has even fabricated a module incorporating GaN Systems prepacked chip in their 62-mm HM series package [95]. Fig. 15 illustrates that the fabrication processes involved in these wirebonded power modules have relatively high maturity, while these modules offer power loop inductance anywhere from 9 nH up to more than 20 nH. This high commutation loop inductance could become a limiting factor for the application of high-power WBG devices.

Packaging plays an important role in ensuring the safe and reliable operation of semiconductor devices. With high-power

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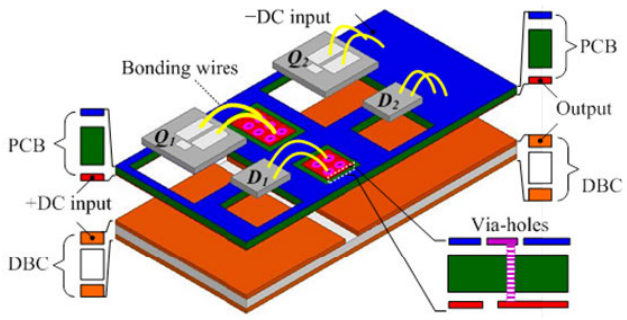

Fig. 16. Hybrid package.

and increased switching speed, the selection of materials, interconnect technologies, and layout become more and more critical. Traditional power modules designed for Si IGBTs show their limitation when exposed to the faster switching speed and high-frequency operation enabled by the new generation of WBG power devices.

Power loop inductance introduces an inductive voltage spike across the device terminal during the hard switching operation. It curtails package reliability due to the increased propensity of partial discharge and insulation failure. The external preventive approach, such as reducing switching speed, harms efficiency by increasing the switching loss. Moreover, to increase the power handling ability of the module, multiple dies are required to parallel in a switching position. An asymmetric layout will lead to uneven dynamic current sharing between the paralleled dies. This will impose a transient temperature imbalance between them and may reduce the reliability of a particular device.

Thermal resistance determines the power handling ability of semiconductor devices. Poorly designed modules will often require extensive and bulky thermal management systems that will increase the cost and reduce power density. Layout, materials, and interconnect technologies have their individual impact on power loop inductance and thermal resistance. Most of the commercial power modules use wirebonds as interconnects from the top side of the semiconductor chips. It increases the area of the commutation loop and restricts the cooling from only one side of the package. Different endeavors have been reported to replace wirebonds to reduce loop inductances and thermal resistances. Some of them are discussed in detail next. Detailed discussion and guidance to choose materials for power modules are reported in the exiting literature [96], [97] and hence not repeated here.

To reduce the loop inductance while keeping the advantages of the maturity from the wirebonded module structure, researchers have proposed a "hybrid" structure (see Fig. 16) that combines the advantages of the maturity from the fabrication processes and the low inductances from multisubstrate vertical commutation loop structures. Wang et al. [98], Chen [99], and Chen et al. [100] have reported such a structure in different designs, respectively. All these works have achieved reduced loops' inductance compared to traditional wirebonded modules.

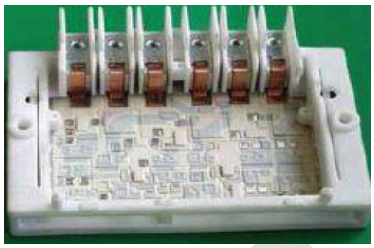

Fig. 17. SiPLIT interconnect technology.

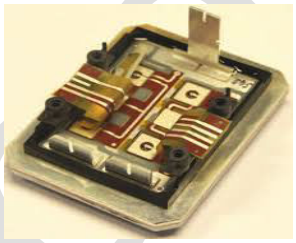

Fig. 18. SKiN technology.

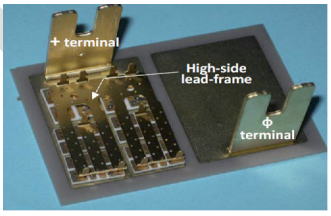

Fig. 19. DLB module package.

B. Wirebondless Modules

Wirebond has its limitations and has been identified as one of the weakest points in modern module fabrication technology. Several endeavors have been taken and new technologies tried to replace the prone-to-failure wirebonds. Siemens introduced a planar interconnect technology (SiPLIT), as shown in Fig. 17. In this technology, Cu is deposited on high-insulating film to connect the top side of the die. Through electrical and thermal characterization, it was found that up to 50% reduction in parasitic inductances and a 20% decrease in thermal resistance were achieved [101].

Semikron has brought this concept to another level and demonstrated its SKiN technology (see Fig. 18) as another interconnect technology to replace wirebonds. In SKiN technology, power chips are sintered to a DBC substrate, and another top side sintering of the power chips is done to a flexible printed circuit (FPC). This technology was introduced in 2011 and is now being used for SiC module packaging. It has shown that a loop inductance of as low as 1.4 nH can be achieved using this technology [102], [103].

Another wirebond alternative is to use copper-clip interconnection and direct leadframe bonding (DLB), as captured in Fig. 19. Woo et al. [104] demonstrated this technology and used silver sintering to connect the Cu clip to the die, where copper clips can reduce the parasitic inductance and help to achieve better heat removal from the top side of the dies. Instead of using copper clips for "pad-to-substrate"

Fig. 20. POL technology.

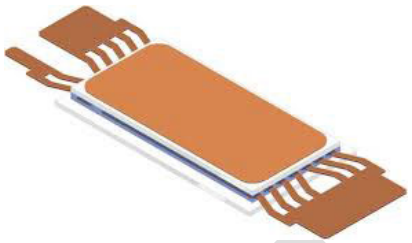

Fig. 21. Delphi 3-D packaged Viper module.

connection, Silicon Power Cooperation and STMicroelectronics demonstrated DLB on power devices. This package structure enables device-to-power terminal direct connection and, thus, can achieve reduced power loop inductance and top side cooling feature. General Electric developed a power overlay (POL) interconnect technology, as illustrated in Fig. 20, for Si and SiC packages [105]. In this package, the topside of the die is connected using a flexible substrate made of polyimide and copper. It reduces the parasitic inductance and increases the reliability of the module.

The development of 2.5-D and 3-D packages provides another pathway to further optimize the commutation loop inductance and achieve higher power density. Such a structure adopts multilayer DBC and vertical power-loop design in power modules and provides double-sided cooling capability with optimized low loop inductance. The 2.5-D design structure has two layers of metallization with the devices connected to the bottom DBC. The copper layer is etched to a desired pattern where the IGBTs and diodes are attached by soldering. The top metal connection and the bottom DBC can be connected through metal post interconnect [metal post interconnect parallel plate structure (MPIPPS)] [106], dimple array, and direct soldering/sintering (flip-chip on flex and embedded power) [107], [108], [109]. Similar designs can also be found in [110]. In 3-D modules, semiconductor chips are attached to two or more substrates, and the interconnection between them can be achieved through any technology. Hopkins et al. have proposed a prismatic module using flexible substrates and a connecting structure in the middle of the package [111]. Zhang et al. [112] used LTCC as a chip carrier sandwiched between two DBCs in a wirebondless SiC package.

Press-pack is a packaging approach that uses pressure contact as interconnect instead of wirebonding and soldering. Connections to the chips are made by physical contact pressure via external clamping between rigid electrodes and strain buffers. Zhu et al. [113] use fuzz buttons as spring contact. It shows reduced stress on the chip interface and enables double-sided cooling. Chang et al. [114] extend a similar concept from Aalborg University. PET films are used as insulators in between metal bars, while the whole package is kept together using bolts from each side.

Power chip on bus (PCoB) technology is another 3-D module design, and thick-finned copper acts as both heatsink and busbar. Power dies are electrically attached to two busbar-like power substrates directly. Molybdenum spacers are used as CTE buffers between the die and bottom substrates for reducing thermal-mechanical stress caused by CTE mismatch [115].

TABLE IV
COMPARISON AMONG DIFFERENT INTERCONNECTS TO REPLACE WIREBONDS

Packaging Scheme	Properties, Pros, and Cons
SiPLIT [101]	• Thick copper on an insulating film is used as a topside interconnect. • Reduction of power loop inductance by 50% and thermal resistance by 30% compared to traditional wire bonded packages. • Increased power handling capacity and low switching loss and overshoot.
SKiN [102]	• Dies are sintered from top and bottom sides. • Sintering improves the bonding reliability compared to solder-based joints. • Very low power loop inductance (~ 1.4 nH) • Reduced switching loss and overshoot
DLB [104]	• Copper clips are used as top side interconnect. • Silver sintering is the attachment method, hence increased reliability compared to solder joints. • Reduced power loop inductance and thermal resistance
POL [105]	• Wire bonds are replaced with flexible substates. • Low power loop inductance reduced switching loss and overshoot.
Press Pack [113]	• Pressure contacts-based connection from top side of the dies instead of soldering/sintering • Reduced stress on the dies. • Low power loop inductance and thermal resistance.
PCoB [115]	• Double sided cooling enabled by 3D packaging structure. • Low power loop inductance due to small loop area.

The 0.5 °C/W thermal resistance and 8-nH loop inductance have been reported for this package.

These 2.5-D and 3-D packages provide both superior thermal and electrical performances, and thus, it has been adopted by the automotive industry as a trend for future advanced EV drives. Most of these modules in EV applications have transfer-molded packages and double-sided cooling features to be able to withstand the high-temperature operation environment. Hitachi [116], Delphi [117] (see Fig. 21), Toyota [118], ST Microelectronics [119], Mitsubishi [120], and Infineon [121] modules are now implemented inside the automobiles for different purposes and types of power conversion. Table IV provides a comprehensive summary of these interconnect technologies.

C. Advanced High-Voltage Power Module

The increasing development of distributed energy systems also poses strong demand for medium- and high-voltage power

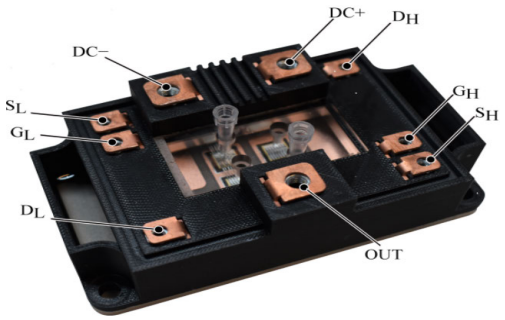

Fig. 22. 10-kV module from Aalborg University.

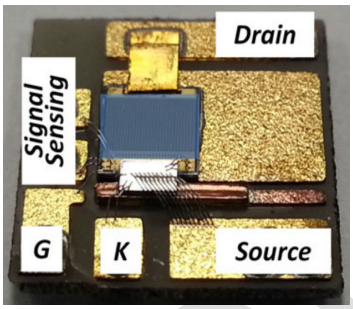

Fig. 23. CPES PQFN GaN package.

Fig. 24. CREE high-temperature GaN package.

Fig. 25. ViSIC 1.2-kV GaN module.

modules (>6.5 kV). Besides the commercially available packages, advanced designs for high-voltage module development are also in progress to support higher voltage and better performance. The U.S. Army Research Laboratory has a lot of research efforts in HV SiC diode and SGTO packaging using different structures, including using metal-tab interconnection, ceramic lid, and Kovar metal connection to achieve both low inductance and better thermal management, using printed ABS housing for enhanced insulation [122]. North Carolina State University [123] and CREE/Powerex [124] have been demonstrating their 10-kV designs in wirebonded power modules. These module designs require specific consideration of insulation, high electric field mitigation, and *dV/dt*-induced noise control. Virginia Tech has proposed another 10-kV module with stacked DBC and spring-loaded pins connection, and has used a CM noise screen to mitigate the CM noise generation from the module and achieved 13-dB reduction [125]. Munk-Nielsen et al. from Aalborg University have designed a 10-kV module in a single DBC substrate and optimized it for lower CM noise emission [126]. Deshpande et al. [127] proposed, as shown in Fig. 22, stacked DBC-based cavitated substrate for balanced *E*-field, voltage, and CM noise reduction from the 15-kV SiC module.

GaN-based HEMTs provide high switching frequency with low loss and radiation harden features in harsh environment applications and, thus, start getting popular in 650-V and 1.2-kV applications [128], [129], [130], [131]. Available products of EPC were initially based on ball grid array (BGA) and later adopted line grid array (LGA) technology where solder bumps are placed on one side of the chip for their solder ability. The intertwined structure of the LGA enables a low-inductance package [132]. Fraunhofer IZM and TU Berlin worked together and came up with a chip in polymer package [133], [134], [135] to switch currents of 80 A or more. This technology embeds power chips into low-profile polymer packages without using a DBC substrate. GaN Systems has patented the GaNPx package for a near chip-scale version of their device enabling high thermal performance and low package inductance using a very similar concept. CPES has presented a package using a metal connection and stack-die structure for 650-V cascode GaN devices and packaged it in a quad flat no-lead (PQFN) compatible format [136] (see Fig. 23). With collaboration with GaN systems, APEI (Wolfspeed) has developed a high-temperature high-current package for the discrete device named as X'6 power discrete package [137] (see Fig. 24).

The parasitics from the gate drive layout, especially the gate loop inductance and the common source inductance, have strong influences on the power module switching performance. Heterogeneously integrated power modules with Kelvin-source connected gate drive circuits and power devices can significantly reduce gate drive parasitics and improve module performance.

ViSIC has its gate driver integrated 1.2-kV GaN module (see Fig. 25) using two series connected GaN HEMT per switching position in half-bridge configuration [138]. GaN systems have an insulated metal substrate (IMS) power module where a metal core PCB is employed. Jørgensen et al. [139] from Aalborg University have shown a hybrid PCB-DBC-based package for a full bridge module. This module complies with Infineon's commercially available Easy 1B package [139] (see Fig. 26). Emon [140] has extended a similar concept for half-bridge phase leg configuration with optimized power loop (0.68 nH) and gate loop inductances (1.2 nH) with a Kelvin connection. Wang et al. [141] proposed a gate driver-integrated

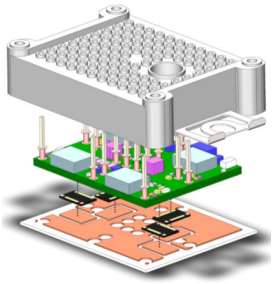

Fig. 26. GaN full-bridge module.

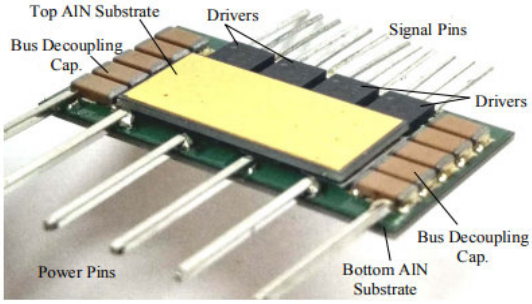

Fig. 27. Double-sided cooled GaN half-bridge module.

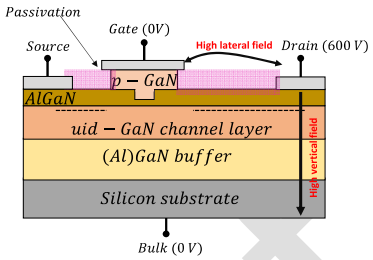

Fig. 28. Schematic of a GaN HEMT, showing the most relevant layers within the structure of the device, and the location of high lateral and vertical fields reached by the device during the OFF-state.

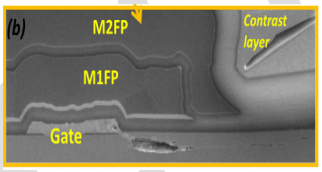

Fig. 29. TEM performed on a cross section showing a severe degradation in the gate side/edge [152]. ©2017 IEEE. Reprinted, with permission, from Rossetto et al. [152].

double-sided cooled solution with 0.95-nH commutation loop inductance and 2-nH gate loop inductance, as shown in Fig. 27.

In order to further reduce the parasitics in the gate driving loop, solutions using monolithically integrated gate drivers with power devices are also proposed by industry and academia researchers. Navitas proposed a GaN Power IC solution using AllGaN[1] process development kits (PDKs) to monolithically integrate 650-V GaN IC circuits (drive, logic) with GaN FETs [142]. EPC [143] and GaNPower International [144] also proposed their integrated products that combine low-power IC circuits with GaN HEMT. Xu et al. [145], Moench et al. [146], Zhu and Matioli [147], Zaman et al. [148], Liang et al. [149], Tang et al. [150], and Noike et al. [151] present monolithic integration efforts from academia, in which most groups realized logic and fate driver integration with GaN HEMTs. Zaman et al. [148] present the gate driver integration and current sensor integration with the GaN power device, while Xu et al. [145] also present the monolithic integration of the gate driver and protection circuits.

VI. Device Reliability

A. OFF-State Degradation of GaN-HEMTs: Extrinsic and Intrinsic Failures

GaN is a WBG semiconductor and has a high breakdown field of 3.3 MV/cm. This value is 11 times higher than that of Si (0.3 MV/cm), and this means that, for the same breakdown voltage, GaN devices can be ∼11 times thinner than their Si counterparts. The OFF-state operation can result in a very high electric field, both in the semiconductor material and the surrounding dielectrics. During the OFF-state operation, the gate, the source, and the bulk are typically grounded (for E-mode transistors), while the drain can be at 600–900 V, depending on the analyzed technology. This may result in high lateral and vertical fields that may approach the breakdown limits of the devices (see a schematic representation in Fig. 28).

The lateral breakdown voltage mostly depends on the geometry of the device and is typically proportional to the distance between the gate and the drain terminals. Recent papers [152] and [153] demonstrated that lateral breakdown can be an extrinsic mechanism, related to the failure of the device in correspondence with the gate head, on the drain side edge, where the electric field is maximum. As discussed in [152], the breakdown voltage decreases with the increasing length of the gate head on the drain side, indicating that a careful device design is the key for obtaining high reliability.

The hypothesis was confirmed through transmission electron microscopy (TEM) (see Fig. 29) that demonstrated the generation of a leakage path between the gate metal and the channel of the transistor. Approaches for improving the reliability were proposed, i.e., by using graded SiN passivation with increased thickness. This process is an extrinsic process that is related to the failure of the SiN dielectric at the edge of the gate head, and for this reason, considerations of time-dependent dielectric breakdown apply. Hence, the E-model (considering that ln(TTF)∼-βV [155], where TTF represents the time to failure, V the stress voltage, and β the slope of the TTF versus V plot with units in V^{-1}) is preliminarily applied to describe the degradation kinetics [153].

The vertical breakdown voltage depends on the properties of the epitaxial layers. When the devices are operated OFF-state, a large field drops on the uid-channel layer and the GaN buffer [156]. Recent papers [157] indicated that GaN stacks subject to high vertical fields can suffer from a time-dependent breakdown, similar to what happens in dielectrics. Time-to-failure was found to be Weibull-distributed, with β greater than one, indicating an intrinsic failure process. Factor β was found to depend on the stress voltage since different voltage

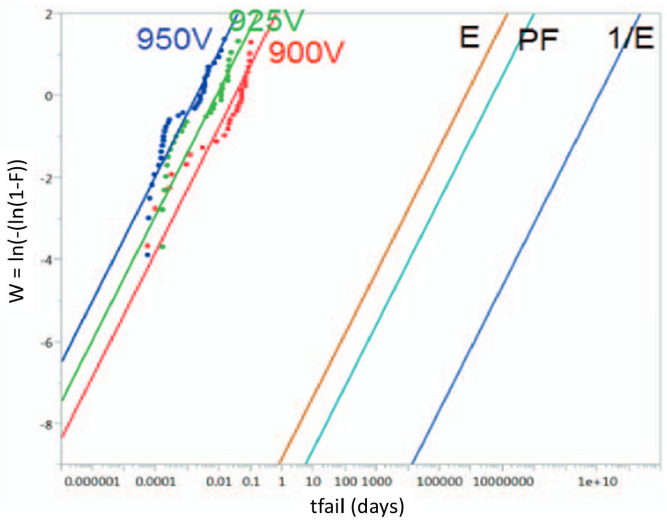

Fig. 30. High-voltage OFF-state stress at $T = 200$ °C on 100-mΩ power transistors at $V_{ds} = 900$, 925, and 950 V. Data are plotted on a Weibull plot; three different extrapolation models are used: E, $1/E$, and PF. Field extrapolation for the three models is done at $T = 200$ °C and $V_{ds} = 600$ V [159]. ©2015 IEEE. Reprinted, with permission, from Moens et al. [159].

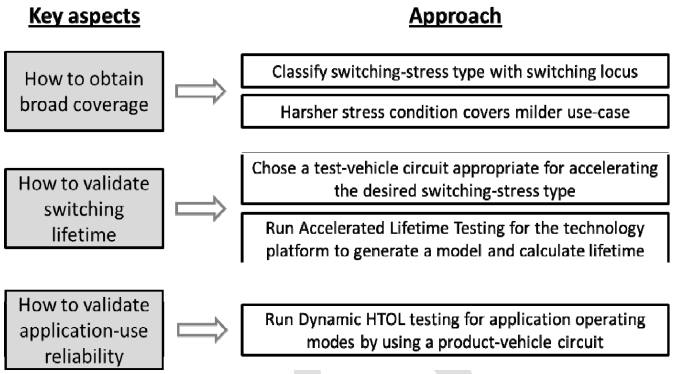

Fig. 31. Simplified explanation of the approach for assuring GaN product switching reliability, courtesy JEDEC JEP180.

ranges may have different leakage mechanisms [158]. The failure mechanism was found to be strongly field-dependent and weakly thermally activated [$E_a = 0.25$ eV, considering an acceleration factor AF(T) = $\exp(E_a/k)$ $(1/T\text{-}1/T_{\text{stress}})$] [159]. In AF(T), E_a represents the activation energy, k the Boltzmann constant, and T and T_{stress} are the absolute temperatures at which the acceleration factor is calculated, and the accelerated stress condition is conducted. The failure was ascribed to the creation of defective paths (due to percolation) between the drain and substrate.

Intrinsic reliability was found to significantly depend on buffer leakage [160]. For high OFF-state voltages, drain leakage was found to be related to Poole–Frenkel (PF) conduction, allowing charge stored in C_N acceptors to leak away [157], [158], [159], [160], [161], [162]. The reliability can be evaluated by high-temperature reverse bias (HTRB, e.g., $Tj = 150$ °C and $V_{\text{DS}} = 600$ V) or high-voltage OFF-state (HVOS, high voltage on drain, in pinch-off conditions, with substrate, and source at ground) stress. Intrinsic failures typically follow a Weibull distribution [157], [162]; different field-acceleration models have been considered, including E, $1/E$, and PF. While the E-model [TTF∼$\exp(-\beta V)$] is the most conservative [158], it was recently proposed [162] that the PF model can effectively reproduce the experimental data (see Fig. 30). In general, the acceleration model may depend on the dominant leakage mechanism near breakdown (PF [162], thermionic emission, variable range hopping, and so on [161], [163]): the modeling and tuning of vertical leakage are the keys for reliable lifetime extrapolation. Superlattice-based buffers may be used to improve vertical reliability, as highlighted in [164], [165], and [166].

Next, we turn our focus to the application reliability needs for GaN FETs. Power conversion involves hard-switching transitions, which can be stressful on devices [167], [168]. For Si power FETs, a combination of technology and product-level tests is typically used to validate operational robustness, for example, unclamped inductive switching (UIS), hot carrier injection (HCI), and high-temperature operating life (HTOL). There are some differences between GaN and Si, which necessitate different testings. For example, UIS is not recommended for GaN, and HCI needs body contact, which is not available for GaN. As a result, the industry has worked together behind a common approach to assure the switching reliability of GaN power conversion devices, described in the Joint Electron Device Engineering Council (JEDEC) JEP180 guideline and summarized in Fig. 31.

Application-specific qualification is a challenging topic for any technology because of multiple topologies and use cases. The common approach for GaN was enabled by the use of the switching locus curve to represent the type of switching stress applied to the device [167] and, thereby, the failure mechanism exercised. This approach allows for the relevant stress to be applied and accelerated by a test-vehicle circuit and for the switching reliability validation to apply broadly. For example, a test-vehicle circuit that applies hard-switching stress can validate the hard-switching robustness of PSDs for the broad class of hard-switching applications. On-wafer testing has also been shown to generate relevant switching loci [169].

To assure switching reliability, adequate switching lifetime needs to be validated and application-use reliability demonstrated. The desired switching lifetime is validated by applying relevant accelerated switching stress, using a test-vehicle circuit. Batches of devices are run at several conditions, varying one stressor at a time and acceleration factors determined from the failure distribution plots. GaN has already demonstrated excellent switching lifetime for both hard and soft switching applications [170], [171], [172]. Application-use reliability is demonstrated by subjecting the FETs to system-level stress in a dynamic HTOL (DHTOL) test.

Robustness to occasional extreme events, such as power line surges, is also an important consideration for any power device. Power converters are typically running when such events occur, so the devices need to be robust to power line surges while switching. In the case of Si FETs, when a power line surge strikes, the FET avalanches or breaks down by impact ionization. Over the years, the industry has engineered Si FETs with avalanche capability, and this

property has become synonymous with power line surge protection. Present-day GaN FETs, however, do not have an avalanche rating. However, they have substantial overvoltage capability [173] and can switch through the surge.This capability has been shown for both hard and soft switchings [173], [174], [175]. The ability of GaN FETs to switch through surge will provide advantages for power-line connected converters.

B. Assessing and Controlling Reliability of SiC MOSFETs: Focus on Bias Temperature Instabilities

Implementing SiC as a PSD material allows to adopt several well-known device concepts and processing technologies from Si such as designs like vertical Schottky diodes or vertical power MOSFETs. Many fundamental procedures to verify the long-term stability of Si devices are essentially the same for SiC. Nevertheless, some specific SiC properties involve major adaptations to existing reliability tests that were developed for Si. Items that turned out to be relevant are the properties of the material itself with its specific defect structures, anisotropies, mechanical and thermal properties, the larger bandgap with its implications on the density and dynamics of interface traps in MOS-based devices, the up to ten times higher electrical fields inside the device and at the outside interfaces, and new operating modes where high-voltage operation and fast switching are combined. The listed items may all influence specific aspects in established qualification tests and require adapting models used to extrapolate test data and correlate it to real-world application conditions.

A very good example of a critical reliability issue that is well-known and extensively studied in Si MOSFET but turns out even more complex and challenging in SiC MOSFET is the bias temperature instability (BTI). BTI causes time-dependent variations of critical electrical device parameters, such as threshold voltage (V_{TH}), ON-resistance (R_{DSon}), and leakage current in the blocking mode (I_{DSoff}). In fact, BTI is a challenge for SiC MOSFETs in many different aspects. The internal mechanism governing BTI in SiC MOSTETS is the presence of broad distributions of slow electron and hotel traps, which can give rise to both device instability and the aging of the device [176].

Due to SiC-specific threshold voltage hysteresis effects caused by charging and discharging of (near)interface traps, one needs to be very careful when measuring V_{TH} of a SiC MOSFET since its value typically depends on the "biasing-history" of the device. To accomplish a reproducible V_{TH}measurement, which is a mandatory requirement for assessing BTI, it is essential to condition the device prior to the readout [177]. Conditioning means bringing the interface of the MOS device into a defined (near-equilibrium) charge state prior to the V_{TH} measurement. This can be done, for example, by applying a short (ms-range) positive gate pulse to the device using voltages around the recommended gate use voltage (c.f. Fig. 32). Other more complex conditioning procedures may also involve negative gate pulses. After conditioning, V_{TH} can be measured in a very accurate and reproducible manner, especially when keeping the time delay between the gate pulse and the V_{TH} readout constant. The easiest way to accomplish a fast and well-timed spot measurement of V_{TH} is to use a gated-diode measurement approach. Here, the gate and drain terminals of the device are shorted, the source terminal is grounded, and a threshold current, e.g., 1 mA, is forced. Being able to measure V_{TH} reproducibly, the next challenge for controlling and assessing BTI in SiC MOSFET is selecting appropriate stress conditions for drift monitoring and/or end-of-life drift evaluation.

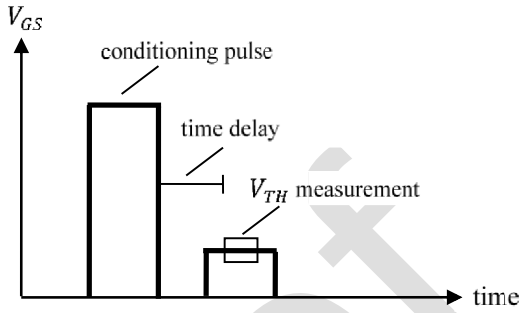

Fig. 32. Example of device conditioning for reproducible V_{TH} measurements in SiC MOSFETs. Prior to the V_{TH} measurement, a positive gate pulse is applied for several milliseconds to bring the MOS interface into a defined charge state. The time delay between the conditioning pulse and V_{TH} measurement needs to be constant.

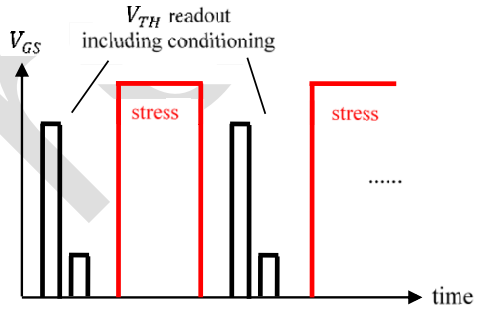

Fig. 33. Simplified sketch of a dc-BTI test using a positive gate stress voltage (PBTI). Stress periods are interrupted for intermediate V_{TH} readouts. Device conditioning is applied for initial, intermediate, and final V_{TH} readouts.

BTI monitoring is crucial for device manufacturers, for example, to control the V_{TH} stability of their device technologies over time or to check whether certain process changes affect parameter stability in general. For this purpose, a simple static dc-BTI stress test at elevated temperatures is typically done (c.f. Fig. 33). Device conditioning is applied for initial and intermediate and final V_{TH} readouts. Although this simple test is not very well reflecting operation conditions in real applications, it has the advantage of being easy to use and offers the potential of significant drift acceleration using stress biases and temperature beyond the specified data-sheet limits. For sure, one needs to be careful to keep stress biases and temperatures low enough in order not to trigger new degradation mechanisms that would not be observed in use conditions. Assessing dc-BTI using different stress biases and temperatures helps to build a degradation model and check for new mechanisms.

Besides monitoring and controlling BTI in production, device manufacturers also need to be able to assess worst

case end-of-life drifts for different mission profiles of various applications. This is needed to consider potentially critical parameter variations caused by BTI in specification limits and system designs. The most straightforward way of studying parameter drifts in real applications is by running long-term application tests, thereby doing intermediate read-outs, and finally extrapolating the drift toward end-of-life [178].

While this kind of testing is very intuitive and important since it has the obvious advantage of being closest to the application, it also comes with several practical disadvantages that typically disqualify such test setups for broad technology qualifications. In fact, an application test mimics only one very specific application condition that is likely not representative of all possible operating conditions in various customer designs. Also, real application tests do not provide much potential for stress acceleration via bias or temperature, and their electrical setups are typically very complex and cannot be scaled up easily. Therefore, one is typically aiming for simplified stress setups that trigger the same drift or failure phenomena that would occur in real applications. The target is to subject devices to such a test and assess worst case end-of-life parameter variations.

By using elevated gate biases and temperatures, it is possible to set up an accelerated stress test that provides, within a reasonable stress time (e.g., 1000 h), the data needed to predict/extrapolate worst case end-of-life drifts. Recent findings [179], [180], [181], however, suggest that a static dc-BTI test may not be best-suited to realistically predict drifts of SiC MOSFETs that are typically switched in the bipolar mode ($V_{GS,off} < 0$ V and $V_{GS,on} \gg V_{TH}$) at operation frequencies of up to 50 kHz and higher. Depending on the application conditions, a static BTI stress test may either significantly overestimate or underestimate real drifts in switching applications. Therefore, a different switching stress test, called the ac-BTI or gate switching stress (GSS) test, has been recently suggested [182]. In this setup, source and drain terminals are grounded, and the gates of devices are stressed at datasheet max-levels ($V_{GH,max}$, $V_{GL,min}$, and $T_{VJ,max}$) using pulsing frequencies of up to 500 kHz. Such high frequencies are used to achieve a considerable number of switching events within a reasonable stress time, e.g., 1000 h. This is essential since it was shown earlier [177], [178] that V_{TH} drift under ac stress conditions follows a power law that depends on the number of switching cycles (N_{Cycles}) given by $\Delta V_{TH} = A_0 \cdot (N_{Cycles})^n$. In this expression, A_0 represents a bias- and temperature-dependent prefactor and the power law exponent n as the main parameter describing the evolution of the time- and frequency-dependent V_{TH} drift.

Recent publications suggest that the frequency dependence of GSS is a consequence of the continuous charging and discharging of fast switching traps at the SiC/SiO_2 interface when pulsing the gate in the bipolar mode. During the fast transition phases of the gate pulse, some trapped charges cannot be emitted fast enough and, therefore, slightly enhance the oxide electric field during and shortly after the gate switching event [183], [184], [185]. An alternative model attributes the observed frequency acceleration to the recombination energy that is released in every single switching event when electrons and holes recombine at the MOS interface. The energy is assumed to be released mostly through vibrational excitations and can act as a "phonon kick" to break nearby bonds or to bring a defect to an excited vibrational state from which it can experience a reaction into a more permanently charged state [185].

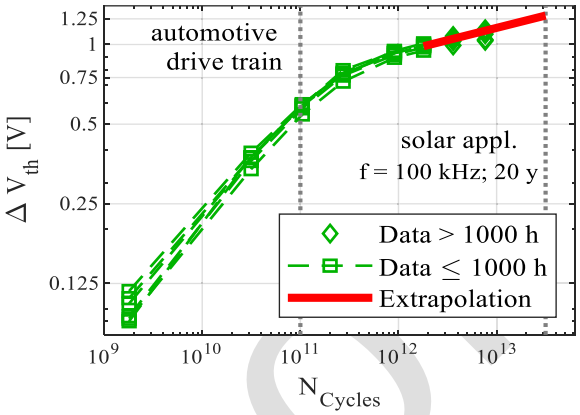

Fig. 34. End-of-life drift evaluation of 1200-V SiC trench MOSFET devices using a 1000-h ac-BTI test. The shown extrapolation is based on 1000-h data. Additional data points after 2000 and 4250 h of stress fit extrapolation. Typical numbers of switching cycles of solar inverter and automotive drive train applications are indicated by vertical lines.

Fig. 34 shows V_{TH} drifts of 1200-V SiC trench MOSFET devices stressed under ac-BTI conditions. Devices were stressed for 4250 h at their datasheet max-levels (+20 V, −10 V, and 150 °C) using a gate pulsing frequency of 500 kHz. In principle, one could use even higher stress frequencies of up to 2 MHz [186] to further accelerate ac-BTI. However, such high frequencies are much more challenging to handle experimentally due to parasitics and self-heating, and might result in undesirable effects, such as voltage overshoots or undershoots. The stress was interrupted multiple times to record the V_{TH} drift. The resulting drift curve shown in Fig. 34 can be used to estimate worst case end-of-life drifts for various applications. The total number of switching events of applications that run at relatively low frequencies, such as an automotive drive train inverter, is already covered within the 1000-h switching test at 500 kHz. Thus, its end-of-life drift can be simply determined by data interpolation. The expected end-of-life drift of other applications that run at much higher frequencies, e.g., solar applications, can be estimated by data extrapolation of a 1000-h ($1.8 \cdot 10^{12}$ cycles) test.

In this paragraph, we have reviewed the reliability and testing challenges of SiC-based power devices with a particular focus on bias temperature instabilities. Basic concepts of assessing and controlling BTI in SiC MOSFETs were discussed. It was highlighted that, even on an unstressed SiC MOSFET device, reproducible measurement of the threshold voltage is challenging but, at the same time, a fundamental requirement for the correct assessment of parameter drift over time. A stable V_{TH} measurement can be achieved by applying device conditioning. Static dc-BTI testing was suggested to be most useful for drift monitoring and comparative studies. For realistic end-of-life drift evaluation, real application tests or application-near-gate switching tests are the preferred

methods. Stressing at datasheet max-levels ensures worst case drift estimations for arbitrary mission profiles.

VII. Conclusion

In this article, PSD technologies that hold promise for power-electronic-based DERs are outlined. Even though Si-based PSDs will continue to play an important role in this commercial landscape, this article provides an overview of the next-generation WBG PSDs based primarily on SiC and GaN, and extends the discussion to the prospective UWBG PSDs. The abilities of the PSDs based on these new materials derive significant advantages, including, but not limited to, higher blocking voltage, lower forward drop, and enhanced thermal sustenance. This may lead to topological simplicity, reduced losses, reduced footprint, enhanced control bandwidth, and increased reliability of the associated power-electronic systems, to name a few.

Regarding SiC PSDs, although SiC JFETs show commercial promise, SiC MOSFETs are currently the most mature active-device technology, especially with in-roads into the medium voltage market. Although the cost of SiC FETs has been reduced, further reductions are deemed necessary for commercial cost competitiveness. GaN, on the other hand, is currently focused on the low-voltage and high-frequency market via the relatively more mature lateral FETs. To extend the benefits of GaN FETs for the medium voltage DER market, vertical versus lateral device architectures are being explored. Vertical GaN FETs have an advantage regarding voltage and power scaling while ensuring economy of scale, provided that the current technological gaps can be addressed shortly.

At the power-electronics system level, the WBG PSDs, notwithstanding their advantages, are posing some challenges. One of them relates to the enhanced conductive and radiative EMI noise, owing to the high slew rate of operation of these electrically triggered PSDs. In this regard, optically triggered PSDs (e.g., PCSS and bipolar optical devices) yield relatively higher immunity to such EMI noise. Such optically triggered devices do not suffer from floating ground problems as well. Hence, attaining higher system voltage via a series connection of such devices, given the paucity or absence of high-voltage PSDs, provides an interesting solution and an alternative to relatively complex multilevel power electronics. Optical devices, due to direct photogeneration, can also address applications with impulsive operating scenarios, including, but not limited to, pulse power, rapid fault isolation, directed energy, and so on.

Of course, packaging of the PSDs, given the newer materials issues associated with the SiC and GaN PSDs, enhanced slew rates of these devices, enhanced transient voltage and current stresses, need for reduced parasitic inductances, and thermal conductivities have posed newer research and development (R&D) challenges that need innovative solutions for high-performance energy conversion. Expectations of significantly higher power density also have the packaging experts exploring novel solutions, such as double-sided cooling, POL, and 3-D integration approaches, to name a few. Other additional challenges involving the enhancement of package functionalities (e.g., integration of passives, gate drivers, and signal processing) need new innovations beyond conventional packaging approaches. Optoelectronic integration of photonic PSDs appears to open new frontiers in packaging R&D regarding the economy of scale, quantum efficiency, and wave guiding, to name a few.

A final issue relates to the reliability of the PSDs. For WBG PSDs, the electric field is significantly higher than their Si counterparts both in the semiconductor material and the dielectrics. As such, careful PSD design and epitaxial optimization are needed for a long lifetime and reduced degradation. Equally important is the need for designing critical accelerated tests for these emerging PSDs for lifetime prediction. This can be used to incorporate reliability into the PSD design process for enhancing the mean time between failures. A key and relatively complex subsequent challenge lies in correlating PSD reliability to power electronics topologies, operating conditions, and switching mechanisms, among other factors. Correlations of such application and device reliabilities are expected to guide system and device engineers to recommend pathways (via device design, fabrication, and operation) for long-term PSD reliability via stressor mitigation in the emerging and perceivably stringent operating conditions for the WBG technology.

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After working in the commercial semiconductor industry, he joined the Sandia National Laboratories (SNL), Albuquerque, NM, USA, in 2016, to work on multiple types of semiconductor devices. He is currently a Distinguished Member of the Technical Staff, SNL, working on the development and maturation of gallium nitride (GaN)-based power electronic devices, GaAs-based optoelectronic devices, and heterogeneously integrated microsystems.

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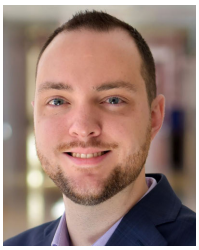
Jack Flicker (Senior Member, IEEE) received the B.S. degree in physics and chemistry from Penn State University, State College, PA, USA, and the Ph.D. degree in materials science and engineering from Georgia Tech, Atlanta, GA, USA, in 2011.

He joined the Sandia National Laboratories, Albuquerque, NM, USA, as a Post-Doctoral Appointee, focusing on power semiconductor reliability in photovoltaic applications. He is currently a Principal Member of the Technical Staff, Sandia National Laboratories. The nature of his work spans multiple TRL levels and incorporates everything from basic analysis to optimization and simulation to experiment and field deployment. His research interests include all aspects of power electronics and power conversion systems that enable improvements in power system operation, from the incorporation of new materials and devices in power conversion systems to utilizing new topologies and controls at the system level and touching all areas of the power electronics value chain ranging from usage of new devices (wide and ultrawide bandgap semiconductors) to new topologies, and controls to the evaluation of system-level behavior.



Andrew T. Binder received the B.S. degree from the University of Arkansas, Fayetteville, AR, USA, in 2013, and the Ph.D. degree from the University of Central Florida, Orlando, FL, USA, in 2019.

He is currently a Senior Member of Technical Staff, Sandia National Laboratories, Albuquerque, NM, USA. At Sandia, he leads a multidisciplinary team developing vertical gallium nitride (vGaN) junction barrier Schottky (JBS) and MOSFET devices and SiC BiDFETs. Under his leadership, this team has successfully demonstrated a new process for vGaN trench MOSFETs at Sandia, an accomplishment that was selected to be featured in the 2021 U.S. DRIVE Highlight by the DOE. In addition to microfabrication, his research background includes a focus on the physics and modeling of breakdown for wide bandgap power devices. His research is focused on the development of vGaN power devices.

Srabanti Chowdhury (Senior Member, IEEE) is currently the Willard and Inez Kerr Bell Faculty Scholar Associate Professor of electrical engineering (EE) with Stanford University, Stanford, CA, USA, and of materials science and engineering (by courtesy). She is also a Senior Fellow with the Precourt Institute of Energy, Stanford University. Her research focuses on wide bandgap (WBG) and ultrawide bandgap (UWBG) materials and device engineering for energy-efficient and compact system architecture for power electronics and RF applications.

Dr. Chowdhury serves on three IEEE conference committees that include the Technical Program Committee of the IEEE VLSI Symposium, IEEE IRPS, and the Executive Committee of the IEEE International Electron Devices Meeting (IEDM). She has served as an Editor for IEEE TRANSACTIONS ON ELECTRON DEVICES from 2019 to 2022. She also serves as an Editor for IEEE ELECTRON DEVICE LETTERS. She also serves on the EDS Compound Semiconductor Devices & Circuits Committee.

Victor Veliadis (Fellow, IEEE) received the Ph.D. degree in electrical engineering from Johns Hopkins University, Baltimore, MD, USA, in 1995.

Prior to entering academia and taking an executive position at PowerAmerica, Raleigh, NC, USA, in 2016, he spent 21 years in the semiconductor industry where his work included the design, fabrication, and testing of SiC devices, gallium nitride (GaN) devices for military radar amplifiers, and financial and operations management of a commercial semiconductor fab. He is currently the Executive Director and the CTO of PowerAmerica, a member-driven manufacturing consortium of industry, universities, and national labs accelerating the commercialization of energy-efficient SiC and GaN power semiconductor technologies. At PowerAmerica, he has managed a budget of $150 million that he strategically allocated to over 200 industrial and university projects to catalyze SiC/GaN semiconductor and power electronics manufacturing, workforce development, and job creation. His PowerAmerica educational activities have trained 420 full-time students in collaborative industry/university wide bandgap (WBG) projects and engaged over 4600 attendees in tutorials, short courses, and webinars. He is currently a Professor of electrical and computer engineering (ECE) with North Carolina State University (NCSU), Raleigh. He has 27 issued U.S. patents, six book chapters, and over 150 peer-reviewed publications to his credit.

Dr. Veliadis is an EDS Distinguished Lecturer.

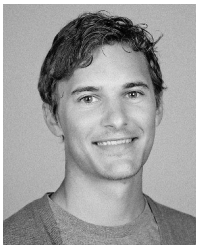
Fang Luo (Senior Member, IEEE) was an Assistant Professor with the Electrical Engineering Department, University of Arkansas, Fayetteville, AR, USA, from 2017 to 2020, and a Research Assistant Professor with The Ohio State University, Columbus, OH, USA, from 2014 to 2017. He is currently an Empire Innovation Associate Professor and the Director of Spellman High Voltage Power Electronics Laboratory, Stony Brook University, Stony Brook, NY, USA. He holds two U.S. patents and has authored/coauthored more than 50 journal articles, 100 peer-reviewed conference papers, and one book. His research interests include high-power-density converter design, high-density electromagnetic interference (EMI) filter design and integration, and power module packaging/integration for wide bandgap devices.

Dr. Luo was a recipient of the NSF CAREER Award. He is an Associate Editor of IEEE TRANSACTIONS ON POWER ELECTRONICS and *International Transactions*.

Sameh Khalil received the Ph.D. degree from the University of Toronto, Toronto, ON, Canada, for his research work on lateral super junction LDMOSTs where he pioneered how to terminate the super junction pillars in such 3-D structures and implemented the first experimental lateral super junction devices.

He was with imec, Leuven, Belgium, International Rectifier (now Infineon Technologies), El Segundo, CA, USA, and HRL Laboratories. He has been with Infineon Technologies since 2015. He is currently a Senior Principal Engineer with Infineon Technologies Americas Corporation. He heads a global gallium nitride (GaN) design-for-reliability team. He gave many presentations, participated in invited talks and panels, and moderated workshops at international conferences.

Dr. Khalil has served on the Technical Program Committee at IRPS, ISPSD, and WiPDA. He was the General Chair of WiPDA 2021. He is also the Co-Chair of the JC701.1 Sub-Committee of the JEDEC's Task Group concerned with Standards of GaN Power Conversion Semiconductor Reliability and Qualification Procedures.



Thomas Aichinger received the Ph.D. degree in electrical engineering from the Vienna University of Technology, Vienna, Austria, in 2010.

From 2011 to 2012, he was a Post-Doctoral Researcher with Penn State University, State College, PA, USA. Since 2012, he has been with the SiC MOSFET Technology Development Team, Infineon Technologies, El Segundo, CA, USA. He has contributed to more than 80 scientific publications, including journal articles, conference papers, and book chapters.

Dr. Aichinger has been serving on the Technical Committee of IRPS and WiPDa. He is currently serving as the Task Group Co-Chair within the JEDEC Sub-Committee JC.70.2 focusing on Standards for SiC Power Electronic Conversion Semiconductor Reliability & Qualification Procedures.

Sandeep R. Bahl (Senior Member, IEEE) received the Ph.D. degree from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 1993.

He worked at HP/Agilent. He is currently a Distinguished Member of the Technical Staff, Texas Instruments (TI), Dallas, TX, USA, responsible for the reliability of TI gallium nitride (GaN) parts. He has hands-on experience in many aspects of technology development, including coinventing TI's direct-drive GaN architecture, creating application reliability methodology for GaN, and cofounding TI's GaN product line. He played a key role in the GaN industry standardization effort, which has led to the formation of the JEDEC JC70 Committee and the increasing market adoption of GaN.

Dr. Bahl serves as the Co-Chair of the JC70 GaN Reliability Task Group and led the first JEDEC GaN Reliability Guideline, JEP180.

Matteo Meneghini (Senior Member, IEEE) received the Ph.D. degree from the University of Padua, Padua, Italy, with a focus on the optimization of gallium nitride (GaN)-based LED and laser structures.

He is currently a Full Professor with the Department of Information Engineering, University of Padua. His main interests are the characterization, reliability, and modeling of compound semiconductor devices [LEDs, laser diodes, and high electron mobility transistors (HEMTs)], and optoelectronic components, including solar cells. Within these activities, he has published more than 400 journal articles and conference proceedings papers.

Alain B. Charles received the Ph.D. degree from the Institut National des Sciences Appliquées de Toulouse, Toulouse, France, in 1989, for his work on optical lithography.

Through his international career, he pioneered most of the key changes in the semiconductor industry, such as subwavelength pattern printing (Motorola ATC, Mesa, AZ, USA) to 300-mm capability development (Semiconductor300, Dresden, Germany), to foundry enablement (Chartered Semiconductors, Singapore) to power technologies (International Rectifier, Newport, U.K.), and later the introduction of wide bandgap semiconductors (Infineon Technologies, El Segundo, CA, USA). Since 2021, he has been running his own consulting company (ABCsWorld Consulting, Redondo Beach, CA, USA) on power semiconductors and is serving on the Board of Cambridge GaN Devices.