A Differential-Mode Isolated AC/AC Converter

Shantanu Gupta, *Graduate Student Member, IEEE*, and Sudip K. Mazumder, *Fellow, IEEE*

***Abstract*—In this article, an isolated single-stage direct power conversion (DPC) type ac/ac converter is outlined. The ac/ac converter is based on differential-mode (DM) architecture where two dc/dc converter modules are connected differentially. The pulsewidth modulation active-clamp-Ćuk converter is used for the DM modules as the converter allows zero-voltage-switching turn-ON capability on all switches over a wide operating range, enabling the construction of a high-efficiency ac/ac converter. This article details the modulation scheme and the operational analysis of the new DM ac/ac converter (DMAC). In DPC-type ac/ac converters, the converter is required to propagate the input port electric signal to the output port with minimal internal energy storage. The capacitative component internal to the converter undergoes the ac voltage transition, which appears as a capacitive load resulting in reactive power injection in the input port. Hence, a thorough design process of the ac/ac converter is provided to minimize the internal capacitance of the converter. A 1-kW hardware prototype is also built using the underscored design process to validate and demonstrate the operation of the ac/ac converter.**

***Index Terms*—AC–ac converter, differential mode, modulation, solid-state transformer (SST), zero-voltage switching (ZVS).**

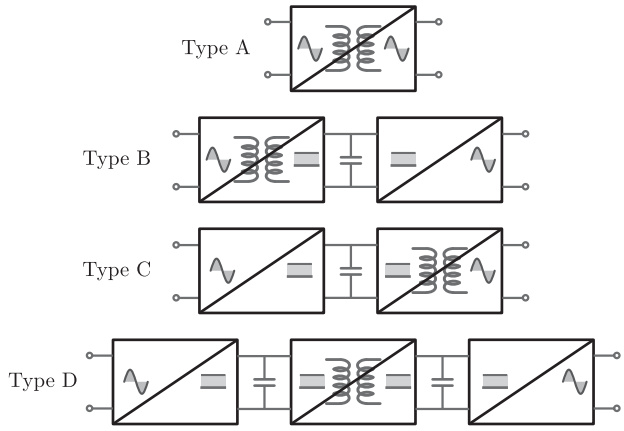

Fig. 1. Topology classification of isolated AC/AC converters [1].

I. Introduction

RESEARCH focus on isolated ac/ac converter has gain traction due to its potential in replacing bulky and monolithic conventional low frequency transformers (LFTs). LFTs are used to step-up or step-down the voltage level and provide galvanic isolation for various levels of electric power transmission. In addition, LFTs have isolation applications to enhance electrical system safety in household and medical equipment. Isolated ac/ac converters used in place of LFTs are referred as solid-state transformer (SST) [1]. A SST offers economical, modular, and denser solution compared to LFT. The modular structure of the SST can play significant role in distributed energy resource (DER) like offshore substation [2], PV based microgrids integration [3] in the power grid and traction systems [4] due to manufacturing and transportation flexibility. However, the efficiency offered by LFTs is quite high ($> 97\%$ [1]). Hence, development of high efficiency isolated ac/ac converter would bolster the adaptation of SSTs in the power grid systems. The ac/ac converter also finds its application as dynamic voltage regulators (DVR) to compensate for voltage sags and swells caused by sudden change in large loads [5], [6], [7]. DVR are generally deployed for sensitive loads such data centers and hospitals [8].

In [1], the isolated ac/ac converter is classified in four types as also shown in Fig. 1. Type A is a DPC type ac/ac converter configuration that is cheaper, simpler, and offers higher efficiency [9]. Typically, in Type A ac/ac converter the power flow is directly propagated between the input and output port without much conditioning or frequency decoupling. Type B and Type C are two-stage ac/ac converter solutions with one stage as an ac/dc converter and the other as a dc/ac converter stage. Besides the required galvanic isolation, the presence of a dc-link in the two-stage ac/ac converter allows the converter to improve the power quality by using the dc-link for filtering and power decoupling. However, the control of a two-stage converter is more complex, and the implementation requires bigger passive components. The converter also suffers from lower efficiency due to compounded loss of the two stages. Type D ac/ac converter configuration consists of three conversion stages converter [10], [11], ac/dc converter, dc/dc converter, and dc/ac. This configuration is most widely used as it allows more operational flexibility due to decoupling offered by the two dc-links [1]. However, more stage count results in lower efficiency,

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Shantanu Gupta is with the Department of Electrical and Computer Engineering, University of Illinois at Chicago, Chicago, IL 60607 USA (e-mail: sgupt57@uic.edu).

Sudip K. Mazumder is with the NextWatt LLC, Hoffman Estates, IL 60607-7101 USA, and also with the University of Illinois at Chicago, Chicago, IL 60607-7101 USA (e-mail: sudipkumarmazumder@gmail.com).

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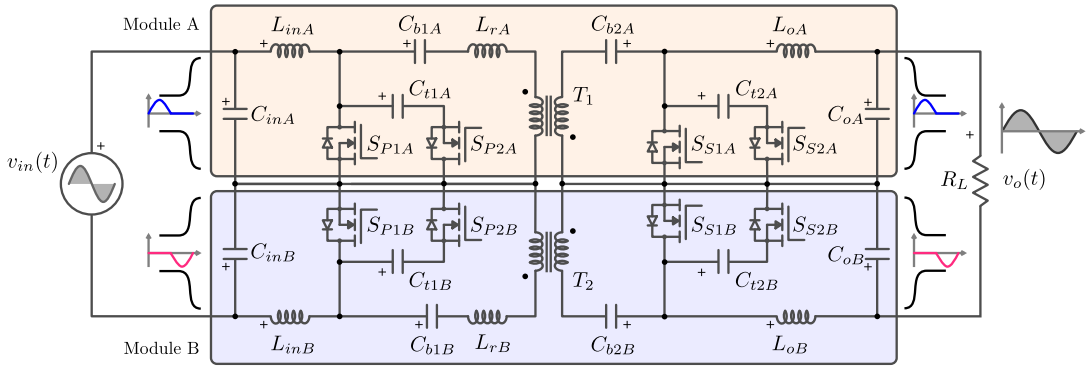

Fig. 2. Topology of the DMAC. The components of modules A and B are annotated with the module name (A or B) in the subscript. In this article, when referencing the components of both modules, the module name is dropped from the subscript.

complex control structure, higher sensor counts, and bulky passive components than the other configuration of isolated ac/ac converters.

The Type A configured ac/ac converter is generally realized using a folding and an unfolding stage to interface the dc/dc converter [1], [12], [13], [14]. Each of these stages requires a minimum of four extra active switches, significantly increasing the device count. For the isolated dc/dc converter stage, soft-switching capable topologies like dual-active bridge (DAB) converter and *LLC* converter are widely used in isolated ac/ac converter due to their soft-switching capabilities resulting in higher efficiencies. However, since DAB is a voltage-source converter, the input and the output currents of the converter are discontinuous and require bulkier filter capacitors. Complex converter modulation [15], [16] is also required to maintain soft-switching over a wide load condition.

In a DM converter, two dc–dc converter modules are connected differentially to enable 4 quadrant (bipolar voltage and bidirectional current) operation [17]. The absence of folding and unfolding stages in the DM converter reduces device count and the associated loss. In ac/dc or dc/ac applications [18], [19], [20], the modules are connected in series on the ac side to enable 4 quadrant operation while on the dc-side, the modules are connected in parallel. In [21], a nonisolated buck–boost module-based DM (NIBB-DM) ac/ac converter is introduced. Both the modules in the DM converter are always active (emulating continuous modulation scheme) resulting in additional losses due to power-circulation and switching losses.

In contrast, the proposed isolated DMAC, shown in Fig. 2, is modulated under discontinuous modulation scheme (DMS). DMS was introduced for differential mode inverter (DMI) in [19] where hard-switched Ćuk converter was used for the modules. The modulation scheme in [19] used duty cycle of the switches as the control parameter for the inverter operation. The component design of the dc/dc modules is straightforward due to presence of constant voltage at the input port. In this article, DMS is extended for DM ac/ac converter for isolated pulsewidth modulation (PWM) active-clamp (PAC) Ćuk based dc/dc converter modules [22], [23], [24]. The active-clamp circuit in PAC-Ćuk dc/dc modules of the DMAC enables ZVS turn-ON capability on all its switches, thereby significantly reducing the switching losses with only four active switches. The PAC-Ćuk converter also allows continuous-input and continuous-output currents resulting in reduced input and output filter capacitors.

In [22], operational principle of PAC-Ćuk topology for dc/dc converter application is discussed. The operational analysis underscored in the article assumes linear modes of operation of the converter due to sizable internal capacitors for dc/dc converter application. However, in Type A ac/ac converter operation, the 50/60 Hz ac voltage in the input port is required to be reproduced at the output port without any phase delay. Hence, contrary to dc/dc [22], ac/dc [25], or dc/ac [19] converter where the converter absorbs the input and output perturbation, the Type A ac/ac converter and its modules are designed to permeate the 50/60 Hz signal by reducing the filtering caused by the capacitor internal to the topology. Reduction of internal capacitor results in non-linear mode of operations and in turn deviation from the linear model for PAC-Ćuk dc/dc converter. In addition, as the internal capacitor of the dc/dc modules undergoes sinusoidal voltage variation resulting in reactive power injection in the input port, a large cumulative internal capacitor would deteriorates the power factor at the input side [14].

In this article, operational analysis and modulation of the DMAC is provided. The analysis captures the nonlinear modes of the PAC-Ćuk converter catering to the ac/ac converter application. Leveraging the analysis, design process of the DMAC is also presented with the objective of minimizing the cumulative internal capacitors while ensuring ZVS turn-ON of all the switches. A 1-kW hardware prototype of the DMAC is also built using the design guidelines to validate the working the DMAC.

In this article, the modulation technique dictating the operation of the modules in DM architecture is provided in Section II. A detailed analysis of the mode of operation of the PAC-Ćuk module is provided in Section III. In Section IV, the design process of the DMAC is discussed in detail to minimize internal capacitance. In Section V, experimental validation of the DMAC converter is provided. A comparison of the proposed ac/ac converter with other recent publications is also provided in Section V. Finally, Section VI concludes this article

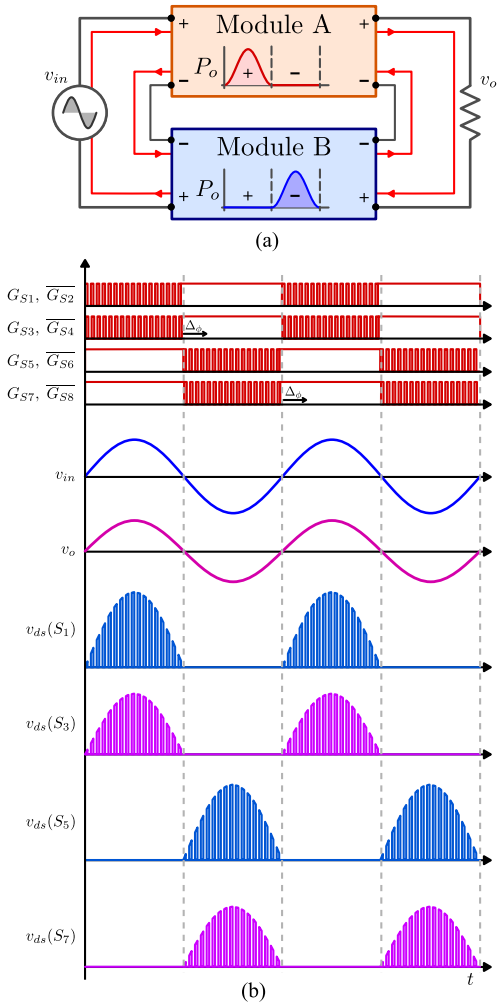

Fig. 3. (a) Power flow depiction. (b) Switching diagram of DMS operated DMAC.

II. Architectural Operation of the DMAC

The proposed single-stage DM ac/ac converter consists of two identical isolated PAC-Ćuk dc/dc modules (Module A and Module B) connected differentially as shown in Fig. 2. A PAC-Ćuk dc/dc module contains two auxiliary capacitors C_{t1} and C_{t2}, two blocking capacitor C_{b1} and C_{b2}, series inductor L_r, isolation transformer and switches $S_1 - S_4$ for module A and $S_5 - S_8$ for Module B. The two modules are operated similar to DMS introduced in [18] and [19] for dc/ac and ac/dc operation.

The DMS devised for dc/ac converter in [19] dictates that one of the two differentially connected modules stays inactive while the other module is responsible for transferring the required power depending on the ac side polarity. A similar principle is employed for the proposed DMAC. In the DMAC, as both the modules are connected in differential series configuration, the module should maintain current continuity even when one of the modules is not transferring any power, as shown in Fig. 3(a). In the DMS modulation for ac/ac converter, the module modulation should ensure that the inactive module is conducting from both input and output side while the active module is transferring the power to maintain the current continuity. As the output side voltage follows the input voltage v_{in} in Type A ac/ac converter, the active module is dictated by the polarity of v_{in}. The switches of the active module are operated normally at switching frequency while switches in the inactive module are at a fixed state such that the inactive module is maintaining current continuity.

During the positive line cycle ($v_{\text{in}} > 0$), Module B is inactive as S_5 and S_7 are kept turned ON for the positive line cycle and do not take part in power transfer, as shown in Fig. 3(b). As S_6 and S_8 are always complementary to S_5 and S_7, respectively, they are kept turned OFF. While $S_1 - S_4$ of Module A are operated with a 50% duty cycle at switching frequency f_{sw} with a phase-shift ratio, Δ_ϕ defined as the ratio of the time delay of turn on of S_3 with respect to S_1 to switching period T_s, to control the power flow. During the negative line cycle ($v_{\text{in}} < 0$), S_1 and S_3 are kept turned ON for the negative line cycle. S_2 and S_4 are always complementary to S_1 and S_3, respectively, are turned OFF. While $S_5 - S_8$ of Module B are operated at 50% duty cycle at switching frequency f_{sw} with a phase-shift ratio Δ_ϕ.

III. Module Operation of the DMAC

In the previous section, the modulation scheme of the two modules is discussed. In this section, the operation principle of the dc/dc modules for the positive input voltage over a switching cycle is described, as shown in Fig. 4. In the figure, the red loop showcases the line frequency current flow and the current continuity formed by the inactive module. Analysis for the negative line cycle is similar to the positive line cycle and, hence, is not described in this article. The results obtained for the positive cycle will be directly applicable to the negative cycle.

The PAC-Ćuk modules designed for the ac/ac converter has significantly smaller capacitors than the PAC-Ćuk dc/dc converter alluded to earlier. The size of the equivalent blocking capacitor, C_b is small enough that the ripple across the capacitor cannot be ignored resulting in nonlinear series inductor current in contrast to the dc/dc converter designed in [22]. Accounting the nonlinearity is important in the analysis as it influences the power transfer equation and alters the maximum power transfer capability of the designed converter. In addition, the ZVS turn-ON region of the switches are also highly dependent upon the series inductor current.

The operation of the DMAC with Module A switching and Module B bypassed is divided into 4 modes of operation in the switching period T_s, as shown in Fig. 4. The waveform associated with the modes is illustrated in Fig. 5. In this article, the small-case variable represents a time-varying variable whereas a capital-case variable is used for the time-invariant variable and parameter. The following assumptions are made to illustrate the operation and analysis of the proposed converter.

1) All the switches ($S_1 - S_8$), capacitors, and magnetic components are assumed ideal. The switches associated with the active module are operated at a 50% duty cycle. The

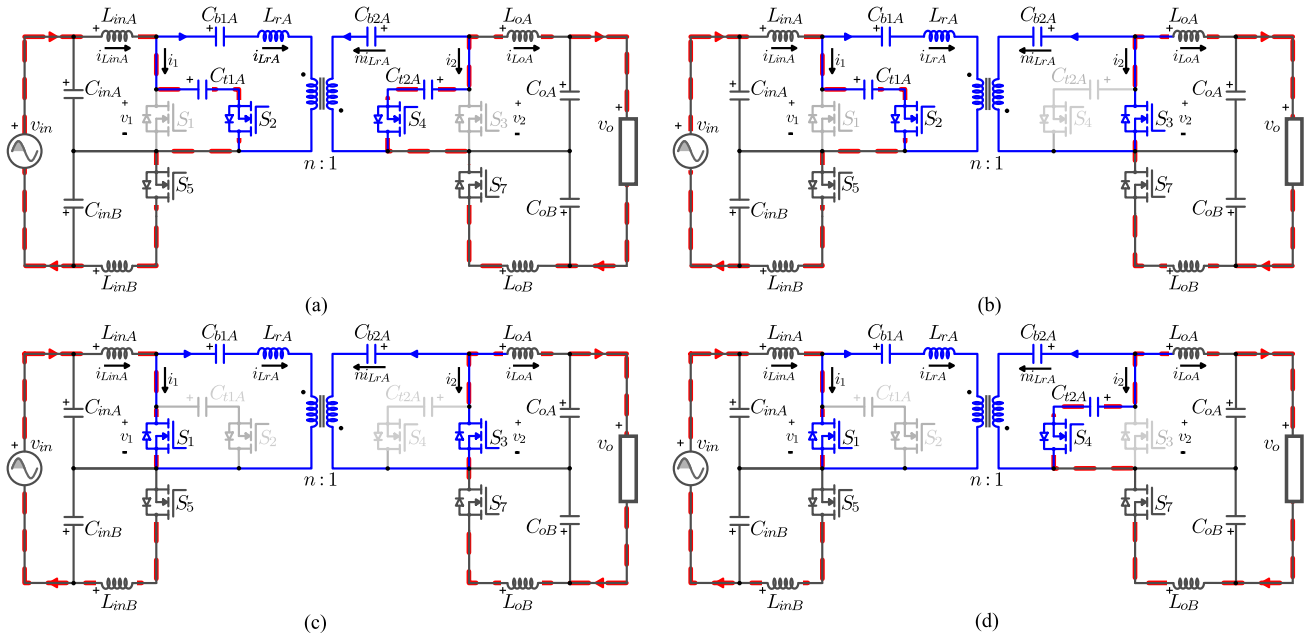

Fig. 4. Modes of DMS operated DM PAC (DM-PAC)-Ćuk AC/AC converter for positive input voltage. The blue loop highlights the high-frequency energy transfer link whereas the red loop highlights the flow of low frequency current.

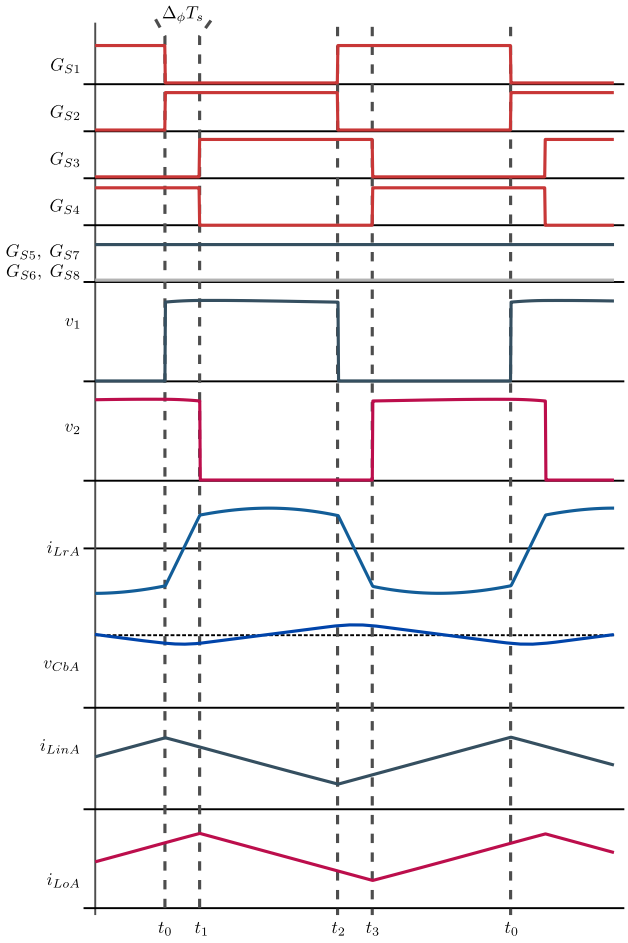

Fig. 5. Waveform of DM-PAC-Ćuk based AC/AC converter over a switching cycle.

output capacitance of the switches is assumed insignificant. Hence, the turn-OFF transition of the switches is ignored in the mode analysis as the duration of the switching transition is small compared to the duration of the modes [26].

2) The transformer turn ratio of $n:1$ is considered. The magnetizing inductance of the transformer is considered much higher than the series inductance. Hence, the two blocking capacitors C_{b1A} and C_{b2A} can be lumped into an equivalent blocking capacitor $C_{bA} = C_{b1A} \parallel \frac{C_{b2A}}{n^2}$ referred to the input side of the transformer.
3) The switching voltage ripple on the auxiliary capacitors is maintained small enough that it can be assumed constant over a switching cycle in the analysis.

In PAC-Ćuk dc/dc converter module, the power is transferred from the input port to the output port using the voltage applied across the high-frequency (HF) link formed by L_{rA}, C_{b1A}, and C_{b2A}, as shown in Fig. 4 by the blue highlight loop. The voltage across the HF-link is given by the difference between v_1 which is the voltage across S_1 and v_2, which is the voltage across S_3. The current flowing into S_1 and S_2 is denoted by i_1 while the current flowing into S_3 and S_4 is denoted by i_2, as shown in Fig. 4. Current i_1 and i_2 is given by

$$i_1 = i_{LinA} - i_{LrA} \tag{1}$$

$$i_2 = -i_{LoA} - n i_{LrA} \tag{2}$$

where i_{LinA} and i_{LoA} are the input and output inductor current while i_{LrA} is the series inductor current of Module A. As the duty cycle of the switches is fixed at 50%, the average voltage across the capacitor is found using the voltage-second balance

on $L_{inA},\ L_{oA}$, and L_{LrA}

$$v_{Ct1A} = 2v_{\text{in}} \tag{3a}$$

$$v_{Ct2A} = 2v_o \tag{3b}$$

$$\langle v_{CbA} \rangle = \langle v_{Cb1A} \rangle + n \langle v_{Cb2A} \rangle = v_{\text{in}} + nv_o \tag{3c}$$

where $\langle \blacksquare \rangle$ is the operator used to denote the average value over a switching period, T_s and v_{CbA} is the equivalent voltage across the capacitors when the circuit is referred to the input side. The circuit is assumed to be in a state where S_1 and S_4 are already turned-ON.

Mode 1 [t_0, t_1]: At $t_0,\ S_1$ is turned-OFF diverting i_1 from S_1 to S_2 resulting in internal diode conduction. The gate of S_2 should be exerted before the polarity reversal of i_1 to achieve the ZVS turn-ON of the switch. The voltage applied across $C_{bA},\ (\ C_{bA} = C_{b1A}\ \|\ \frac{C_{b2A}}{n^2})$, and L_{rA} is positive and is the sum of v_{Ct1A} and nv_{Ct2A}. Using the KVL and KCL in the HF-link loop, the differential equation of i_{LrA} and v_{CbA} is given by

$$L_{rA}\frac{di_{LrA}}{dt} = 2\left(v_{\text{in}} + nv_o\right) - v_{CbA} \tag{4}$$

$$C_{CbA}\frac{dv_{CbA}}{dt} = i_{LrA}. \tag{5}$$

Solution of i_{LrA} and v_{CbA} for this mode is obtained as follows:

$$\begin{aligned} v_{CbA} = {} & 2\left(v_{\text{in}} + nv_o\right) - \left(2\left(v_{\text{in}} + nv_o\right)\right. \\ & \left. - v_{CbA}\left(t_0\right)\right)\cos\omega_r\left(t - t_0\right) \\ & + Z_r i_{LrA}\left(t_0\right)\sin\omega_r\left(t - t_0\right) \end{aligned} \tag{6}$$

$$\begin{aligned} i_{LrA} = {} & \frac{\left(2\left(v_{\text{in}} + nv_o\right) - v_{CbA}\left(t_0\right)\right)}{Z_r}\sin\omega_r\left(t - t_0\right) \\ & + i_{LrA}\left(t_0\right)\cos\omega_r\left(t - t_0\right) \end{aligned} \tag{7}$$

where Z_r is the resonance impedance and ω_r is the resonance frequency given by

$$Z_r = \sqrt{\frac{L_{rA}}{C_{bA}}}, \omega_r = \frac{1}{\sqrt{L_{rA}C_{bA}}}. \tag{8}$$

Mode 2 [t_1, t_2]: At $t_1,\ S_4$ is turned off diverting i_2 to S_3 resulting in internal diode conduction. The gate of S_3 is applied before the polarity reversal of i_2 to achieve the ZVS turn-ON of the switch. During this mode, the voltage applied across C_{bA} and L_{rA} is v_{Ct1A}. The differential equation of i_{LrA} and v_{CbA} is given by

$$L_{rA}\frac{di_{LrA}}{dt} = 2v_{\text{in}} - v_{CbA} \tag{9}$$

$$C_{CbA}\frac{dv_{CbA}}{dt} = i_{LrA}. \tag{10}$$

Solution of i_{LrA} and v_{CbA} for this mode is obtained as follows:

$$\begin{aligned} v_{CbA} = {} & 2v_{\text{in}} - \left(2v_{\text{in}} - v_{CbA}\left(t_1\right)\right)\cos\omega_r\left(t - t_1\right) \\ & + Z_r i_{LrA}\left(t_1\right)\sin\omega_r\left(t - t_1\right) \end{aligned} \tag{11}$$

$$\begin{aligned} i_{LrA} = {} & \frac{\left(2v_{in} - v_{CbA}\left(t_1\right)\right)}{Z_r}\sin\omega_r\left(t - t_1\right) \\ & + i_{LrA}\left(t_1\right)\cos\omega_r\left(t - t_1\right). \end{aligned} \tag{12}$$

Mode 3 [t_2, t_3]: At $t_2,\ S_2$ is turned off diverting i_1 to S_1 resulting in internal diode conduction. The gate of S_1 is applied before the polarity reversal of i_1 to achieve ZVS turn ON of the switch. During this mode, the voltage applied across C_{bA} and L_{rA} is zero. The differential equation of i_{LrA} and v_{CbA} is given by

$$L_{rA}\frac{di_{LrA}}{dt} = -v_{CbA} \tag{13}$$

$$C_{CbA}\frac{dv_{CbA}}{dt} = i_{LrA}. \tag{14}$$

Solution of i_{LrA} and v_{CbA} for this mode is obtained as follows:

$$v_{CbA} = v_{CbA}\left(t_2\right)\cos\omega_r\left(t - t_2\right) + Z_r i_{LrA}\left(t_2\right)\sin\omega_r\left(t - t_2\right) \tag{15}$$

$$i_{LrA} = -\frac{v_{CbA}\left(t_2\right)}{Z_r}\sin\omega_r\left(t - t_2\right) + i_{LrA}\left(t_2\right)\cos\omega_r\left(t - t_2\right). \tag{16}$$

Mode 4 [$t_3, T_s + t_0$]: At $t_3,\ S_3$ is turned off diverting the current, i_2 to S_4 resulting in internal diode conduction. The gate of S_4 is applied before the polarity reversal of i_2 to achieve ZVS turn ON of the switch. During this mode, the voltage applied across C_{bA} and L_{rA} is. The differential equation of i_{LrA} and v_{CbA} is given by

$$L_{rA}\frac{di_{LrA}}{dt} = 2nv_o - v_{CbA} \tag{17}$$

$$C_{CbA}\frac{dv_{CbA}}{dt} = i_{LrA}. \tag{18}$$

Solution of i_{LrA} and v_{CbA} for this mode is obtained as follows:

$$\begin{aligned} v_{CbA} = {} & 2nv_o - \left(2nv_o - v_{CbA}\left(t_3\right)\right)\cos\omega_r\left(t - t_3\right) \\ & + Z_r i_{LrA}\left(t_3\right)\sin\omega_r\left(t - t_3\right) \end{aligned} \tag{19}$$

$$\begin{aligned} i_{LrA} = {} & \frac{\left(2nv_o - v_{CbA}\left(t_3\right)\right)}{Z_r}\sin\omega_r\left(t - t_3\right) \\ & + i_{LrA}\left(t_3\right)\cos\omega_r\left(t - t_3\right). \end{aligned} \tag{20}$$

The solution of the modes requires initial conditions of i_{LrA} and v_{CbA} for all the modes. The closed-form solution of these nonlinear modes is complex, hence, additional simplification is required. As the duty cycle of the switches is 50%, leveraging the symmetricity of i_{LrA} and v_{CbA} following relation of the initial conditions can be obtained

$$i_{LrA}\left(t_0\right) = -i_{LrA}\left(t_2\right) \tag{21a}$$

$$i_{LrA}\left(t_1\right) = -i_{LrA}\left(t_3\right) \tag{21b}$$

$$v_{CbA}\left(t_0\right) = -v_{CbA}\left(t_2\right) + 2\left(v_{in} + nv_o\right) \tag{21c}$$

$$v_{CbA}\left(t_1\right) = -v_{CbA}\left(t_3\right) + 2\left(v_{in} + nv_o\right). \tag{21d}$$

Using solution of i_{LrA} and v_{CbA} for the modes and relation given by (21), $i_{LrA}(t_0)$ and $i_{LrA}(t_1)$ are found as

$$i_{LrA}(t_0) = -\frac{v_{in}\sin\left(\frac{T_s\omega_r}{4}\right) + nv_o\sin\left(\frac{T_s\omega_r}{4}(\Delta_\phi - 1)\right)}{Z_r\cos\left(\frac{T_s\omega_r}{4}\right)} \tag{22a}$$

$$i_{LrA}(t_1) = \frac{nv_o\sin\left(\frac{T_s\omega_r}{4}\right) + v_{\text{in}}\sin\left(\frac{T_s\omega_r}{4}\left(\Delta_\phi - \frac{1}{4}\right)\right)}{Z_r\cos\left(\frac{T_s\omega_r}{4}\right)}. \tag{22b}$$

As the output power contribution from the inactive module is zero, only the output power transfer from the active module is required to find the power dependency on Δ_ϕ. Hence, the total power transferred is equivalent to the power transferred into the capacitor C_{t2A} by i_{LrA} over a switching cycle. As i_{LrA} is flowing through C_{t2A} only in mode 1 and mode 4, the power relation is given by

$$p_o = \frac{1}{T_s}\int_0^{T_s} nv_2 i_{LrA}dt = \frac{1}{T_s}\int_{t_3}^{T_s+t_1} nv_2 i_{LrA}dt. \tag{23}$$

Substituting (3), (7), (20), and (21) into (23), a closed-form solution of instantaneous output power is obtained after simplification and given by

$$p_o = \frac{8nv_{\text{in}}v_o}{Z_r\omega_r T_s}\left(\frac{\sin\left(\Delta_\phi\frac{T_s\omega_r}{2}\right)\sin\left(\frac{T_s\omega_r}{2}(0.5-\Delta_\phi)\right)}{\cos\left(\frac{T_s\omega_r}{4}\right)}\right). \tag{24}$$

Equation (24) provides the output power as a function of the control parameter (Δ_ϕ) and design parameters (ω_z, Z_r, T_s) where ω_r and Z_r are depended upon C_{b1A}, C_{b2A}, and L_{rA}.

IV. Design Guidelines of Key Components for the DMAC

In this Type A ac/ac converter solution, the capacitors internal to the topology follow the input and output voltage profile resulting in a capacitive load seen at the input terminal of the converter. The capacitive current drawn by the converter is responsible for charging the internal capacitor and satisfy the relation given by (3). Capacitive loading results in reactive power injection into the input source and reduces the power factor for resistive load at the output of the DMAC. Lower reactive power injection reduces the circulating current and conduction loss. In this section, the process to design the DMAC for the required power range is discussed using the analysis from the previous section while ensuring ZVS turn-ON conditions on all the switches.

A 1 kW ac/ac converter is designed in this section to illustrate the design process. The specification used for the design is given in Table I. As both the dc/dc modules are identical, the design process in this section applies to both modules. Hence, the module subscript is dropped while addressing the components.

The transformer turn ratio, n is determined based on nominal input and output voltage as given by

$$n = \frac{V_{\text{in},nom}}{V_{o,nom}} \tag{25}$$

TABLE I
Required Specification of the DMAC

Parameter	Value
V_{in}	220 V_{rms}
V_o	220 V_{rms}
$P_{o,max}$	1 kW
$P_{o,min}$	250 W
f_s	40 kHz
t_{db}	400 ns

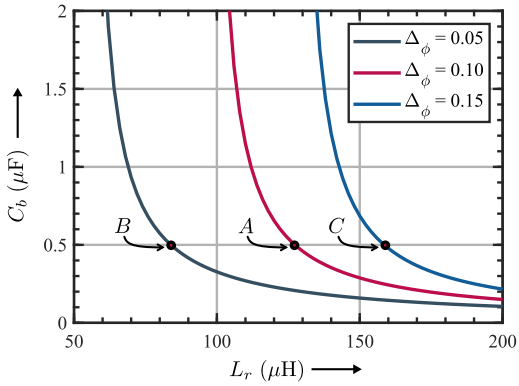

Fig. 6. L_r and C_b dependency on Δ_ϕ for $P_o = 1$ kW, $V_{in} = V_o = 220\ V_{\text{rms}}$, and $f_s = 40$ kHz.

where $V_{\text{in},nom}$ and $V_{o,nom}$ are the rms of nominal input and output voltages, respectively. With (25), the converter exerts unity gain under nominal voltage operation while the transformer supports the nominal voltage conversion. Equal nominal input and output voltages are chosen for the hardware prototype to minimize component variability with unity transformer turn ratio. The dead time t_{db} of 400 ns is used to prevent the shoot-through between the complimentary switch pairs.

Input and output inductor, L_{in} and L_o: The PAC-Ćuk converter allows continuous input and output current through L_{in} and L_o which reduces or eliminates the requirement of additional filters. The size of L_{in} and L_o are determined based on the required current ripple through the inductor as given by

$$L_{\text{in}} = \frac{V_{in}^2 T_s}{4rP_{o,\text{max}}}, L_o = \frac{V_o^2 T_s}{4rP_{o,\text{max}}} \tag{26}$$

where $r = \frac{\Delta I}{I}$ is the ripple current ratio [27]. For this converter, $r = 0.5$ is used to select L_{in} and L_o.

Series inductor L_r and blocking capacitor C_b: The high-frequency resonance link formed by the blocking capacitor and inductor is responsible for transferring power from the input to the output side. As discussed in Section III, the output power of the PAC-Ćuk converter depends on Δ_ϕ, L_r, and C_b. The resonance parameters, L_r and C_b should be designed such that the converter allow transfer of the desired minimum and maximum output power with the specification given in Table I.

Using (23), the rms output power transfer for resistive load is given by (27). By solving (27) for specification given by Table I, required L_r and C_b relation is obtained to deliver 1 kW output power for various Δ_ϕ, as shown in Fig. 6. The required capacitor

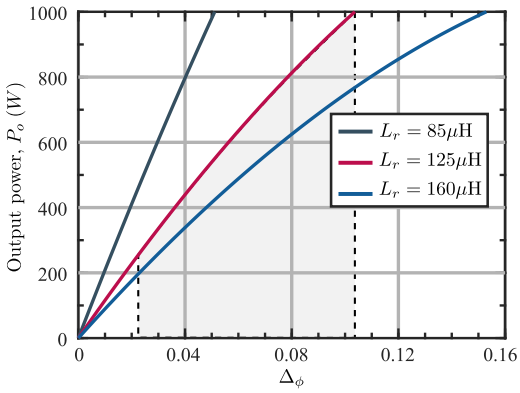

Fig. 7. Output power dependency on the phase-shift ratio for various L_r and $C_b = 0.5\ \mu$F.

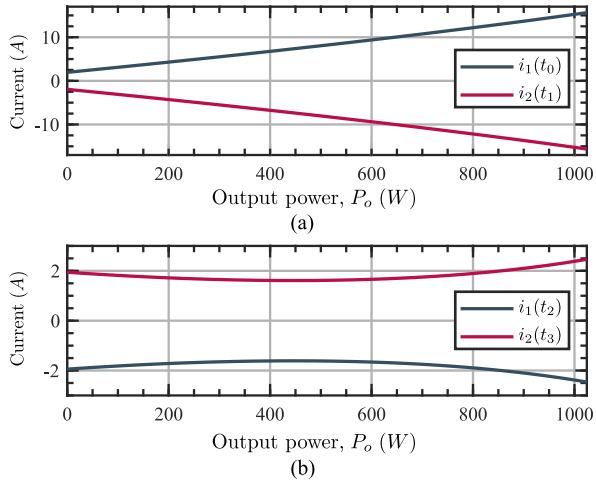

Fig. 8. (a) $i_1(t_0)$ and $i_2(t_1)$, and (b) $i_1(t_2)$ and $i_2(t_3)$ for $L_r = 125\ \mu$H and $C_b = 0.5\ \mu$F against output power with $V_{\text{in}} = V_o = 220\ V_{\text{rms}}$.

and series inductor have inverse relation for fixed operating point. A smaller capacitor requires a larger inductor for the same output power and Δ_ϕ. On the other hand, a smaller Δ_ϕ at the rated output power allows selection of smaller resonance link

$$P_o = \frac{8V_{\text{in}}V_o}{nZ_r\omega_r T_s}\left(\frac{\sin\left(\Delta_\phi\frac{T_s\omega_r}{2}\right)\sin\left(\frac{T_s\omega_r}{2}\left(0.5-\Delta_\phi\right)\right)}{\cos\left(\frac{T_s\omega_r}{4}\right)}\right). \tag{27}$$

In the ac/ac converter design, the capacitor needs to be minimized to limit the reactive power injection by the converter. From Fig. 6, $C_b = 0.5\ \mu$F allows a balanced solution for L_r. Reducing C_b further would require much higher L_r, which increases the core size and the conduction loss.

Fig. 7 shows the output power dependency on Δ_ϕ for different L_r (near point A, B, and C marked in Fig. 6). For $L_r = 85\ \mu$H, the inductor size is small, however, near low load operation the required phase-shift period, $\Delta_\phi T_s$ is smaller than the dead time duration. In a phase-shift based modulation, the minimum phase-shift is limited by the dead time and switching transient duration [28], [29], [30] as the converter modes are not clearly defined during the dead time. Hence, Point A ($L_r = 130\ \mu$F and $C_b = 0.5\ \mu$F) marked in Fig. 6 is selected for the HF-link parameters. $L_r = 125\ \mu$F and $C_{b1} = C_{b2} = 2\ C_b = 1\ \mu$F is selected for the designed converter. The shaded region in Fig. 7 shows the range of Δ_ϕ for load range 250 W – 1 kW.

The designed L_r and C_b should also ensure the ZVS turn-ON of all the switches. The ZVS turn-on condition requires that negative drain-to-source current is flowing through the switch to be turned ON. From Fig. 4, the current through S_1 and S_2 is i_1, hence, ZVS turn-ON condition for S_1 and S_2 depends on i_1. Similarly, ZVS turn-ON condition for S_3 and S_4 depends on i_2. Using the requirement of negative drain-to-source current, the ZVS turn-ON conditions for the switches are given by

$$i_1(t_0) = \frac{P_o}{v_{\text{in}}} + \frac{v_{\text{in}}T_s}{4L_{\text{in}}} - i_{Lr}(t_0) > 0\,[\text{ZVS for } S_2] \tag{28a}$$

$$i_1(t_2) = \frac{P_o}{v_{\text{in}}} - \frac{v_{\text{in}}T_s}{4L_{\text{in}}} - i_{Lr}(t_2) < 0\ [\text{ZVS for } S_1] \tag{28b}$$

$$i_2(t_1) = -\frac{P_o}{v_o} - \frac{v_0T_s}{4L_o} - ni_{Lr}(t_1) < 0\,[\text{ZVS for } S_3] \tag{28c}$$

$$i_2(t_3) = -\frac{P_o}{v_o} + \frac{v_0T_s}{4L_o} - ni_{Lr}(t_3) > 0\,[\text{ZVS for } S_4]\,. \tag{28d}$$

ZVS conditions for S_2 and S_3 are easily satisfied in (28) as the input and output inductor current assists in the inequality, whereas conditions for S_1 and S_4 are more critical to satisfy. Using (28) and (22), Fig. 8 showcases the $i_1(t_0)$, $i_1(t_2)$, $i_2(t_1)$, and $i_2(t_3)$ as a function of output power for the selected component parameters and specification given by Table I. As the current at the time instance of switch turn-ON satisfies the inequality given by (28), the ZVS turn-ON is ensured for all the switches of the DMAC for the full operating load range. For example, in Fig. 8(a), $i_1(t_0)$ is always greater than 0 A and monotonously increasing with output power, which indicates that i_{ds} of S_2 is negative before the gating signal is applied. Hence, ZVS turn-ON condition for S_2 is satisfied for full range of load. Similarly, other switches also satisfies the ZVS turn-ON condition as evident from Fig. 8.

Auxiliary capacitors, C_{t1} and C_{t2}: The size of C_{t1} and C_{t2} is determined using the allowed voltage variation across these capacitors. Only C_{t1} is taken as an example to illustrate the design process. Current i_1 flows through C_{t1} when S_2 is conducting $(t_0 - t_2)$, as shown in Fig. 9. By using the charge balance equation on the capacitor ($Q = CV$), C_{t1} is given by

$$C_{t1} > \frac{\int_{t_a}^{t_2} i_1(\tau)\,d\tau}{\Delta V_{Ct1}} \tag{29}$$

where ΔV_{Ct1} is the required maximum voltage variation across the capacitor at full load and t_a is time instant when $i_1 = 0$ A. The minimum C_{t1} can be obtained by solving (29) for the maximum load condition. The minimum capacitor relation for C_{t2} can also be obtained similarly. For a 5% peak-to-peak voltage ripple of the average voltage Δv_{Ct1}, minimum C_{t1} of 0.33 μF is required. $C_{t1} = C_{t2} = 0.47\ \mu$F is selected for the designed converter. Hence, the peak voltage on the auxiliary capacitor, C_{t1} is 655 V for 220 V input voltage.

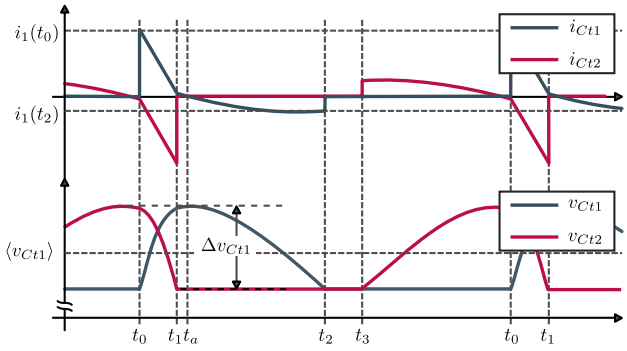

Fig. 9. Voltage and current waveform for the auxiliary capacitors.

TABLE II
DESIGNED PARAMETERS OF THE PROTOTYPE CONVERTER

Parameter	Value
L_{lk}	125 μH
L_{in}, L_o	600 μH
L_m	2 mH
C_{t1}, C_{t2}	0.47 μF
C_{b1}, C_{b1}	1 μF
C_{in}, C_o	0.5 μF
$S_1 - S_8$	UF3C120040K4S
Max. load	45 Ω
Nominal voltage gain, k	1

V. EXPERIMENTAL RESULTS

A 1-kW hardware prototype of the DMAC was built based on the design discussed in the previous section. The specifications of the designed prototype are summarized in Table II. As the two PAC-Ćuk modules are constructed identically, Table II is used for both modules. The series inductance of 125 μH is realized using split winding on the high-frequency transformer resulting in the reduced magnetic count. EE 65 N27 core is used for the transformer with 28 turns ON both the primary and secondary sides of the transformer. The input and output inductors are also realized using gapped EE 65 N27 with 36 turns. As the auxiliary capacitor clamps the switch in the PWM active-clamp converter, the peak voltage across the device is same as the peak voltage across the auxiliary capacitors.

Fig. 10 showcases the complete experimental setup of the DMAC. The two separate PAC-Ćuk modules can be seen in the figure. Texas instrument's TMS320F28379D controller is used to generate the modulated PWM signals for the DMAC and fed into each module using D-Sub shielded cables. A simple closed-loop PI controller on the output voltage, v_o is used to perform the output voltage control, as shown in Fig. 11. The reference output voltage is generated using the phase-locked loop on the input voltage v_{in} and the required rms voltage of the output port. The output of the PI controller is fed to the DMS modulator which bypasses the inactive module as per input voltage polarity, as shown in Fig. 3. It is to be noted that the sensed input voltage can also be directly used to generate the output voltage reference and polarity detection. For variable ac input source Pacific power's 360-AMX is used. The efficiency, THD of the output voltage, and the power factor at the input are measured using Tektronix's PA3000 power analyzer. The loading of the converter is performed using resistor loads.

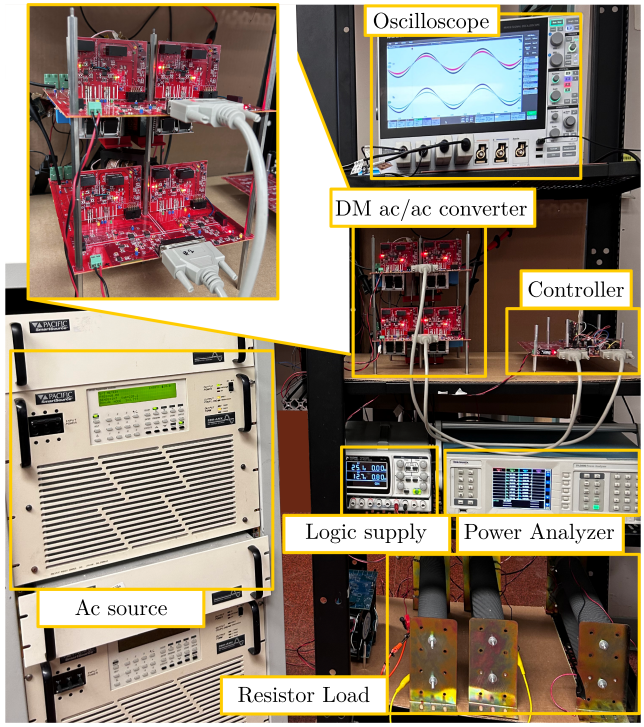

Fig. 10. Experimental setup of the proposed single-stage DM-PAC-Ćuk AC/AC converter.

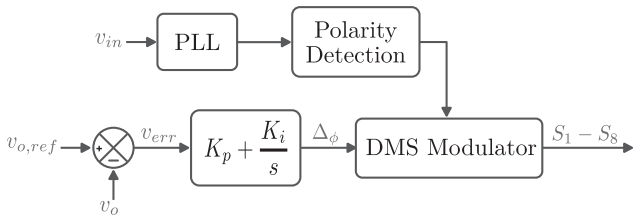

Fig. 11. Block diagram of the output voltage control.

Fig. 12(a) and (b) shows the operation of the designed hardware prototype at full load and 18% load conditions. In both load conditions, the output voltage can be seen to be following the input voltage while preserving the sinusoidal characteristic of the input port. In the case of full load (45 Ω), the output voltage total harmonic distortion (THD) is observed to be 1.45% while the input current has a power factor >0.99. The measured efficiency at full load and rated input voltage of 220 V_{rms} is 96.96%. In case of 18% load (250 Ω), the output voltage THD is measured to be 2.11% while the input current power factor is 0.85. The input current leads the input voltage for the resistive load, indicating a capacitive reactive power generated by the converter. The measured efficiency of the converter at 18% load condition is 95.01%.

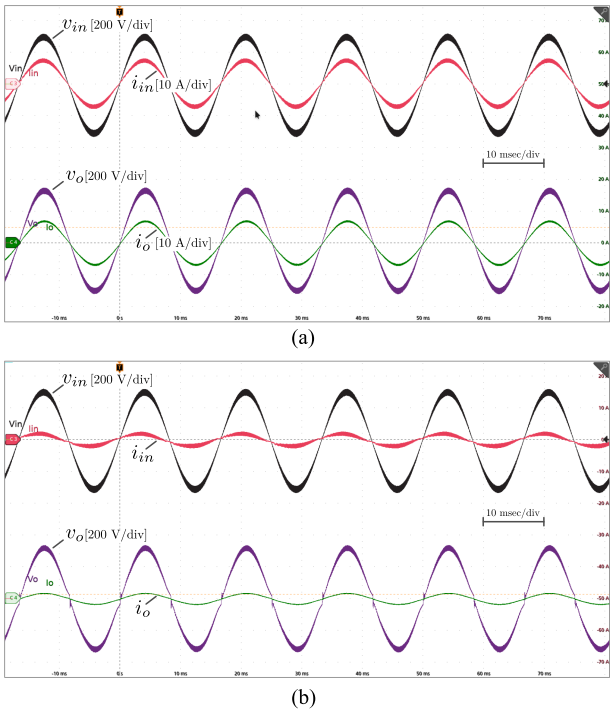

Fig. 12. Experimental waveform at 220 V_{rms} input voltage, 220 V_{rms} output voltage. (a) Full load $R_L = 45\ \Omega$. (b) $R_L = 250\ \Omega$. Input voltage v_{in}:[200 V/div], output voltage v_o:[200 V/div], input current i_{in}:[10 A/div], and output current i_o:[10 A/div].

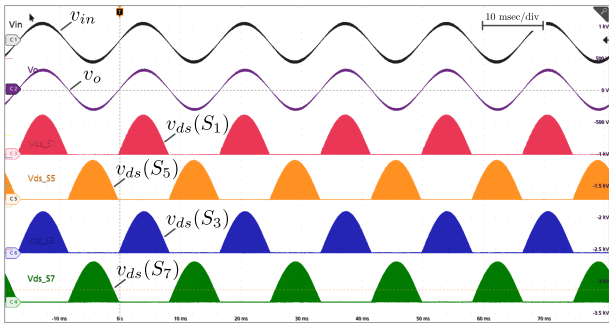

Fig. 13. Experimental results for the voltage across the switches of the DMAC over line cycles operating at full load. All signals: [500 V/div].

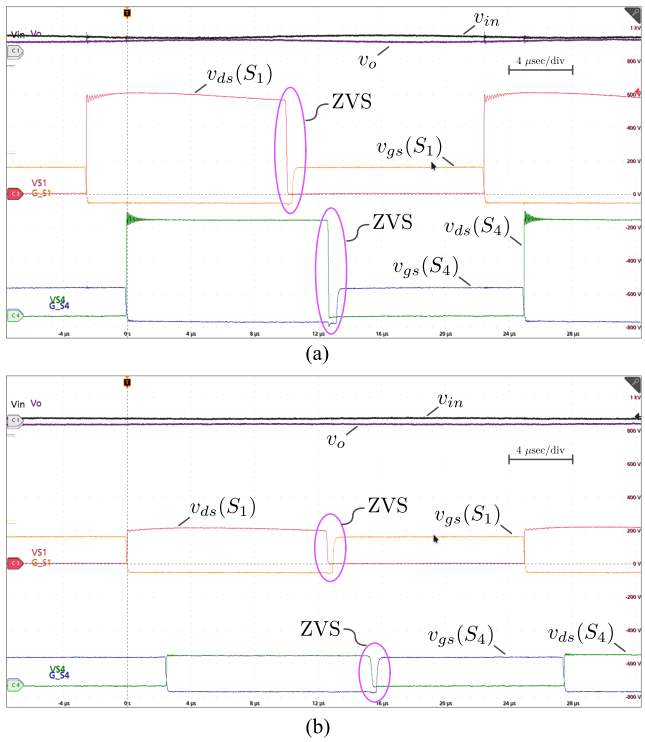

Fig. 14. Switch waveform of S_1, and S_4 showcasing ZVS turn-ON (a) near the peak of the input voltage, and (b) near zero crossing. Input voltage, v_{in}: [500 V/div], output voltage, v_o: [500 V/div], drain to source voltage of S_1, $v_{ds}(S_1)$: [200 V/div], S_4, $v_{ds}(S_4)$: [200 V/div], and gate to source voltage of S_1, $v_{gs}(S_1)$: [20 A/div], and S_4, $v_{gs}(S_4)$: [20 V/div].

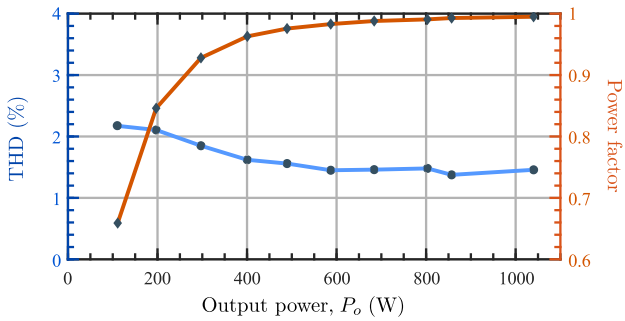

Fig. 15. Measured output voltage THD and input power factor versus the output power of the proposed converter. The blue trace is the output voltage THD, and the orange is the input current power factor.

In Fig. 13, drain to source voltages v_{ds} of switches for both the modules of the DMAC is shown. Module A is active ($S_1 - S_4$ are switching)when the input voltage is positive while Module B is active ($S_7 - S_8$ are switching) when input voltage is negative for DMS. The v_{ds} of switches follows the input and output voltage as given by (3) and shown in Fig. 3. In Fig. 14(a) , the waveform captures the switching waveforms for the instance when the voltage is near the peak of input voltage while in Fig. 14(b) the instance is near the zero-crossing. In both cases, the ZVS turn-ON of the switches can be observed as the drain to source voltage of the switches is 0 V, before the gate signal is applied indicating ZVS turn-ON across the full line cycle. The ZVS turn-on of S_2 and S_3 is not shown explicitly, however, from Fig. 14, the v_{ds} of S_1 and S_4 is getting clamped to the auxiliary capacitor on removal of gate S_1 and S_4 indicating the diode conduction of the complimentary switches S_2 and S_4. The gate of S_2 and S_4 are applied after the dead-time elapsed, resulting in ZVS turn-ON of S_2 and S_4.

Fig. 15 shows the output voltage THD and the input power factor against range of load conditions. The output voltage THD of the converter is maintained below 2.18%. Even at a 10% load condition, the THD is measured to be 2.18%. The power factor of the proposed converter is near unity for the full load condition, however, it degrades as the load is reduced. The power factor trend of Fig. 15 is observed because the converter draws a certain capacitative current (similar to LFTs magnetizing current) to maintain the desired output voltage. As the load is increased at the output, the percentage share of capacitative current drawn

TABLE III
COMPARISON WITH OTHER AC–AC CONVERTERS

Topology	This work	SHBC [31]	BISS [32]	SFBC [11]	LLC [14]	NIBB-DM [17]
Switches	8	8	10	12	12	8
Capacitor	12	5	3	5	3	4
Magnetic cores	6 (2*)	5	3	5	3	2
ZVS	Yes	Partial	Yes	Partial	Yes	No
Peak efficiency	97.3%	91.8%	94.5%	94.4%	96.3%	93.8%
Output power	1 kW	500 W	400 W	1 kW	1.5 kW	460 W
Switching frequency	40 kHz	30 kHz	20–40 kHz	30 kHz	40 kHz	60 kHz
Nominal voltage gain, k	1	1	1	1	1	1
Output voltage	220 V	110 V	110 V	220 V	220 V	120 V
Galvanic isolation	Yes	Yes	Yes	Yes	Yes	No

*Integrated magnetics solution [24], [33]

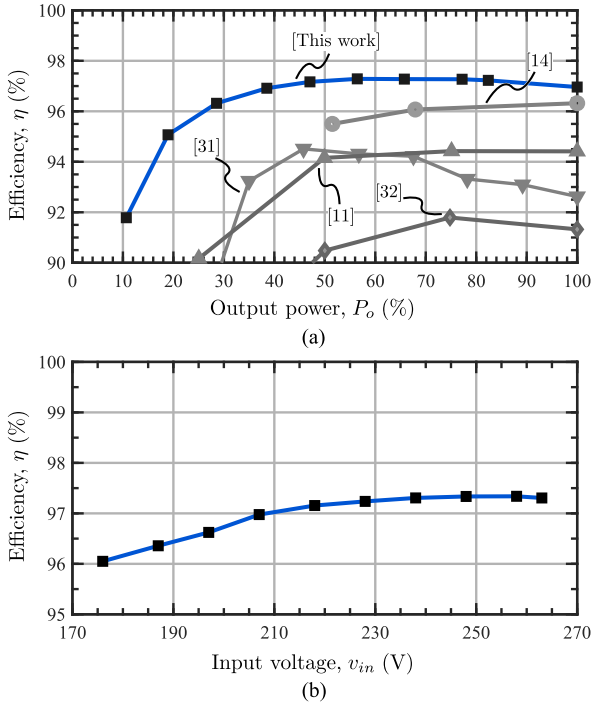

Fig. 16. Efficiency of the proposed ac/ac converter versus (a) varying output power for fixed $V_{\text{in}} = V_o = 220\ V_{\text{rms}}$, and (b) varying input voltage V_{in} for fixed $V_o = 220\ V_{\text{rms}}$ and 100% (45 Ω) output power.

to maintain the output voltage reduces resulting in near unity power factor at the full load condition. The design process discussed in Section IV minimizes the capacitor internal to the topology which in turn reduces the capacitative current for ac/ac application.

Fig. 16 shows the measured efficiency versus output power range and input voltage for fixed output voltage. In Fig. 16(a), the peak efficiency of 97.28% is measured at around 50% load condition at the nominal input voltage of 220 V_{rms}, while the measured efficiency at the full load is 97.16%. The efficiency curve is relatively flat across the 35% to 100% load range for the unity gain conversion. The flat efficiency characteristic is generally desired as the converter operates in the full load range. The efficiency drop for low load conditions is due to higher share of voltage dependent losses which are predominently magnetic losses compared to active power delivered at the output.

The proposed ac/ac converter is also operated with wide input voltage variation while maintaining the nominal output voltage to demonstrate voltage regulation capability. In Fig. 16(b), the efficiency of the proposed ac/ac converter with voltage regulation is shown. The converter maintains the high-efficiency characteristic over the wide gain. The input voltage was varied from 176 V_{rms} to 265 V_{rms} at full load. The peak efficiency of 97.34% was measured at $V_{\text{in}} = 260\ V_{\text{rms}}$. The minimum efficiency of 96.02% occurs at the minimum operated input voltage of 176 V_{rms}. At input voltage of 176 V_{rms}, the input current is 5.71 A_{rms} which is the maximum rated current. Due to higher conduction losses with lower input voltage, the efficiency of the converter is lower at lower input voltage. The proposed converter also has relatively flat efficiency for wide input voltages.

The DMAC is compared with some recently published work of similar power levels in Table III. The efficiency of the DMAC is found to be higher than the topologies presented in Table III, as also shown in Fig. 16(a) over a wide load range. In Fig. 16(a), the efficiency data is normalized over the reported peak output power to present efficiency comparison in term of percentage output power. As discussed in the introduction, the Type A ac/ac converter performs better in terms of efficiency due to lower conversion stages. The *LLC* and bidirectional flyback-based Type A ac/ac converter presented in [14] and [32], respectively, also offers high efficiency, however, the presence of folding and unfolding circuit results in a higher number of switches, as noted in Table III. The symmetric half-bridge converter (SHBC) and symmetric full-bridge converter (SFBC) based Type D ac/ac converter presented in [31] and [11], respectively, integrated the DAB converter with the rectifier and inverter stage to reduce the component counts. However, the multiconversion stage suffers from higher losses resulting in lower efficiency. The NIBB-DM with continuous module operation introduced in [21] offered peak efficiency of 93.8%. The low efficiency of the converter can be attributed to the continous operation of the two modules resulting in high conduction losses. In addtion, the hard-switch operation of the switches results in higher switching losses. The DMAC converter, unlike traditional LFT, has the ability

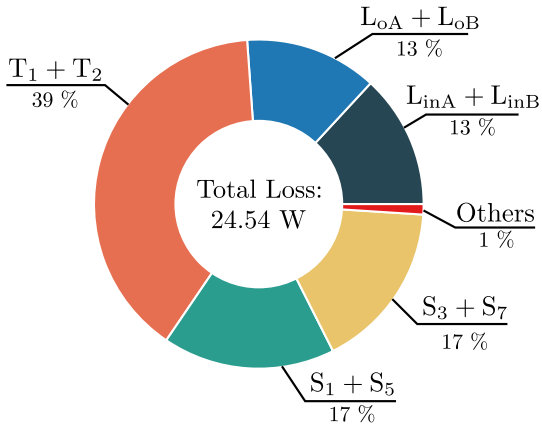

Fig. 17. Projected loss distribution of the DMAC for $V_{\text{in}} = V_o = 220\ V_{\text{rms}}$ and 100% (45 Ω) output power.

to regulate the output voltage with wide input voltage variation. The peak efficiency of the DMAC is >97%, which is comparable to LFT [1].

Fig. 17 presents the estimated loss distribution of the DMAC prototype at full load condition. More than 60% of the losses are incurred through the magnetic components. Design optimization of the magnetic component could further enhance the efficiency of the DMAC. Integration of the input and output inductors [24], [33], [34], [35] on a single magnetic core could also help in reducing the magnetic losses and component counts. The total loss incurred by the clamp circuit switches (S_2, S_4, S_6, and S_8) is near 1% of the total loss of the converter grouped under others in Fig. 17.

VI. Conclusion

This article introduces an isolated ac/ac converter based on differential-mode architecture. The DMAC is made of two symmetric PWM PAC-Ćuk dc/dc modules connected differentially to enable ac/ac converter operation. The modulation scheme of the modules of the DMAC is discussed in the article to achieve high-efficiency operation. As the dc/dc modules in the DMAC architecture are subjected to time-varying 50/60 Hz sinusoidal input voltages, the converter is required to propagate the low frequency voltage signal to the output port. Hence, the design process and operation analysis of the PAC-Ćuk dc/dc modules in the DMAC application becomes critical and is discussed in this article. A 1-kW hardware prototype was built using the design process outlined in the paper to validate the DMAC. The designed hardware prototype achieved a peak efficiency of 97.28% while maintaining a flat efficiency profile for wide load variation while output voltage THD below 2.18% is also maintained. Similar to magnetizing current in a conventional transformer, the Type A ac/ac converter exhibits capacitative current to build the output voltage. The DMAC results in >0.99 input power factor for a full load operation, however, the power factor degrades with the lower output load as the share of capacitative current to maintain the output voltage increases. The converter is also tested for wide gain by varying the input voltage from 176 V_{rms} to 265 V_{rms} while maintaining the nominal output voltage of 220 V_{rms}. Higher efficiency is observed for lower gain due to reduced copper losses for the same output power.

One of the main features of the proposed converter architecture is the modular flexibility and scalability of the architecture. As the DMAC application in power systems requires high power and high voltage rated converters, cascaded, and parallel connection of the modules for the high voltage rating will be explored in the future.

TABLE IV
Scaling of Secondary Side Component for Nonunity Voltage Conversion Gain

$V_o = V_{in}$	$V_o = kV_{in}$
$n = 1$	$n = \frac{1}{k}$
L_o	$k^2 L_o$
C_{t2}	$\frac{C_{t2}}{k^2}$
C_{b2}	$\frac{C_{b2}}{k^2}$
C_o	$\frac{C_o}{k^2}$

Appendix A
Transformer Turn Ratio, n

The transformer turn ratio is dependent on the nominal input and output voltages as given by (27). Equal nominal input and output voltage is considered for the designed hardware prototype of the DMAC resulting in unity transformer turn ratio. In Table IV, the scaling of the output side components of the DMAC for a nominal voltage gain $k = \frac{V_o}{V_{\text{in}}} = \frac{1}{n}$ is provided.

Appendix B
Acronyms and Symbols

Some of the common acronyms and symbols used are delineated as follows.

LFT	Low frequency transformer.
DPC	Direct power conversion.
PAC-Ćuk	PWM active clamp Ćuk.
C_{t1}, C_{t2}	Primary and secondary side blocking auxiliary capacitors.
C_{b1}, C_{b2}	Primary and secondary side blocking capacitors.
n	Transformer turn ratio.
C_b	Equivalent blocking capacitor referred to primary side $C_b = C_{b1} \|\| n^2 C_{b2}$.
L_r	Inductor in series with C_{b1}.
L_{in}, L_o	Input and output inductors.
$S_1 - S_4$	Switches of the Module A.
$S_5 - S_8$	Switches of the Module B.
T_s	Switching time period of the DMAC.
f_s	Switching frequency of the DMAC.
Z_r	Characteristic impedance of high frequency link formed by L_r and C_b, $Z_r = \sqrt{L_r/C_b}$.
ω_r	Angular frequency of high frequency link formed by L_r and C_b, $\omega_r = 1/\sqrt{L_r C_b}$.
Δ_ϕ	Phase-shift ratio of Module A (Module B) defined as the ratio between the time period when both

	main switch $S_1(S_5)$ and $S_3(S_5)$ are inactive to the switching period T_s.
V_{in}, V_o	Rms input and output voltages of the ac/ac converter.
v_{in}, v_o	Instantaneous input and output voltages of the ac/ac converter.
p_o	Output power transfer over a switching time period T_s.
P_o	Rms Output power transfer over a line cycle.
$i_{LrA}(t)$	Instantaneous current through L_{rA} of Module A.
$v_{CbA}(t)$	Instantaneous voltage across the equivalent blocking capacitor C_{bA} of Module A referent to primary side of the transformer.
$v_1(t), v_2(t)$	Instantaneous node voltage across the switch S_1 and S_3.
$i_1(t), i_2(t)$	Total current going into the node voltage $v_1(t)$ and $v_2(t)$ total current going out of the node voltage $v_2(t)$.

DISCLAIMER

This article is covered by the following intellectual property: S. K. Mazumder, "Solid-state power-conversion system", US Non-Provisional (Utility) Application No. 17/134178 and International PCT Application PCT/US20/67047, filed on December 2020. (Provisional patent application submitted in December 2019).

REFERENCES

[1] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 186–198, Sep. 2013, doi: 10.1109/JESTPE.2013.2277917.

[2] B. Yang et al., "A critical survey of technologies of large offshore wind farm integration: Summary, advances, and perspectives," *Protection Control Modern Power Syst.*, vol. 7, no. 1, pp. 1–32, May 2022, doi: 10.1186/S41601-022-00239-W.

[3] S. K. Mazumder, M. Tahir, and K. Acharya, "Pseudo-decentralized control-communication optimization framework for microgrid: A case illustration," in *Proc. IEEE/PES Transmiss. Distrib. Conf. Expo.*, 2008, pp. 1–8, doi: 10.1109/TDC.2008.4517290.

[4] D. Dujic, F. Kieferndorf, F. Canales, and U. Drofenik, "Power electronic traction transformer technology," in *Proc. IEEE 7th Int. Power Electron. Motion Control Conf.*, 2012, pp. 636–642, doi: 10.1109/IPEMC.2012.6258820.

[5] J. G. Nielsen and F. Blaabjerg, "A detailed comparison of system topologies for dynamic voltage restorers," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1272–1280, Sep./Oct. 2005, doi: 10.1109/TIA.2005.855045.

[6] M. J. Newman, D. G. Holmes, J. G. Nielsen, and F. Blaabjerg, "A dynamic voltage restorer (DVR) with selective harmonic compensation at medium voltage level," *IEEE Trans. Ind. Appl.*, vol. 41, no. 6, pp. 1744–1753, Nov./Dec. 2005, doi: 10.1109/TIA.2005.858212.

[7] J. Rosas-Caro and F. Peng, "Voltage swell /sag compensation with single-phase Z-source AC/AC converter keywords proposed topology," pp. 1–8, 2009. [Online]. Available: https://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5156277

[8] A. Honrubia-Escribano, E. Gómez-Lázaro, A. Molina-García, and J. A. Fuentes, "Influence of voltage dips on industrial equipment: Analysis and assessment," *Int. J. Elect. Power Energy Syst.*, vol. 41, no. 1, pp. 87–95, 2012, doi: 10.1016/j.ijepes.2012.03.018.

[9] L. Zheng, R. P. Kandula, and D. Divan, "Soft-switching solid-state transformer with reduced conduction loss," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5236–5249, May 2021, doi: 10.1109/TPEL.2020.3030795.

[10] J. Ge, Z. Zhao, L. Yuan, and T. Lu, "Energy feed-forward and direct feed-forward control for solid-state transformer," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4042–4047, Aug. 2015, doi: 10.1109/TPEL.2014.2382613.

[11] O. C. Da Silva Filho, F. L. Tofoli, L. H. S. C. Barreto, and D. De Souza Oliveira, "Single-phase isolated AC-AC symmetrical full-bridge converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 1, pp. 846–855, Feb. 2022, doi: 10.1109/JESTPE.2021.3107335.

[12] Q. Huang, S. Rajendran, S. Sen, Z. Guo, L. Zhang, and A. Q. Huang, "500kVA hybrid solid state transformer (HSST): Architecture, functionality and control," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 4864–4871, doi: 10.1109/ECCE44975.2020.9235435.

[13] Z. Guo, S. Sen, S. Rajendran, Q. Huang, X. Feng, and A. Q. Huang, "Design of a 200 kW medium-frequency transformer (MFT) with high insulation capability," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 3471–3477, doi: 10.1109/ECCE44975.2020.9235985.

[14] L. F. Pacheco, K. C. M. Nascimento, and I. Barbi, "Isolated AC/AC converter with LLC resonant converter high-frequency link and four-quadrant switches in the output stage," *IEEE Access*, vol. 8, pp. 213104–213114, 2020, doi: 10.1109/ACCESS.2020.3040617.

[15] H. Qin and J. W. Kimball, "Solid-state transformer architecture using AC-AC dual-active-bridge converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3720–3730, Sep. 2013, doi: 10.1109/TIE.2012.2204710.

[16] J. Huang, Y. Wang, Z. Li, and W. Lei, "Unified triple-phase-shift control to minimize current stress and achieve full soft-switching of isolated bidirectional DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4169–4179, Jul. 2016, doi: 10.1109/TIE.2016.2543182.

[17] S. Ćuk and R. D. Middlebrook, "Advances in switched-mode power conversion part I," *IEEE Trans. Ind. Electron.*, vol. IE-30, no. 1, pp. 10–19, Feb. 1983, doi: 10.1109/TIE.1983.356697.

[18] S. Mehrnami, S. K. Mazumder, and H. Soni, "Modulation scheme for three-phase differential-mode Ćuk inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2654–2668, Mar. 2016, doi: 10.1109/TPEL.2015.2442157.

[19] S. Mehrnami and S. K. Mazumder, "Discontinuous modulation scheme for a differential-mode Ćuk inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1242–1254, Mar. 2015, doi: 10.1109/TPEL.2014.2314688.

[20] C. Bao, S. Gupta, and S. K. Mazumder, "Modeling and analysis of peak-current-controlled differential mode Ćuk inverter," in *Proc. IEEE 12th Int. Symp. Power Electron. Distrib. Gener. Syst.*, 2021, pp. 1–7, doi: 10.1109/PEDG51384.2021.9494167.

[21] A. A. Khan, H. Cha, and H. F. Ahmed, "An improved single-phase direct PWM inverting buck-boost AC-AC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5384–5393, Sep. 2016, doi: 10.1109/TIE.2016.2565461.

[22] S. Gupta and S. K. Mazumder, "A novel modulation scheme for isolated PWM active-clamp Ćuk DC/DC converter," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14966–14980, Dec. 2022, doi: 10.1109/TPEL.2022.3189672.

[23] D. B. Costa and C. M. C. Duarte, "The ZVS-PWM active-clamping Ćuk converter," *IEEE Trans. Ind. Electron.*, vol. 51, no. 1, pp. 54–60, Feb. 2004, doi: 10.1109/TIE.2003.819697.

[24] A. Sepahvand, M. Doshi, V. Yousefzadeh, J. Patterson, K. K. Afridi, and D. Maksimovic, "Automotive LED driver based on high frequency zero voltage switching integrated magnetics Ćuk converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–8, doi: 10.1109/ECCE.2016.7854893.

[25] N. Kumar, M. Mohamadi, and S. K. Mazumder, "Passive damping optimization of the integrated-magnetics-based differential-mode Ćuk rectifier," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10008–10012, Oct. 2020, doi: 10.1109/TPEL.2020.2981918.

[26] S. Gupta and S. K. Mazumder, "Hysteresis based triangular current mode control for bridgeless totem pole converter," in *Proc. IEEE 12th Int. Symp. Power Electron. Distrib. Gener. Syst.*, 2021, pp. 1–7, doi: 10.1109/PEDG51384.2021.9494197.

[27] H. Li-Gao and W. Jian, "Selection of the current ripple ratio of converters and optimal design of output inductor," in *Proc. IEEE 5th Conf. Ind. Electron. Appl.*, 2010, pp. 1163–1167, doi: 10.1109/ICIEA.2010.5515878.

[28] Y. Xie, J. Sun, and J. S. Freudenberg, "Power flow characterization of a bidirectional galvanically isolated high-power DC/DC converter over a wide operating range," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 54–66, Jan. 2010, doi: 10.1109/TPEL.2009.2024151.

[29] H. Bai, C. C. Mi, and S. Gargies, "The short-time-scale transient processes in high-voltage and high-power isolated bidirectional DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2648–2656, Nov. 2008, doi: 10.1109/TPEL.2008.2005106.

[30] H. Zhou and A. M. Khambadkone, "Hybrid modulation for dual-active-bridge bidirectional converter with extended power range for ultracapacitor application," *IEEE Trans. Ind. Appl.*, vol. 45, no. 4, pp. 1434–1442, Jul./Aug. 2009, doi: 10.1109/TIA.2009.2023493.

[31] O. C. D. S. Filho, F. L. Tofoli, D. Honorio, L. H. Barreto, and D. D. S. Oliveira, "Single-phase isolated AC-AC converters based on the dual active bridge converter," *IEEE Trans. Ind. Electron.*, vol. 69, no. 6, pp. 5680–5689, Jun. 2022, doi: 10.1109/TIE.2021.3088363.

[32] K.-Y. Lo and W.-Y. Wang, "Bidirectional isolated single-stage single-phase AC-AC converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 6, pp. 6828–6836, Dec. 2021, doi: 10.1109/JESTPE.2021.3074307.

[33] D. P. Fernandez, R. A. Fantino, J. C. Balda, and S. K. Mazumder, "Inductor and transformer-coupled magnetic structure for zero-ripple DC-DC cúk converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 654–659, doi: 10.1109/APEC42165.2021.9487405.

[34] M. Mohamadi and S. K. Mazumder, "Confluence of integrated magnetics and TCM for a ZVS based higher-order differential-mode rectifier," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 8624–8642, Jul. 2023, doi: 10.1109/TPEL.2023.3265350.

[35] M. Mohamadi, S. K. Mazumder, and N. Kumar, "Integrated magnetics design for a three-phase differential-mode rectifier," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10561–10570, Sep. 2021, doi: 10.1109/TPEL.2021.3066506.

Shantanu Gupta (Graduate Student Member, IEEE) received the B.Tech. degree in electrical engineering from Delhi Technological University, Delhi, India, in 2016. He is currently working toward the Ph.D. degree in electrical and computer engineering with the University of Illinois Chicago, Chicago, IL, USA.

From 2016 to 2019, he was a Research Engineer with TEX E.G., Japan. His work involved working on embedded and power electronics systems. Among the projects he worked on were the development of a semiconductor wafer alignment machine and a motor driver for a refrigerator compressor. His research interests include soft-switching techniques and power electronics topologies.

Mr. Gupta is a Reviewer for IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS.

Sudip K. Mazumder (Fellow, IEEE) received the Ph.D. degree in electrical and computer engineering from Virginia Tech, Blacksburg, VA, USA, in 2001.

He has been the President with NextWatt LLC, Hoffman Estates, IL, USA, since 2008 and has been a Professor with University of Illinois Chicago, Chicago, IL, USA, since 2001. He has more than 30 years of professional experience and has held research and development and design positions in leading industrial organizations and was a technical consultant for several industries.

Prof. Mazumder was named a Fellow of the American Association for the Advancement of Science, in 2020, and a Fellow of the Asia-Pacific Artificial Intelligence Association in 2022. He is the Editor in Large for the IEEE TRANSACTIONS ON POWER ELECTRONICS since 2019 and was an IEEE Distinguished Lecturer between 2016–2019. He has been an Administrative Committee Member for IEEE Power Electronics Society (IEEE PELS), since 2015. He has also been a Member-at-Large for IEEE PELS, since 2020. He was the Chair for the IEEE PELS Technical Committee on Sustainable Energy Systems, from 2015 to 2020. He was the General Chair for IEEE International Symposium on Power Electronics for Distributed Generation Systems Conference in 2023. He is the recipient of the 2023 IEEE Power and Energy Society's Ramakumar Family Renewable Energy Excellence Award, and several IEEE awards/honors, including IEEE TRANSACTIONS ON POWER ELECTRONICS Prize Paper Awards (2022, 2002) and Highlighted Papers (2023, 2022, 2018), Featured Article for IEEE TRANSACTIONS ON BIOMEDICAL ENGINEERING (2023), IEEE Conference Best Paper Award (2013), and IEEE International Future Energy Challenge Award (2005). In June 2023, he was chosen as a recipient of the honorary title of UIC Distinguished Professor to be effective in AY'23 pending Board of Trustees approval. He is the recipient of the most prestigious awards at UIC, including Distinguished Researcher Award in Natural Sciences and Engineering (2020), Inventor of the Year Award (2014), and University Scholar Award (2013). Earlier, he received the prestigious U.S. Office of Naval Research Young Investigator Award (2005) and the U.S. National Science Foundation CAREER Award (2003). He has also made original contributions to the areas of control of power-electronic systems at the semiconductor device level for numerous and wide-ranging applications in commercial and defense space; high-frequency-link power electronics, including hybrid-modulation-based pulsating-dc-link inverter and differential-mode-converter (ac/ac, dc/ac, ac/dc) topologies for applications encompassing but not limited to renewable and alternative energy, electric vehicles, solid-state transformer, energy storage, and offshore wind; discretized high-frequency and Boolean energy and data transfer; and optically-controlled power semiconductor devices (including optical emitter turn-OFF thyristor, heterojunction devices, high-gain bipolar devices, and hybrid and monolithic photoconductive semiconductor switches) and power electronics.