Design and Performance Analysis of Cuk SIDO Converter Using PI-Lead Compensator for EV Auxiliary Power Supply

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***Abstract*—This article presents a proportional–integral–lead (PI-Lead) compensator for a single-input multi-output (SIMO) converter used in EV auxiliary power supply applications. The proposed SIMO converter (SIMOC) is made by adding an extra switch and inductor to each output port of the standard Cuk converter. This converter archives N-outputs with independent control. To bring out better clarity about the design and analysis of SIMO converter, the operating principle, mathematical modeling and performance characteristics of a simplified Cuk single input dual output converter (SIDOC) are analyzed. However, the cross-regulation (CR) and cross-coupling (CC) problems caused by the coupled capacitor in Cuk SIDOC make the converter unstable. Also, these problems make it harder to design the control constraints. So, this article suggests the design and analysis of a PI-Lead compensator to deal with the converter's CC and CR problems. MATLAB/Simulink is used to test how well the proposed control algorithm works. A hardware prototype is also made in the laboratory to validate the efficacy of the proposed controller. The transient performance of Cuk SIDOC with the proposed control algorithm proves that it can eliminate CC and CR effects and handle parameter uncertainties.**

***Index Terms*—Auxiliary power supply, compensator design, decoupling network, single-input dual-output converter (SIDOC), single-input multi-output converter (SIMOC).**

I. Introduction

THE modern technologies with which we are so familiar, such as computers, electric vehicle auxiliary power supplies [1], internet, wireless communications [2], renewable energy systems [3], portable power electronic devices [4], etc., all started from the invention of integrated circuits. DC-DC converters that provide more than one output are often necessary in order to support a variety of loads that operate at varying voltages. However, in order to obtain the 'N' independent output, it is necessary to have the 'N' number of the independent converter. As a result, in order to bring the total cost of the system down, recent research has focused heavily on investigating a large number of new shared switches or inductors that have numerous output converters [5], [6]. For instance, Fig. 1 depicts how the SIMOC can be utilized in the auxiliary power supply of an electric vehicle.

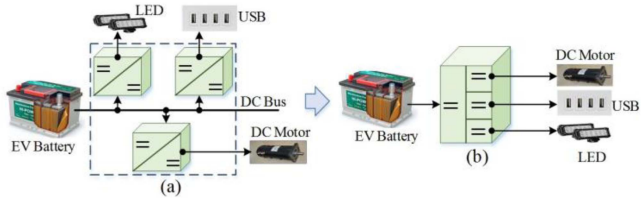

Fig. 1. Application of SIMO converters in EV auxiliary power supply: (a) conventional and (b) proposed.

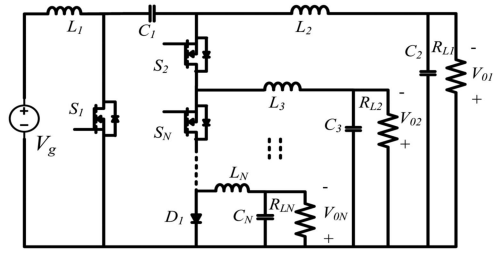

Fig. 2. Multi-output Cuk converter topology.

In previous literature, numerous innovative SIMOC topologies, such as integrated SIMO [7], [8] and coupled inductor SIMOCs (CI-SIMOCs) [9], have been described. For better clarity about the design and analysis of Cuk SIMOC, as given in Fig. 2, a simplified Cuk SIDOC modeling, operating principle and performance characteristics are analyzed. However, controlling each output voltage independently in a dual output converter is required for the device to function effectively. However, in the case of the SIDOC, it is afflicted by severe issues such as cross-regulation and cross-coupling, which places the converter in a mode in which it is difficult to control the output voltage independently [10]. A change in the reference voltage

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of one output affects another output, which is referred as CC. Furthermore, any load change on one output affects the current flowing through the other output. This condition is called CR. Both concerns have an impact on the performance of the system during the transient phase and the steady-state phase.

By utilizing the linked inductor, the buck CI-SIDOC is able to enhance converter efficiency. This is accomplished by lowering the current ripple [9]. However, the size of the converter will expand due to the use of a coupling transformer, and the design will become more complicated. To solve the problem, a conventional buck converter is used as a starting point for developing the buck SIDOC [11]. To regulate the output voltage, only two switches are used; however, the second output voltage is not controlled over its whole range.

In the topology of the Cuk converter, the inclusion of an inductor on both the input and output side helps to reduce the output current ripple. In contrast, the presence of a linked capacitor helps to minimize the voltage ripple. Additionally, the capacitive stored energy transfer is more effective than coupled inductor or single inductor SIMO converters for transferring power between the input and output ports. Because of this, the Cuk converter-based SIDOC topology is considered in this article. In [12], a condensed presentation of the topological synthesis of the converter is provided. However, much emphasis is not placed on developing a control approach to nullify the influence of CC and CR. Therefore, to address these two difficulties, this article aims to design an adaptive closed-loop control method, which ultimately enhances the performance and efficiency of the converter. Because of this, a necessary need of a SIMOC is the ability to adjust the output voltages independently.

In [13], a switching strategy known as time-division multiplex switching is suggested. Each switching mode in this article is broken down into *N* sub-modes, each of which can provide *N* outputs and can be operated separately. This removes CR but results in a significant current ripple when applied to conditions with a high load.

In [8], predictive and multivariable numerical control is proposed to remove CR. Nevertheless, the analysis, computations, and execution of these procedures are challenging. In [11], the solution to the issue of CR with a straightforward PI controller is recommended to be incorporated into a SIDOC. However, the CC effect is not taken into account in [14]. The suggested control algorithm eliminates the CR effect by regulating the common and differential-mode output voltages independently In [15], a cross-derivative state feedback controller that is based on small-signal modeling is proposed. The small-signal modeling is accomplished by taking an average of the ripple in the inductor current. The operation of the controller is determined by the pole and zero locations for CC and CR compensations concerning the operating point of the system. As a result, the converter's performance is susceptible to different variations in the input voltage and the converter settings.

A decoupled voltage mode control [16], a decoupled current-mode control [17] and predictive digital current control [18] are offered as solutions to these issues in SIMOCs. These solutions prevent voltage fluctuations, mitigate CC and CR issues, and improve output voltage stability. Nevertheless, the complexity of the converter may be increased due to the design of the controller. The major highlights of the article are summarized as follows.

1) The proposed SIMOC is derived from a conventional Cuk converter by adding a set of switches and inductors to each individual output port.
2) It is proposed to use a decoupler with a PI-Lead compensation in a Cuk SIDOC to eliminate CC and CR issues.
3) In this design, the PI-Lead compensator parameters are tuned in such a way that the PI control unit improves the steady-state response. In contrast, the Lead control unit improves the transient response of the uncompensated system.
4) The closed-loop stability of the proposed controller is analyzed and verified by both MATLAB/simulation and experimental results.

However, this article is a continuation of the previous work in [16]. In [16], a model of the Cuk SIDOC was developed showcasing a decoupled-based voltage mode controller. The unsolved issues of the article are discussed and fixed in Section III of this article.

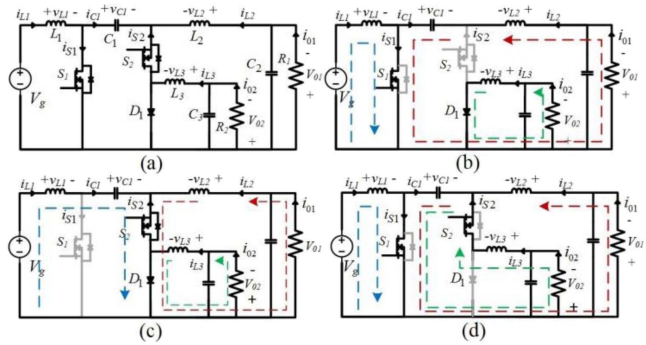

Fig. 3. Topological state of proposed Cuk SIDOC: (a) equivalent circuit, (b) interval-1, (c) interval-2, and (d) interval-3.

II. Operating Principle of Cuk SIDOC

In this section, the performance of the proposed converter is evaluated in three dissferent intervals using all of the switching states that are conceivable.

A. Power Electronic Circuit

The schematic representation of the SIDOC's circuit layout can be found in Fig. 3. There are two output ports on the converter. The regulation of the port-1and 2 output voltage (V_{01} and V_{02}) is accomplished by adjusting the duty cycles of the switches S_1 and S_2. To increase the output voltage quality, the output ports have been out fitted with low-pass filters L_2-C_2 and L_3-C_3 respectively. The input and output ports are connected by a coupled capacitor, which is denoted by the letter C_1. Within the context, the duty cycle of the switches S_1 and S_2 is referred to by the notation D_{S1} and D_{S2} respectively.

B. Operational Principle

A switching period, denoted by the notation T_S, is segmented into three periods in accordance with the switching condition of the Cuk SIDOC. The operation of the circuit during each interval is detailed below, and the corresponding figures are given in Fig. 3(b), (c), and (d), respectively.

Interval-1 ($t_0 - t_1$): Before time t_0, the switches S_1 and S_2 are in the ON position and the D_2 is in reverse-biased condition. Now the time t_0, S_1 is still turned ON, but S_2 is switched OFF while D_2 becomes forward-biased. The voltage across inductors

are $v_{L1} = v_g$, $v_{L2} = v_{C1} - v_{01}$, $v_{L3} = -v_{02}$. As a direct result of this, the inductor currents i_{L1} and i_{L2} are increasing in a linear manner whilst i_{L3} decreasing in a linear manner. For interval 1, the state-space equations are as follows:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_g \ , \ L_3 \frac{di_{L2}}{dt} = v_{C1} - V_{01}, L_3 \frac{di_{L3}}{dt} = -V_{02} \\ i_{C1} = -i_{L2} \ , \ i_{C2} = i_{L2} - V_{01}/R_1, \ i_{C3} = i_{L3} - V_{02}/R_2 \end{cases} \tag{1}$$

Interval-2 ($t_1 - t_2$): At this point t_1, S_1 is turned OFF and S_2 is turned ON while D_2 continues to be forward-biased. The voltage across inductors are $v_{L1} = v_g - v_{C1}$, $v_{L2} = -v_{01}$, $v_{L3} = -v_{02}$. As a result, the inductor currents i_{L1}, i_{L2} and i_{L3} are decreasing in a linear manner. For interval 2, the state-space equations are as follows:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_g - v_{C1}, \ L_3 \frac{di_{L2}}{dt} = -V_{01}, L_3 \frac{di_{L3}}{dt} = -V_{02} \\ i_{C1} = i_{L1} \ , \ i_{C2} = i_{L2} - V_{01}/R_1, i_{C3} = i_{L3} - V_{02}/R_2 \end{cases} \tag{2}$$

Interval-3 ($t_2 - t_3$): At this point t_2, both the switches S_1 and S_2 is turned ON, whereas D_2 has become reverse-biased. The voltage across inductors are $v_{L1} = v_g$, $v_{L2} = v_{C1} - v_{01}$, $v_{L3} = v_{C1} - v_{02}$. As a result, the current flowing through the inductors i_{L1}, i_{L2} and i_{L3} are increasing linearly. For interval 3, the state-space equations are as follows:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_g \ , L_2 \frac{di_{L2}}{dt} = v_{C1} - V_{01}, L_3 \frac{di_{L3}}{dt} = v_{C1} - V_{02} \\ i_{C1} = -i_{L2} - i_{L3}, \ i_{C2} = i_{L2} - V_{01}/R_1, \ i_{C3} = i_{L3} - V_{02}/R_2 \end{cases} \tag{3}$$

Using the volt-sec balanced approach across the inductors L_1, L_2 and L_3, the steady-state relations among the capacitor voltage, the inductor current and duty cycle are presented as follows:

$$V_{C1} = \frac{V_g}{1 - D_{S1}} \ ,$$

$$V_{01} = V_{C2} = \frac{D_{S1}}{1 - D_{S1}} V_g, V_{02} = V_{C3} = \frac{D_{S1} + D_{S1} - 1}{1 - D_{S1}} V_g \tag{4}$$

$$I_{L1} = \frac{D_{S1}}{1 - D_{S1}} I_{L2} + \frac{D_{S1} + D_{S2} - 1}{1 - D_{S1}} I_{L3},$$

$$I_{01} = I_{L2} = \frac{V_{01}}{R_1} \ , I_{02} = I_{L3} = \frac{V_{02}}{R_2} \tag{5}$$

In (4), the output voltage V_{01} is dependent on the magnitude of the input voltage as well as the duty ratio of the switch S_1. However, according to (4), the output voltage V_{02} is dependent on the input voltage as well as the duty ratio of both switches S_1 and S_2. As a result, the CC and CR effects manifest themselves while trying to regulate the reference voltage and load at port-1.

III. Problem Formulation

Before designing the Cuk SIDOC's control system, it is essential to determine plant characteristics. The state-space averaging method is used to obtain various transfer functions (TFs). The average state-space model of the converter in continuous conduction mode is depicted in the form of a matrix in (6). The whole system consists of six state variables comprising three inductor currents, two output voltages, and a coupled capacitor voltage and is written by a state vector $x = [i_{L1} \quad i_{L2} \quad i_{L3} \quad v_{C1} \quad v_{C2} \quad v_{C3} \ ]^T$.

A. Small-signal Modeling

The small-signal model is obtained by linearizing the nonlinear state-space model and the TFs are derived to determine the Cuk SIDOC's dynamic behavior. The state-space model is

$$\dot{\hat{x}} = A\hat{x} + B\hat{u}, \ \ \hat{y} = C_t\hat{x} + D\hat{u} \tag{6}$$

Where $\hat{x} = [\widehat{i_{L1}} \quad \widehat{i_{L2}} \quad \widehat{i_{L3}} \quad \widehat{v_{C1}} \quad \widehat{v_{C2}} \quad \widehat{v_{C3}}]$,

$\hat{u} = [\widehat{v_g}]$ and $\hat{y} = [\widehat{v_{01}} \quad \widehat{v_{02}}]$

For small-signal modeling, ac perturbations are added x, v_g, and d_{S1}, d_{S2} , which are as given below.

$$x = X + \hat{x}, \quad v_g = V_g + \hat{v}_g, \ d_{s1} = D_{S1} + \widehat{d_{s1}} \text{ and } d_{s2} = D_{S2} + \widehat{d_{s2}} \tag{7}$$

By substituting values from (7) into (6), ignoring the higher-order terms and separating the DC and AC terms, the small-signal model of the Cuk SIDOC in matrix form is depicted below:

$$\dot{\hat{X}} = A\hat{x} + B\hat{V}_g + B_{DS1}\hat{D}_{S1} + B_{DS2}\hat{D}_{S2},$$

$$\hat{y} = C_t\hat{x} + D\hat{u} + D_{ds1}\hat{d}_{S1} + D_{ds2}\hat{d}_{S2} \tag{8}$$

Using the Laplace transform of (8) and simplifying

$$\hat{X}\ (t) = (sI - A)^{-1}\left(B\hat{V}_g\,(t) + B_{DS1}\hat{D}_{S1}\,(t) + B_{DS2}\hat{D}_{S2}\,(t)\right) \tag{9}$$

$$\hat{Y}\ (t) = C_t(sI - A)^{-1}\left(B\hat{V}_g\,(t) + B_{DS1}\hat{D}_{S1}\,(t) + B_{DS2}\hat{D}_{S2}\,(t)\right) + D\hat{u} + D_{ds1}\hat{d}_{S1} + D_{ds2}\hat{d}_{S2} \tag{10}$$

where

$$B_{ds1} = \left[\frac{V_C}{L} \quad \frac{V_C}{L_1} \quad \frac{V_C}{L_2} \quad \frac{-1}{C}(I_L + I_{L1} + I_{L2}) \quad 0 \quad 0\right]^T$$

$$B_{ds2} = \left[0 \quad 0 \quad \frac{V_C}{L_2} \quad \frac{-I_{L2}}{C} \quad 0 \quad 0 \ \right]^T$$

$$D = D_{dS1} = D_{dS2} = 0$$

Considering (8) for output voltage V_{01} and V_{02}, input voltage V_g and duty cycle D_{S1}, D_{S2} the input to output and control to output small-signal TF of Cuk SIDOC are respectively given as

$$\begin{cases} \frac{\hat{v}_{01}(s)}{\hat{d}_{S1}(s)} = C_t\,(sI - A)^{-1}B_{DS1} \\ \frac{\hat{v}_{01}(s)}{\hat{d}_{S2}(s)} = C_t\,(sI - A)^{-1}B_{DS2} \\ \frac{\hat{v}_b(s)}{\hat{d}_{S1}(s)} = C_t\,(sI - A)^{-1}B_{DS1} \\ \frac{\hat{v}_b(s)}{\hat{d}_{S2}(s)} = C_t\,(sI - A)^{-1}B_{DS2} \end{cases} \tag{11}$$

Using the Laplace transform of (11) and simplifying, the TF of Cuk SIDOC is expressed in matrix form as depicted in (12) and (13).

$$\hat{Y}\ (s) = \left(C_t(sI - A)^{-1}B + D\right)\ \hat{U}\,(s) \tag{12}$$

$$\begin{bmatrix} \hat{v}_{01}\,(s) \\ \hat{v}_{02}\,(s) \end{bmatrix} = \begin{bmatrix} G_{11}\,(s) & G_{12}\,(s) \\ G_{21}\,(s) & G_{22}\,(s) \end{bmatrix} \begin{bmatrix} \hat{d}_{S1}\,(s) \\ \hat{d}_{S2}\,(s) \end{bmatrix} \begin{bmatrix} G_{v1g}\,(s) \\ G_{v2g}\,(s) \end{bmatrix} [\hat{v}_g \ \ (s)] \tag{13}$$

From (9), the duty cycle to output voltage TFs is derived by considering $\hat{v}_g = 0$ and provided as

$$\begin{bmatrix} \hat{v}_{01} \\ \hat{v}_{02} \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} \hat{d}_{S1} \\ \hat{d}_{S2} \end{bmatrix} \tag{14}$$

To estimate the TF, Leverrier's algorithm [16] is used to find the inverse of the matrix as given below:

$$(sI - A)^{-1} = \frac{Adj(sI-A)}{|sI-A|} = \frac{P_{n-1}s^{n-1} + P_{n-2}s^{n-2} + \ldots + P_1 s + P_0}{s^n + a_{n-1}s^{n-1} + \ldots + a_1 s + a_0} \tag{15}$$

The state-space model of Cuk SIDOC and the plant TF is derived below.

Where

$$x = [i_{L1} \quad i_{L2} \quad i_{L3} \quad v_{C1} \quad v_{C2} \quad v_{C3}]^T$$

$$y = [v_{01} \quad v_{02}]^T$$

$$u = [v_g \quad D_{S1} \quad D_{S2}]^T$$

$$A = \begin{bmatrix} 0 & 0 & 0 & \frac{-(1-D_{S1})}{L_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{D_{S1}}{L_2} & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & \frac{D_{S1}+D_{S2}-1}{L_3} & 0 & \frac{-1}{L_3} \\ \frac{(1-D_{S1})}{C_1} & \frac{-D_{S1}}{C_1} & \frac{-(D_{S1}+D_{S2}-1)}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & \frac{-1}{R_1C_2} & 0 \\ 0 & 0 & \frac{1}{C_3} & 0 & 0 & \frac{-1}{R_2C_3} \end{bmatrix},$$

$$B = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{-1}{C_2} & 0 \\ 0 & 0 & \frac{-1}{C_3} \end{bmatrix},$$

$$C_t = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

B. Problem Description of SIDO Converter

The small-signal modeling allows for the extraction of the output TFs $G_{11}(s)$, $G_{22}(s)$,$G_{12}(s)$ and $G_{21}(s)$ from [16], [19]. Multiple peaks can be seen in the magnitude plot of the bode plot in Fig. 4, depicting the duty cycles to output voltage TFs. The existence of multiple peaks has an impact on the stability of the converter [20].

The open-loop simulation result of the Cuk SIDOC shows the CC and CR effect. As depicted in Fig. 5(a), when the input voltage increased from 48V to 52V in steps, then the output voltages V_{01} and V_{02} also changed (4). The change in duty ratio of the switch S_1 from 56% to 68% changes the output voltage V_{01} as illustrated in Fig. 5(b). At the same time, the output voltage V_{02} changes, indicating the existence of CC effects in the Cuk SIDOC. Similarly, the variation in the duty ratio of the switch S_2 from 75% to 85% results in the variation of output voltage V_{02} from 24V to 28V as illustrated in Fig. 5(c). At the same time, the output voltage V_{01} changes with an overshoot of 2V. This indicates the presence of CC effects in the SIDOC. When the load of port-1 changes, the port's current and voltage fluctuate as expected. But it also changes the current and voltage at port-2, as depicted in Fig. 6(a). This means the converter is affected by the CR effect. Similarly, when the load in port 2 changes, the current and voltage in port-1 also change, as depicted in Fig. 6(b). PI-Lead compensator is proposed in this article as a solution to the aforementioned Cuk SIDOC problems.

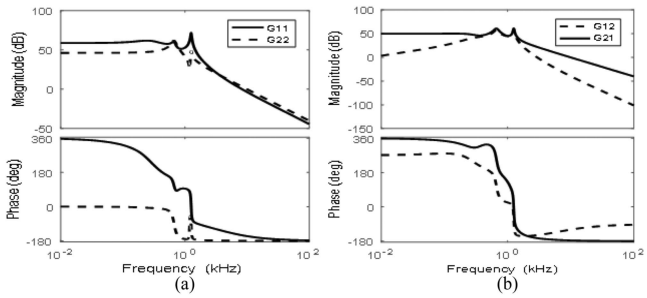

Fig. 4. Bode diagram of (a) control to output TFs $G_{11}(s)$, $G_{22}(s)$ and (b) CC TFs $G_{12}(s)$, $G_{21}(s)$.

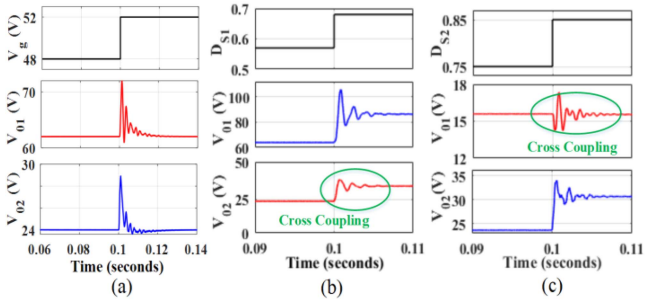

Fig. 5. Transient response of Cuk SIDOC in open-loop condition. (a) Step change in V_g from 48V to 52V. (b) Step change in D_{S1} from 56% to 68%. (c) Step change in D_{S2} from 75% to 85%.

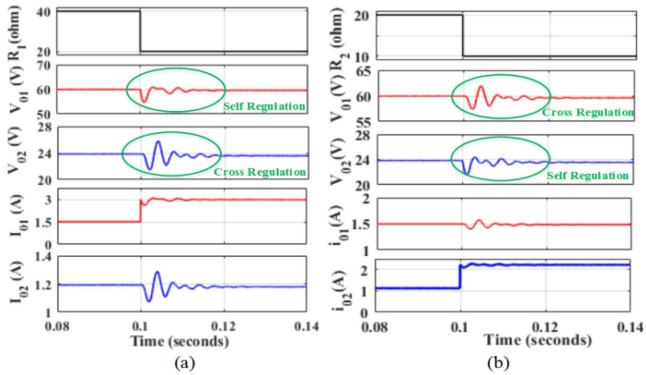

Fig. 6. Effect of cross-regulation and self-regulation in Cuk SIDOC. (a) R_1 from 40 Ω to 20 Ω and (b) R_2 from 20 Ω to 10 Ω.

IV. Proposed Decoupled Based Voltage Mode Controller With PI-Lead Compensator

The plant TF of Cuk SIDOC is $G(s) = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix}$. The TF *G(s)* is a MIMO system, which necessitates a decoupling network in order to construct compensators due to the interference

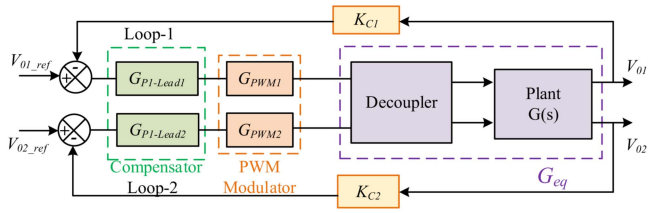

Fig. 7. Closed-loop decoupling network of Cuk SIDOC.

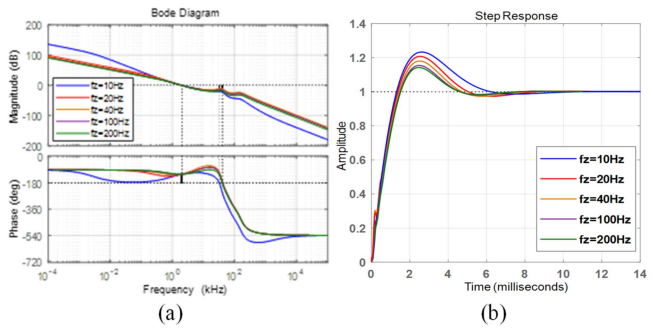

Fig. 8. Compensated G_{eq1} responses with different f_z at $f_{gc} = 2$ kHz and $\emptyset_{margin} = 75^0$. (a) Bode plot. (b) Step response.

caused by several interacting control loops. To achieve this objective of creating two self-regulating control loops, as illustrated in Fig. 7, a decoupler matrix $D = \begin{bmatrix} -g_{22}/g_{21} & 1 \\ 1 & -g_{11}/g_{12} \end{bmatrix}$ is utilized in the decoupling network. The matrix $[D]$ is combined with the plant matrix $[G]$ resulting in an equivalent decoupled TF [21]. Therefore, these two self-regulating control loops work without disconcerting one another, as described in (16).

$$G_{eq} = G*D = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} * \begin{bmatrix} \frac{-g_{22}}{g_{21}} & 1 \\ 1 & \frac{-g_{11}}{g_{12}} \end{bmatrix}$$
$$= \begin{bmatrix} g_{12} - \frac{g_{11}g_{22}}{g_{21}} & 0 \\ 0 & g_{21} - \frac{g_{11}g_{22}}{g_{12}} \end{bmatrix} = \begin{bmatrix} G_{eq1} & 0 \\ 0 & G_{eq2} \end{bmatrix} \quad (16)$$

It is inferred that the cross-coupling components of the decoupled TF turn to zero. So it is ensured that one output is affected by one input only. These G_{eq1} and G_{eq2} equivalent decoupled TFs are higher-order TF, so we use the Pade-Approximation method [22] to reduce the second-order system. This reduced-order TF helps to calculate the parameter of the PI-Lead compensator easily. The Bode plot of G_{eq1} and G_{eq2} TFs and their 2nd-order reduced TFs are illustrated in Fig. 10 and 13, respectively. According to the PI-Lead compensator, a closed-loop system is designed.

A. PI-Lead Compensator Design

The frequency response of a well-controlled and stable DC-DC converter should meet the following requirements [23], [24], [25].

1) To get rid of steady-state errors in the output voltage, the gain in the low-frequency region should be high. Also, the dc-dc converter should work well if the gain margin is more than 12dB. At low frequencies, the slope of the frequency response should be less than 20 dB per decade.
2) To make sure that the closed-loop system is stable, the phase margin (PM) should be higher than 45^0. Higher PM improves the transient response, hence decreasing overshoots caused by variations in input voltage and/or load current.
3) The compensated system's bandwidth (or GCF) should be between one-tenth and one-quarter of the switching frequency of the converter.

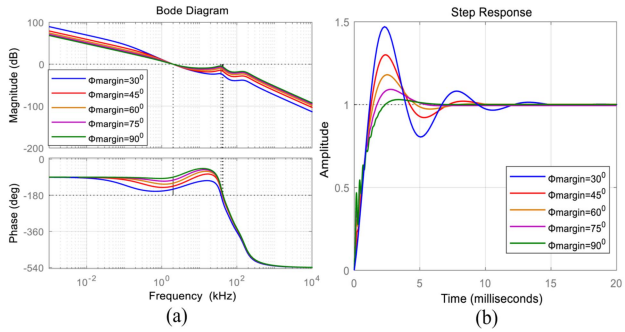

Fig. 9. Compensated G_{eq1} responses with different phase margins at $f_{gc} = 2$ kHz and $f_z = 20$ Hz. (a) Bode plot. (b) Step response.

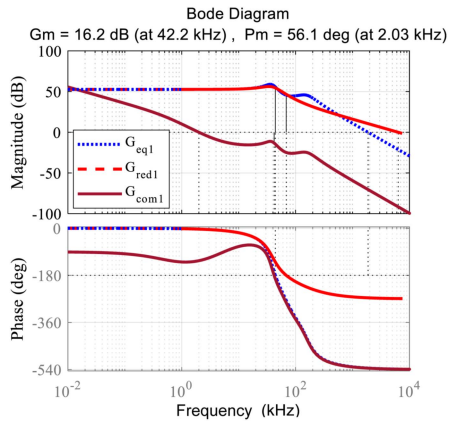

Fig. 10. Comparisons of the compensated and uncompensated systems (G_{eq1}) using the Bode plot at $f_{gc} = 2$ kHz, $f_z = 20$ Hz, and $\emptyset_{margin} = 60^0$.

From [26], It is obvious that the compensator requires an origin pole to get rid of steady-state errors, and it also needs enough positive phase at GCF to increase PM. So, both PI and Lead compensator need to be used together to get these qualities in a single compensator. The PI component of this coupled compensator boosts the gain at low frequency, improving the s steady-state operation of the system. The Lead compensator also aids in providing the required PM at the desired GCF, which improves the system's transient response. It is represented as

$$G_{PI\_Lead} = \left(K_p + \frac{K_I}{s}\right) * \left(K_{Lead}\frac{s+\alpha}{s+\beta}\right)$$
$$= K\frac{\left(1+\frac{s}{\omega_z}\right)(s+\alpha)}{s(s+\beta)} \quad (17)$$

where $\omega_z = {}^{K_I}/_{K_p}$, $K = K_I * K_{Lead}$

To calculate the parameters of the PI-Lead compensator, the pseudocode of the PI-Lead compensator parameter design is given as follows.

PI-Lead compensator parameter design $(K, \omega_z, \alpha, \beta)$ of eq(17)

Begin

Taking system transfer function (G)

$g_{eq} = D * G$

Reduce system order using the Pade approximation method.

Calculating GCF_{sys}, ϕ_{sys}, K_{sys} of the reduced system.

Corner frequency=0.1*GCF_{sys}

Enter the specified PM and GCF of the overall compensated system.

% GCF=0.1*switching frequency, PM= 45^0 %

Calculating K_{sys_PI} and ϕ_{sys_PI} at GCF, of the PI-compensated system.

do

{

PM=PM+1^0, $K_{req} = \frac{1}{K_{sys}}, \phi_{req} = -180^0 - \phi_{sys} + PM$

$K = K_{req}\sqrt{\frac{1+sin\phi_{req}}{1-sin\phi_{req}}}, \alpha = \omega_{gc}\sqrt{\frac{1-sin\phi_{req}}{1+sin\phi_{req}}}, \beta = \omega_{gc}\sqrt{\frac{1+sin\phi_{req}}{1-sin\phi_{req}}}$

}

while ($GM_{com} > 12dB$ && $PM_{com} > 45^0$ of PI-Lead compensator system and step response of PI-Lead compensator system)

end (PI-Lead compensator parameter design)

The frequency and step time responses of compensated G_{eq1} the system with different corner frequencies at constant at f_{gc} = 2 kHz and $\emptyset_{\text{margin}} = 75^0$ are illustrated in Fig. 8(a) and (b), respectively. Similarly, Fig. 9(a) and (b) show the frequency and step time responses of the compensated system $G_{eq1}(s)$with different phase margin and $f_{gc} = 2$ kHz and $f_z = 20$ Hz, respectively. According to requirement and stability conditions, the PI-Lead compensator parameter of G_{eq1} system is designed based on f_{gc} = 2 kHz and $f_z = 20$ Hz and $\emptyset_{margin} = 60^0$. The uncompensated system without reduction (G_{eq1}), the uncompensated system with reduction (G_{red1}) and compensated system (G_{com1}) bode plots are depicted in Fig. 10. The transfer function of PI-Lead compensators for G_{eq1} is

$$G_{pilead1}(s) = \frac{7.621 \times 10^{-2}\, s^2 + 21.3\, s + 540.4}{251.3\, s^2 + 9266\, s} \quad (18)$$

The frequency and step responses of compensated G_{eq2} system with different corner frequencies at constant at $f_{gc} = 2$ kHz and $\emptyset_{margin} = 75^0$ are depicted in Fig. 11(a) and (b), respectively. Similarly, Fig. 12(a) and (b) show the frequency and step time responses of compensated G_{eq2} system with different phase margin and $f_{gc} = 2$ kHz and $f_z = 40$ Hz, respectively. According to requirement and stability conditions, the PI-Lead compensator parameter of G_{eq1} system is designed based on $f_{gc} = 2$ kHz and $f_z = 40$Hz and $\emptyset_{margin} = 60^0$. The uncompensated without reduction (G_{eq2}), uncompensated without reduction (G_{red2}) and compensated system (G_{com2}) bode plots are depicted in Fig. 13.

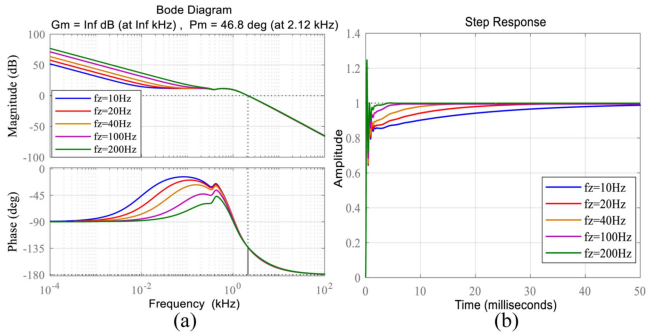

Fig. 11. Compensated G_{eq2} responses with different f_z at $f_{gc} = 2$ kHz and $\emptyset_{margin} = 75^0$. (a) Bode plot. (b) Step Response.

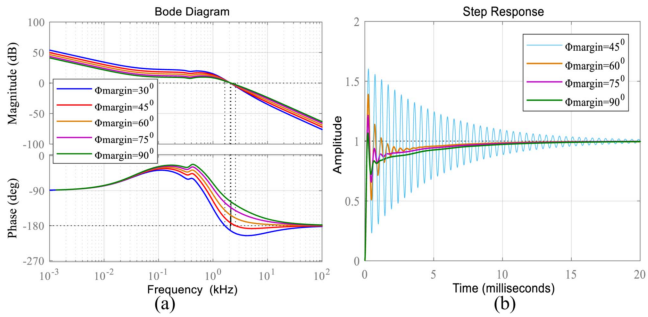

Fig. 12. Compensated G_{eq2} responses with different phase margin at f_{gc} = 2 kHz and $f_z = 40$ Hz. (a) Bode plot. (b) Step response.

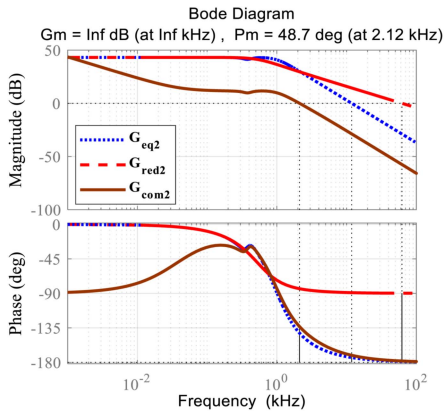

Fig. 13. Comparisons of the compensated and uncompensated systems (G_{eq2}) using the Bode plot at $f_{gc} = 2$ kHz, $f_z = 40$ Hz, and $\emptyset_{margin} = 75^0$.

The transfer function of PI-Lead compensators for G_{eq2} is

$$G_{pilead2}(s) = \frac{9.259\, s^2 + 1.006 \times 10^5\, s + 2.471 \times 10^7}{251.3\, s^2 + 3.738\, e^6\, s} \quad (19)$$

V. Simulation Results

Using numerical simulation in the MATLAB/Simulink environment, the performance of the Cuk SIDOC is examined. A simulation of the converter was carried out using an input voltage of 48 V and a load consisting just of resistors. Table I provides a

TABLE I
EXPERIMENTAL PARAMETER SPECIFICATIONS

Converter Parameters	Value
Input DC voltage (V_g)	48 V
Peak input current and load current (i_{g_max}, i_{01_max} and i_{02_max})	5 A
Operating frequency	20 kHz
Inductance (L_1, L_2, L_3)	333 μH, 830 μH, 480 μH
Capacitance (C_1, C_2, C_3)	10μF, 47μ F and 47μ F
Load (R_1 and R_2)	40Ω and 20Ω
Switch (S_1, S_2)	IRFS4410

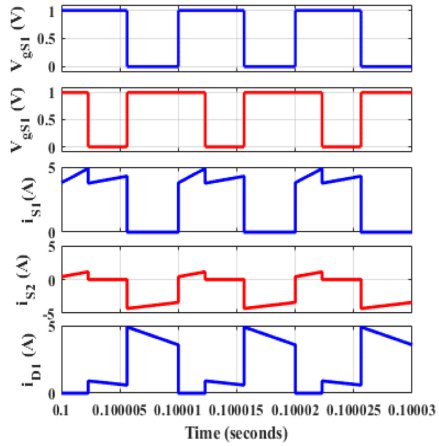

Fig. 14. Steady-state simulation waveforms of the Cuk SIDOC.

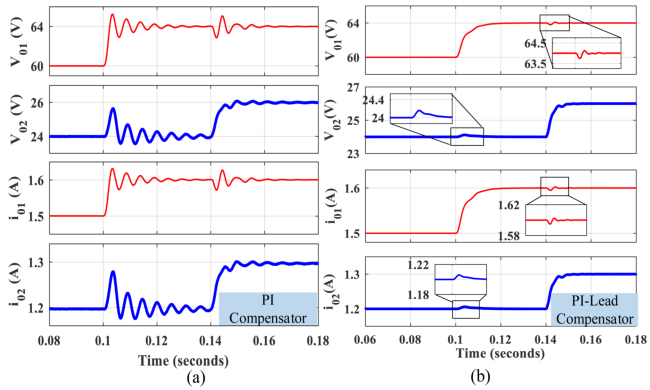

Fig. 15. Cuk SIDOC transient response under variation in output voltage reference: (a) PI compensator and (b) PI-Lead compensator.

summary of the simulation parameters that are utilized. During steady-state operation, V_{ref-1} and V_{ref-2} are set at 60 V and 24 V, respectively. The transient performance of the converter during closed-loop operation is compared with the suggested PI-Lead compensator and PI compensator, which are presented in Figs. 15–17. A time domain comparative analysis (overshoot, undershoot and settling time) is presented in Tables II–IV for both PI-Lead and PI compensator during reference voltage change, load change and input voltage change.

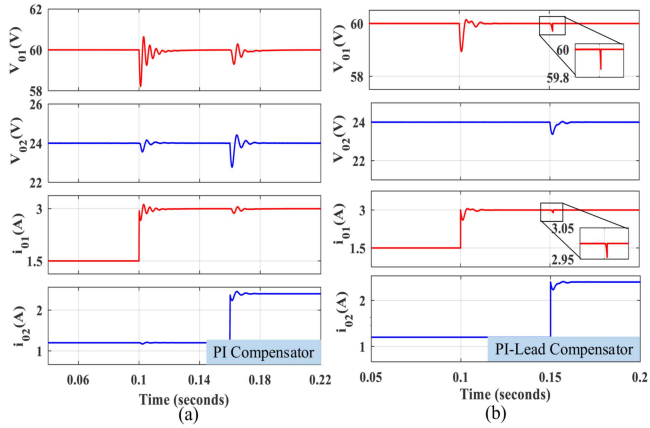

Fig. 16. Cuk SIDOC transient response under Load-1 R_1 variation 50% at 0.1 s as well as Load-2 R_2 variation 50% at 0.16 s using (a) PI controller and (b) PI-Lead compensator.

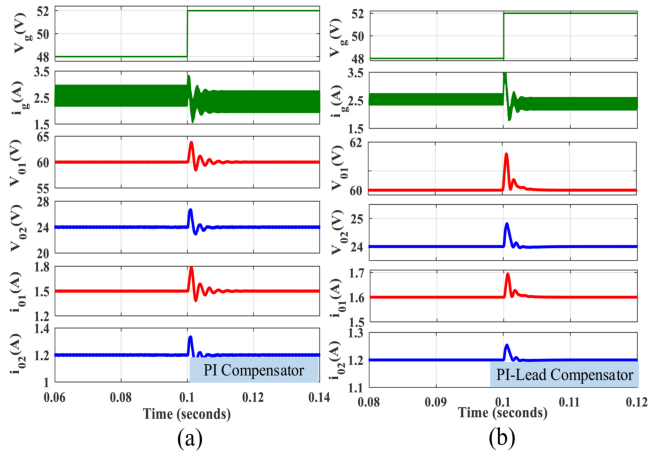

Fig. 17. Transient response with input voltage V_g variation from 48V to 52V at 0.1 s. (a) PI compensator and (b) PI-Lead compensator.

TABLE II
COMPARATIVE PERFORMANCE ANALYSIS BETWEEN PI AND PI-LEAD COMPENSATOR DURING REFERENCE VOLTAGES CHANGE

	Performance Parameters	V_{ref1} change (from 60 V to 64 V at 0.1 s)		V_{ref2} change (from 24 V to 26 V at 0.14 s)	
		PI Fig. 15(a)	PI-Lead Fig. 15(b)	PI Fig. 15(a)	PI-Lead Fig. 15(b)
V_{01}	Settling time	30 ms	10 ms	30 ms	12 ms
	Overshoot	2.1%	0%	2.18%	0.4 %
V_{02}	Settling time	40 ms	10 ms	40 ms	12 ms
	Overshoot	5.5%	1.1%	0.2%	0%

A. Verification of Steady-State Performance

At steady-state, switch voltages and currents are illustrated in Fig. 14. In addition, it has been found that both V_{01} and V_{02} are capable of tracking their respective reference voltages with voltage ripples that are less than 2% with ΔV_{01}= 40 mV and ΔV_{02}= 20 mV.

TABLE III
COMPARATIVE PERFORMANCE ANALYSIS BETWEEN PI AND PI-LEAD COMPENSATOR DURING LOAD CHANGE

	Performance Parameters	R_1 change (from 40Ω to 20Ω)		R_2 change (from 20Ω to 10Ω)	
		PI Fig. 16(a)	PI-Lead Fig. 16(b)	PI Fig. 16(a)	PI-Lead Fig. 16(b)
V_{01}	Settling time	22 ms	10 ms	15 ms	2 ms
	Undershoot	3.33%	1.6%	1.5%	0.03%
	Index1 (self)	0.0166	0.008	-	-
	Index1 (cross)	-	-	0.0075	0.00015
V_{02}	Settling time	12 ms	2 ms	25 ms	12 ms
	Undershoot	2.2%	1.1%	6.66%	2.5%
	Index1 (self)	-	-	0.0333	0.0125
	Index1 (cross)	0.011	0.0055	-	-

TABLE IV
COMPARATIVE PERFORMANCE ANALYSIS BETWEEN PI AND PI-LEAD COMPENSATOR DURING INPUT VOLTAGE CHANGE

	Performance Parameters	Input voltage V_g change (from 48 V to 52 V at 0.1 s)	
		PI Fig. 17(a)	PI-Lead Fig. 17(b)
V_{01}	Settling time	16 ms	8 ms
	Overshoot	6.66%	2.5%
V_{02}	Settling time	10 ms	6 ms
	Overshoot	12.5%	3.33%
i_g	Settling time	12 ms	6 ms
	Overshoot	1 A	1 A

B. Verification of Cross-Coupling Effect

The robustness of the proposed PI-Lead compensator on the Cuk SIDOC has been verified by changing the reference voltage. The simulation results of output voltage and current are illustrated in Fig. 15, showing the performance of Cuk SIDOC with PI-Lead compensator when the reference signal of output voltage V_{ref1} (from 60 V to 64 V at 0.1 s) and V_{ref2} (from 24 V to 26 V at 0.14 s) changed. In PI-Lead compensator, the output voltage V_{01} tracks the V_{ref1} and settles in 10 ms. The change in V_{ref1} resulted in a negligible change in V_{02}. In this instance, V_{02} with an overshoot of 200 mV, as illustrated in Fig. 15(a). Similarly, the change in $V_{ref2,}$ the output voltage V_{01} and V_{02} follow the reference voltage and settle in 12ms. Moreover, variations in V_{ref2} have almost minimal effect on V_{01} with an overshoot of 200 mV, as illustrated in Fig. 15. As a result, the suggested control method can eradicate the CC effect in the Cuk SIDOC, as was covered in Fig. 5. In comparison to the PI controller used in the Cuk SIDOC, the PI-Lead has a shorter amount of time required to converge while also exhibiting a slight overshoot. The performance parameters with PI and PI-Lead compensator in Cuk SIDOC, when the reference voltage V_{ref1} and V_{ref2} changed, are summarized in Table II.

C. Verification of Cross-Regulation Effect

The converter has been verified by changing the output load, and the performance of both PI and PI-Lead compensator has been recorded and presented in Fig. 16(a) and (b), respectively. In these circumstances, the output load resistance of port-1 is changed from 40 ohms to 20 ohms in 0.1 seconds, while the output load resistance of port-2 is changed from 20 ohms to 10 ohms in 0.15 seconds. In the PI-Lead compensator, the change in load on port-1, the output voltage $V_{01,}$ dropped by 1 V and settled within 10 ms, as illustrated in Fig. 16(b). The change in load at port 1 has an insignificant impact on the voltage and current at port 2. In a similar fashion, the change in load at port-2 causes the output voltage V_{02} to drop by 0.6 V and settle at 12 ms. Nevertheless, the change in load at port 2 has only a marginal impact on the voltage and current at port 1, which is quite negligible.

The performance parameters with the PI and PI-Lead compensator of the Cuk SIDOC are summarized in Table III when the load changes. The voltage drops are quantified as listed for Index 1 and Index 2 in Table III; compared to the PI controller, the PI-Lead controller provides better performance. The quantitative value of Index 1 and Index 2 provided by the PI-Lead controller is smaller than the PI controller, and the transient settling time of the voltage waveform by the PI-Lead compensator is much faster.

$$Index1\ (self) = \frac{\%\ of\ load\ change * \Delta v_0\ (same\ channel)}{V_{rated}} \tag{20}$$

$$Index2\ (cross) = \frac{\%\ of\ load\ change * \Delta v_0\ (other\ channel)}{V_{rated}} \tag{21}$$

D. Verification in Variations in the Input Voltage

The robustness of the proposed PI-Lead compensator over Cuk SIDOC has been verified by changing the input voltage. Before the variation, the converter is operating under a steady-state condition with $V_g = 48$ V, $i_{01} = 1.5$ A and $i_{02} = 1.2$ A, $V_{ref1} = 60$ V, $V_{ref2} = 24$ V. The performance of the converter with a PI compensator and a PI-Lead compensator is illustrated in Fig. 17(a) and (b), respectively, when the input voltage V_g changes from 48 V to 52 V at 0.1 s.

The output voltages of the PI and PI-Lead compensators follow their respective reference voltages, but PI-Lead compensator has minimum overshoot and settles within a millisecond. In PI-Lead compensator, the overshoot in V_{01} and V_{02} is found to be 1.5 Volt and 0.8 Volt, respectively. The time-domain performance parameters (settling time and overshoot) with the PI and PI-Lead Compensator of the converter are summarized in Table IV. It is observable that PI-Lead Compensator has a slightly better performance than the PI compensator.

VI. EXPERIMENTAL VALIDATION

In the laboratory, a hardware prototype of the Cuk SIDOC is developed to validate the performance of the proposed control algorithm, which is presented in Fig. 18. In this article, a MOSFET-based load change technique is used in order to achieve robustness against variations in load. Fig. 19 illustrates the converter's performance when it is operating in a steady condition.

The result that was obtained illustrates the switching pulses of both switches, as well as the voltage that is present across both switches and the inductor current $(i_{L1},\ i_{L2},\ i_{L3})$. The findings of the experiments lend support to the theoretical analysis that is illustrated in Fig. 3. Changing the load and reference voltage of

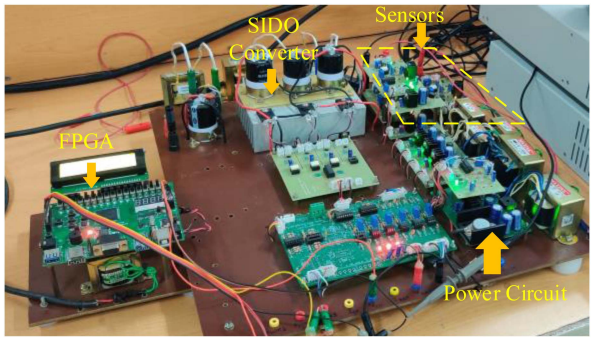

Fig. 18. Implemented laboratory prototype of SIDOC.

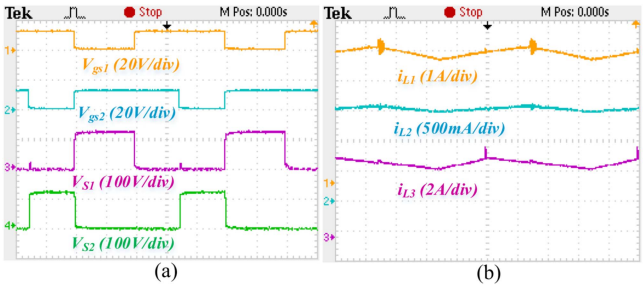

Fig. 19. Steady-state waveforms of (a) Gate signals D_{S1} and D_{S2} and the switch voltages V_{S1} and V_{S2}; (b) inductor currents i_{L1}, i_{L2}, i_{L3}.

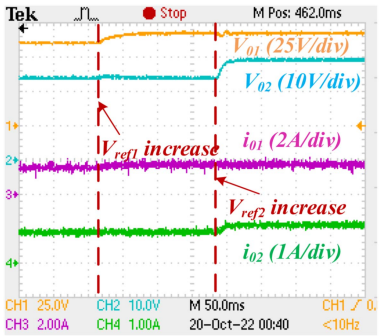

Fig. 20. Transient performances of the PI-Lead Compensator-based Cuk SIDOC with V_{ref1} change from 60V to 64V and V_{ref2} change from 24V to 28V.

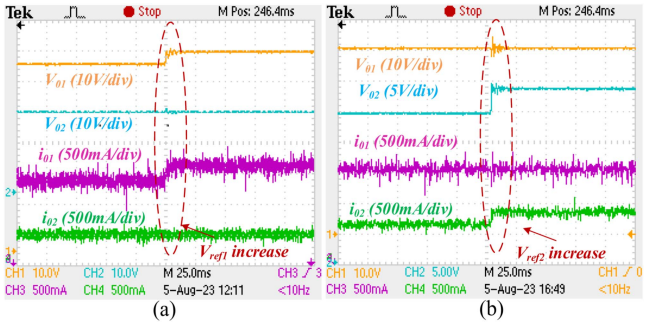

Fig. 21. Transient performances of the PI controller-based Cuk SIDOC with (a) V_{ref1} change from 60V to 64V and (b) V_{ref2} change from 24V to 28V.

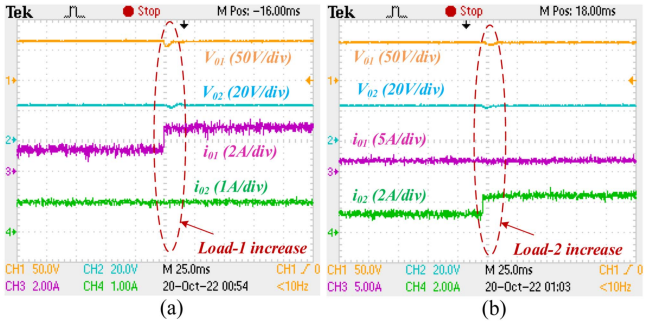

Fig. 22. Dynamic response of the PI-Lead compensator based Cuk SIDOC. (a) Load-1 change from 40 Ω to 20 Ω. (b) Load-2 changes from 20 Ω to 10 Ω.

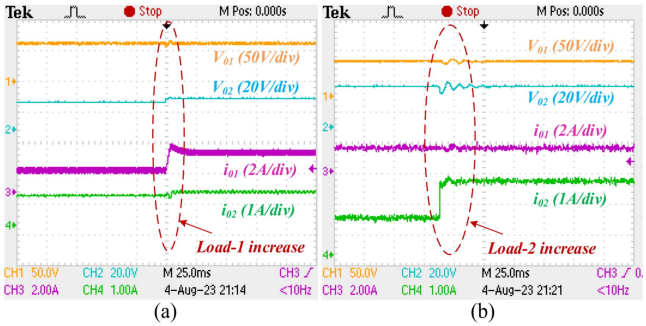

Fig. 23. Dynamic response of the PI controller-based Cuk SIDOC. (a) Load-1 change from 40 Ω to 20 Ω. (b) Load-2 changes from 20 Ω to 10 Ω.

the two ports is one way to test the dynamic performance of the converter. The findings indicate that two different voltages and currents are obtained from the output port. The performance of the converter is illustrated in Fig. 20 in response to a change in the reference voltage at port-1 from 60 V to 64 V. The results indicate that there is a correlation between the change in reference voltage and the port-1 output voltage, which stabilizes after 30 ms. The corresponding port current, denoted by i_{01}, will change as a result, as shown in Fig. 20. There is hardly any change discernible in the magnitude of the port-2 voltage and current readings. In a similar vein, the experimental findings that were obtained with a modification in the reference voltage for port-2 are presented in Fig. 20. It is clear from looking at Fig. 20 that the alterations in the reference voltage of port-2 have minimal impact on the voltage and current of port-1. As a result, the influence of CC that is present in the converter is nullified by the control technique that was proposed. In Fig. 21 shows the reference voltage change with the PI controller where the PI controller can't nullify the CC effect.

Fig. 22 illustrates how the converter's dynamic performance responds to load variations. The change in load on port-1 causes the current through port-1 to increase from 1.5 A to 3 A, but the current through port-2 remains the same at 1.2 A. The two-port voltage transients settle down very rapidly whenever there is a change in the load. Similarly, when i_{02} goes from 1.2 A to 2.4 A, the current flowing via port-1 does not change; it remains at 1.5 A. The voltage at the output port, measured as V_{01} and V_{02}, is subject to transients but quickly returns to its steady state. As a result, the CR effect is diminished by implementing the PI-Lead compensator approach. But in the PI controller case, the CR effect is not diminished, which is shown in Fig. 23. The

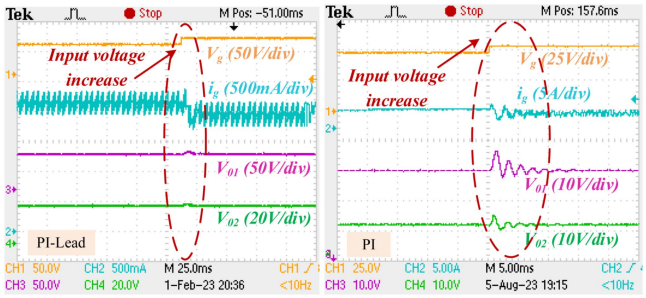

Fig. 24. Dynamic response of the (a) PI-Lead and (b) PI Compensator-based SIDOC with input voltage change from 48 V to 52 V.

performance of the converter in both PI-Lead and PI controller are illustrated in Fig. 24 in response to an increase in the input voltage V_g from 48V to 52V. In the PI-Lead compensator, the output voltages are linearly proportional to their respective reference voltages, with only a slight overshoot of two output voltages, but in PI controller there is more oscillation than in the PI-Lead compensator, which is shown in Fig. 24(b).

VII. Conclusion

In this article, a new method is proposed for decoupling the Cuk SIDOC. Earlier, the presence of the coupled capacitor in this converter has created problems like CC and CR. Therefore, a detailed analysis describes that both outputs can be separated by designing a decoupler that nullifies the CR and CC problems of the SIDOC. Furthermore, the effect of decoupling is investigated on the closed-loop TFs of load regulation and audio-susceptibility. It shows that the sixth-order TFs of audio susceptibility and self-regulation of Cuk SIDOC get reduced to that of the second-order TFs of a SISO Cuk converter. While designing the compensator, it is possible to meet the performance goals of cross-coupling, self-regulation, and cross-regulation by giving the compensator a high gain. On the other hand, a high compensator gain results in a greater crossover frequency, which causes the system to become unstable. Therefore, the compensator is developed with both cross-coupling and stability as potential tradeoff constraints. Considering these conditions, a decoupled-based PI-Lead compensator is designed. Thus, this analysis may help in developing other multiport converters with suitable modifications for applications like electric vehicles and residential power supplies.

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