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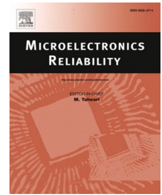

Assessing the reliability of SiC MOSFET through inverter-like accelerated test vs. power cycling test

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A R T I C L E I N F O

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A B S T R A C T

Silicon carbide (SiC) MOSFETs are known for their superior performance compared to traditional silicon devices, making them well-suited for a wide range of applications in power electronics. However, there is a lack of long-term reliability studies for SiC MOSFETs under real-world operating conditions. This article introduces an innovative inverter-like accelerated test (IAT) and compares it with the standard power cycling test (PCT) to thoroughly assess the degradation mechanisms and reliability of SiC MOSFETs. The IAT is designed to replicate the operational conditions of an inverter, providing a more realistic evaluation of the long-term performance of the SiC MOSFET. There are some differences in the principles of these two accelerated tests (ATs). The paper provides detailed insights into these differences and the methodologies used, including the test bench design and junction temperature estimation, and presents the experimental results. The findings highlight significant differences in the degradation behavior observed under IAT and PCT conditions and the lifetime evaluation, underscoring the necessity for realistic testing protocols to ensure reliable lifetime predictions for SiC MOSFETs in practical applications.

1. Introduction

Silicon carbide (SiC) MOSFETs offer significant advantages over traditional Si devices in power electronics systems, including higher blocking voltage, faster switching speeds, greater power handling capacity, and improved thermal conductivity. These features make SiC MOSFETs highly desirable for high-efficiency and high-power-density power converters [1–5]. However, due to the relative novelty of this technology, limited field data regarding the long-term reliability of SiC MOSFETs is available. Additionally, a recent survey has indicated that power semiconductor failures represent over half of all converter failures in the industry [6]. Therefore, it is crucial to conduct thorough evaluations of the long-term reliability of the SiC MOSFET to facilitate improvements and minimize destructive failures in these devices [1]. When assessing the reliability of SiC MOSFETs in the industry, ATs play a crucial role. The results of these tests provide a basis for estimating the lifetime of the product in the design phase. Standard ATs for devices typically involve high-temperature gate bias testing for gate reliability, high-temperature reverse bias, and high-voltage high-humidity high-temperature reverse bias testing for chip edge termination blocking capability, and Power Cycling Test (PCT) for packaging reliability [7,8]. However, these standardized tests are mainly conducted under simplified and controlled conditions, which may not fully replicate the actual operation profiles of the devices in power converters. For example, in PCT, the impact of switching stress on power devices is often overlooked as the applied drain voltage is much lower than in normal operating conditions. Similarly, high voltage bias tests involve applying a constant static electrical stress to gate oxide without any current flow through the power devices during the aging process. In reality, devices are installed in active power electronic converters, and their degradation mechanism under practical operating conditions is highly complex [9]. Moreover, the standard tests for the reliability of SiC MOSFETs typically focus on specific degradation mechanisms. However, the conditions experienced by SiC MOSFETs in real converters involve a combination of factors such as high average junction temperature, high-frequency temperature fluctuations, thermal cycling stress, and voltage bias stress during PWM cycles. Additionally, the static bias test may lead to reliability evaluation results that deviate from practical conditions. Therefore, the current standard tests may not adequately assess the degradation phenomena and mechanisms of power devices under actual operating conditions [9].

Numerous studies have been conducted on advanced accelerated

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tests, primarily focusing on full-bridge and half-bridge converters, yet often neglect the presence of other components within the circuit [9–16]. In [9], a PFC converter was developed to study gate oxide and package degradation. However, the setup is simplified and only accounts for forward conduction, missing the real application conditions and the complexity of a converter. The study in [13] presents an AC power aging test utilizing a three-phase converter-to-load topology, along with an apparatus and methodology for advanced accelerated power cycling of power modules under realistic conditions. However, this approach relies heavily on calibration tools, such as infrared cameras and control software, to measure junction temperature accurately, which increases both complexity and cost. The research in [14] indicates no significant difference in failure modes between DC and PWM PCTs. Nevertheless, as highlighted in [15], while differences in degradation between DC and AC PCTs have been observed, further investigation is warranted since this comparative study remains relatively nascent. Additionally, [16] implemented a rapid PCT on a power module, with load and cooling durations of less than 1 s per cycle, which resulted in a notable concentration of voids forming exclusively in the central region of the solder layer. However, this study evaluates the power device in isolation, neglecting the interactions with other circuit components. Which limits its ability to replicate real-world conditions and thermal behaviors in converter applications.

To accurately assess the reliability of SiC MOSFETs under real application conditions, an accelerated test using a converter rather than a simplified setup is required. The H-ANPC inverter was selected for its ability to replicate complex, real-world operations, such as high-frequency switching and varied conduction modes, making it ideal for providing a realistic testing environment. Recognized as one of the popular inverter topologies for high-efficiency applications, especially in three-phase PV inverters and bi-directional systems like battery storage, the H-ANPC offers superior efficiency, flexible modulation, and the ability to handle high-voltage applications up to 1500 V [17]. Despite its popularity, comprehensive studies on the reliability of this inverter topology remain limited, which further supports its selection for this investigation.

In this article, an Inverter-like Accelerated Test (IAT) is proposed and compared with the standard PCT to evaluate the degradation phenomena, reliability, and lifetime of SiC MOSFETs. The PCT, a widely used method, is essential for evaluating device lifetime and degradation mechanisms, providing valuable guidance for lifetime estimation during product design [18]. Significant differences between the PCT and IAT are elaborated in this article to highlight the value of realistic testing protocols.

The article is structured as follows: Section 2 covers the operating principles of the PCT and IAT and test bench design, while Section 3 details the junction temperature estimation method utilized. Section 4 provides insight into the lifetime estimation of the SiC MOSFETs. In conclusion, Section 5 will showcase the experimental hardware results and provide an in-depth discussion. Following that, Section 6 will include concluding remarks.

2. Accelerated Tests (ATs)

This article discusses two distinct ATs that are conducted to assess the reliability and lifetime evaluation of the SiC MOSFET by subjecting it to harsh thermo-mechanical stresses and accelerated testing conditions. During the tests, each device under test (DUT), which are SiC MOSFETs in this case, experiences cyclic changes in its junction temperature (T_j) and internal temperature distribution due to self-heating from conduction and switching losses, as well as active cooling from a dedicated cooling system. The mismatch in thermal expansion coefficients of the various material layers within the package results in the development of thermomechanical stresses, particularly in regions with steep temperature gradients [19].

According to failure criteria, an increase of 5 % in the conduction voltage (V_{DS_ON}) or an increase of 15 % in thermal resistance (R_{DS_ON}) is used to detect failures in the conductive path, such as wire bond or the chip solder layer, respectively. However, these parameters are partially correlated; for example, a higher R_{DS_ON} leads to a higher junction temperature, causing an increase in V_{DS_ON}, which in turn amplifies losses and results in a more pronounced temperature rise [19].

The ATs are described as follows:

1. PCT: In this test, the device is subjected to accelerated thermal cycling conditions. The device undergoes cyclic changes in the junction temperature within the package due to its conduction loss while an active cooling system is operating. The conduction time (T_{on}) and cooling time (T_{off}) last in the range of a few seconds. Also, the input voltage remains low, whereas the DC current (I_S) approaches the peak range of the device due to the temperature increase caused by conduction loss.
2. IAT: In this test, the device is operated within an inverter. The device experiences temperature cycling due to conduction and switching losses and an external cooling system. The input voltage reaches the nominal value of the inverter operation, and the device current approaches the peak value of its own. The aim of this test is to ensure that the device experiences accelerated operation conditions for the inverter. Additionally, the PCT primarily functions at the component level, whereas IAT monitors device degradation during the inverter operation, taking into account the presence and influence of other components and maintaining the same temperature profile as the inverter. This approach allows for the detection of different rates of failure compared to PCT, and it is also a more realistic AT condition.

Although it is possible to operate PCT and IAT in different ways, there are challenges in running PCT similarly to IAT or vice versa. For example, achieving a higher frequency of junction temperature fluctuation in PCT requires a high-speed heating and cooling system, which is extremely difficult to implement. Additionally, the temperature profile of the device in the inverter significantly impacts its lifetime. To operate PCT with the exact temperature profile of the inverter, a more complex circuit than the inverter would be necessary. On the other hand, the RMS current of the device in PCT is significantly lower than in IAT. The load current must be reduced to achieve the same RMS current as the PCT in IAT, which substantially lowers the junction temperature of the device. As a result, the IAT takes much longer to show any degradation. By comparing the degradation rates in PCT and IAT, this article provides information that is crucial for more realistically predicting the lifetime of the device and optimizing the design and operation of inverters. In addition, several necessary steps need to be considered to develop a device model, including circuit design, selection of operating conditions, duration of tests, reliability assessment, and lifetime evaluation, which will be discussed in the following sections.

2.1. PCT principles and test bench

According to the previous discussion, the first step is circuit design and selecting the type of device. In this article, a discrete SiC MOSFET in TO-247 packages is used. A circuit consisting of a DC power supply, protections, and an RL load for various PCTs is then developed. The circuit diagram, which is a full bridge topology, and the temperature profile of the PCT are shown in Fig. 1 and Fig. 2, respectively. There are several advantages to using a full bridge inverter over other circuits, such as its simple design and the requirement for a minimum amount of input energy [18]. Additionally, forced air cooling is provided throughout the duration of the test. The primary purpose of the testing circuit is to conduct current through the SiC MOSFETs, causing the junction temperature to increase to its maximum level. Subsequently, the power is turned off until the temperature is reduced to a minimum value.

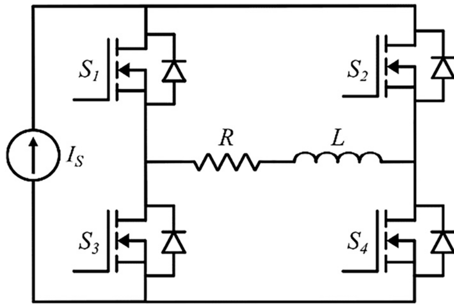


Fig. 1. Circuit diagram of H-bridge configuration.

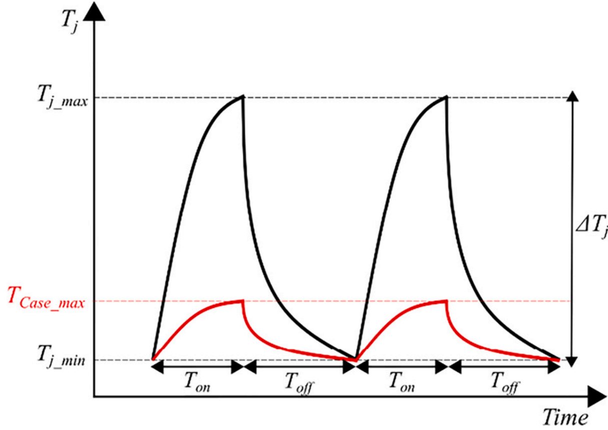


Fig. 2. The junction temperature profile of the DUT under PCT.

2.2. IAT principles and test bench

In this article, the IAT setup is an H-ANPC inverter that employs the same SiC MOSFET as the PCT. However, the circuit presents increased complexity. As illustrated in Fig. 3, the H-ANPC inverter comprises a DC power supply, DC link capacitors, four Si IGBTs, two SiC MOSFETs, snubber capacitors and resistors, and an LC filter. While the SiC MOSFETs, S_5 and S_6, operate at high frequency, the Si IGBTs, S_1-S_4, function at line frequency. The modes and operation of the H-ANPC inverter are elaborated in [20] as hybrid topology B. Due to the modulation of the H-ANPC inverter, the SiC MOSFETs and their anti-parallel diodes are conducted in different modes, influencing the lifetime of the SiC MOSFETs, as detailed in subsequent sections. In the IAT setup, the cooling mechanism relies on the desired junction temperature. Forced air cooling is implemented during experimentation; however, the number and power of the fans are adjusted based on desired stress conditions. It is noted here that each is equipped with a heatsink to manage thermal connectivity and isolation over the heatsink effectively.

As depicted in Fig. 4, the temperature profile of the SiC MOSFET tracks the load current within half a cycle. Additionally, temperature elevation occurs during diode conduction while the SiC MOSFET is turned off (T_{off} region in Fig. 4), further affecting the lifetime of the SiC MOSFET. Another notable distinction between the PCT and IAT temperature profiles is illustrated in Fig. 4, where the ripple in junction temperature is evident. This ripple effect stems from the SiC MOSFET switching action and influences the overall junction temperature dynamics. Along the current path, each SiC MOSFET in the IAT setup is influenced by other components, such as snubber filters and Si IGBTs.

3. Online junction temperature estimation

Estimating junction temperature is essential for managing the thermal stress of the SiC MOSFETs under different IAT test conditions and determining the necessary cooling actions to maintain these conditions. Regular monitoring of the junction temperature during testing is critical to identify the end point of the test, which occurs due to device degradation. This process also enables online monitoring of degradation throughout the test duration. Moreover, monitoring the junction temperature helps in issuing alerts if the temperature increase in one device could potentially affect other devices and components. For SiC MOSFETs, the R_{DS_ON}, which serves as an indicator of failure and is influenced by the junction temperature. Consequently, degradation-related changes in R_{DS_ON}, are typically reflected by a substantial rise in junction temperature, signaling device failure.

Previously, external circuitry was built to enable the measurement of on-state voltages that are typically much smaller in magnitude than the blocking voltage of the device [21–23]. However, this requires additional circuitry and has the potential to interrupt the normal working of the device, and with increased device count, this leads to converter size and cost burden. In contrast, this article introduces a real-time method that directly measures the electrothermal data of the device, facilitating rapid estimation of junction temperature. The fundamental equation

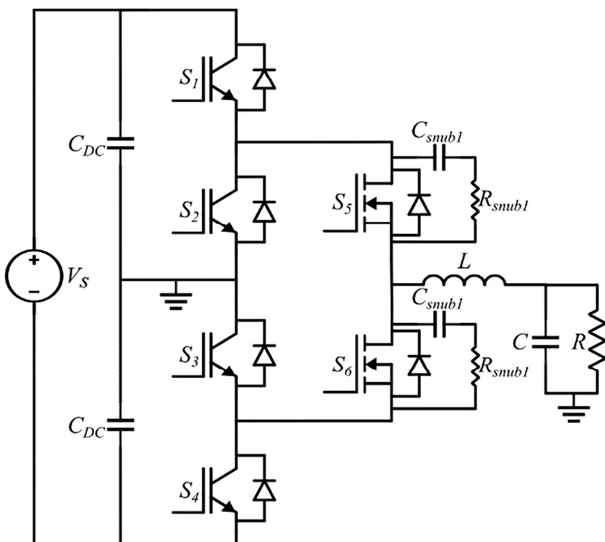


Fig. 3. The H-ANPC inverter schematic.

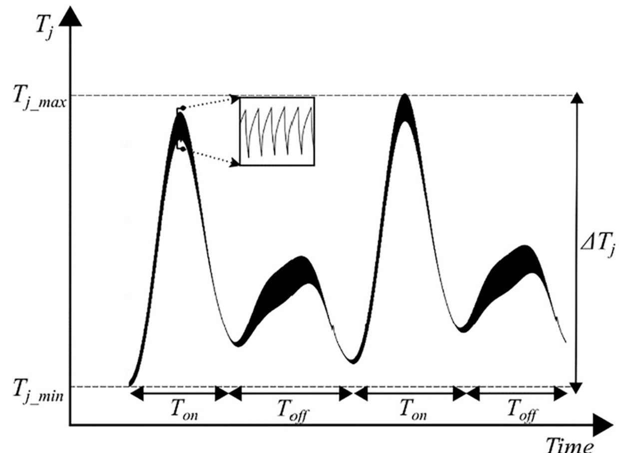


Fig. 4. The junction temperature profile of the DUT under IAT.

governing the junction temperature estimation is given by

$$T_j = Z_{th(j-c)}.P_{loss} + T_C \tag{1}$$

where, $Z_{th(j-c)}$ is the thermal impedance from junction to case, P_{loss} is the device power loss, and T_C is the case temperature. Foster thermal models are used to represent the thermal network. The dynamic thermal impedance parameters for the device thermal model are derived from the thermal impedance plot given in its datasheet. The case temperature is measured by placing thermocouples at the case of the device where it is in contact with the heatsink. The power loss calculation is achieved based on the data from the oscilloscope. This section further discusses the methodology used to estimate junction temperature in real-time and detect device degradation.

3.1. Power loss calculation

In the IAT setup, it is essential to account for both conduction and switching losses due to the high-frequency switching of the H-ANPC inverter. This necessitates a comprehensive measurement setup capable of capturing current and voltage data of the devices over one line cycle, with sufficient bandwidth to accurately record device switching information. For this purpose, differential voltage probes are used to measure the low on-state voltage across the DUT, while a high-resolution oscilloscope captures this data. A voltage probe with a 600 V range, combined with the 16-bit ADC of the oscilloscope, achieves a resolution of 9.1 mV, which is suitable for detecting on-state voltages between 0 and 10 V. Moreover, a Rogowski current probe is wrapped around the leg of the device under test to measure the current through the device. However, since using multiple such probes for all the devices is both expensive and uses up multiple channels on the oscilloscope, a single high-bandwidth current probe is instead used to measure the current through the output inductor. Given the knowledge of the switching states, this inductor current measurement can determine the current for any device in the H-ANPC inverter. The Rogowski coil is then utilized to verify the accuracy of the device current derived from the inductor current measurements and calibrate the readings used for junction temperature estimation.

The voltage and current data communication is achieved using TCP/IP protocol over a local area network, connecting the oscilloscope to a remote PC programmed for regular trigger-based data transmission. This instantaneous data is processed to assess the discrete averaged power loss to estimate the dynamic thermal variation in SiC MOSFETs. For this, the data collected on the remote PC, along with the case temperature data, is passed through a MATLAB function that generates the dynamic plot for the junction temperature. The conduction loss of the device at the nth data sample is given by

$$P_{cond}(n) = i_L(n) \bullet v_{DS}(n) \bullet 1_{v_{DS.n<v_{lim}}} \tag{2}$$

where, $1_{v_{DS.n<v_{lim}}}$ indicates a function that equals 1 when $v_{DS.n<v_{lim}}$ and 0 otherwise. Here v_{lim} is the maximum on-state voltage of the device at the maximum current and temperature that the device can handle (~ 10 V). In (2) $i_L(n)$, and $v_{DS}(n)$ are the inductor current and voltage, respectively, at the nth data sample. Additionally, periodically, zoomed-in waveforms are used to capture the switching transients. Switching loss is calculated by integrating the current and voltage for the switching on and off time. This, along with conduction loss averaged over each switching cycle is used to obtain the average device power loss during each switching period, and is given by

$$P_{loss}(k) = \sum_{n=0}^{m-1} P_{cond}((k-1)m+n+1) + \bullet \Delta t_k \left(\sum_{n=1}^{L_{on}-1} i_{DS}(n) \bullet v_{DS}(n) + \sum_{n=1}^{L_{off}-1} i_{DS}(n) \bullet v_{DS}(n) \right) \bullet f_{sw}. \tag{3}$$

In (3), k is the number of switching cycles in the line cycle, and ranges from 1 to $\lfloor \frac{N}{m} \rfloor$. For the oscilloscope Sampling Rate (SR), line frequency of the test as f_l and switching frequency f_{sw}, $N = SR/f_l$ is the record length of the oscilloscope and $m = SR/f_{sw}$. The switching loss is measured by zoomed-in waveform centered at the turn-on and turn-off duration, and thus L_{on} and L_{off} are the oscilloscope length during the tune-on and turn-off duration.

3.2. Device degradation detection

Considering the sinusoidal operation of the H-ANPC inverter, R_{DS_ON} of the SiC MOSFETs exhibits a cyclic pattern corresponding to the operating condition of the power cycle. Therefore, the oscilloscope measurement for the device current and voltage during the pth oscilloscope reading is used to calculate R_{DS_ON} those accounts for varying power conditions as follows:

$$R_{DS_ON}(p) = \sqrt{\frac{1}{T}\left(\sum_{N}\left(\frac{v_{DS}(n) \bullet 1_{V_{ds.n<v_{lim}}}}{i_L(n)} \bullet 1_{I_L \neq 0}\right)^2\right)} \tag{4}$$

where, $1_{I_L \neq 0}$ indicates a function that equals 1 when $I_L \neq 0$ and 0 otherwise. Since R_{DS_ON} is indicative of device degradation, which affects junction temperature, IAT tests are conducted with a sufficient margin to accommodate increases in R_{DS_ON} without causing overheating and premature device failure. This is verified through offline measurements with a Keithley device characterizer at both the beginning and end of the test, confirming the increase in this degradation parameter at room temperature.

Fig. 5 presents a flowchart depicting the junction temperature estimation process. Initially, inverter test parameters such as input voltage (V_{in}), output current (i_{out}), and external cooling temperature (T_{cool}) are adjusted to achieve the desired maximum junction temperature (T_{j_set}) for the SiC MOSFETs under test. In this test, T_{cool} is the cooling provided to achieve the desired case temperature through adjustments in fan speed and power. Once the maximum junction temperature (T_{j_max}) reaches the set value (T_{j_set}), adjustments to the input parameters are halted, and continuous monitoring of R_{DS_ON} is initiated. This real-time

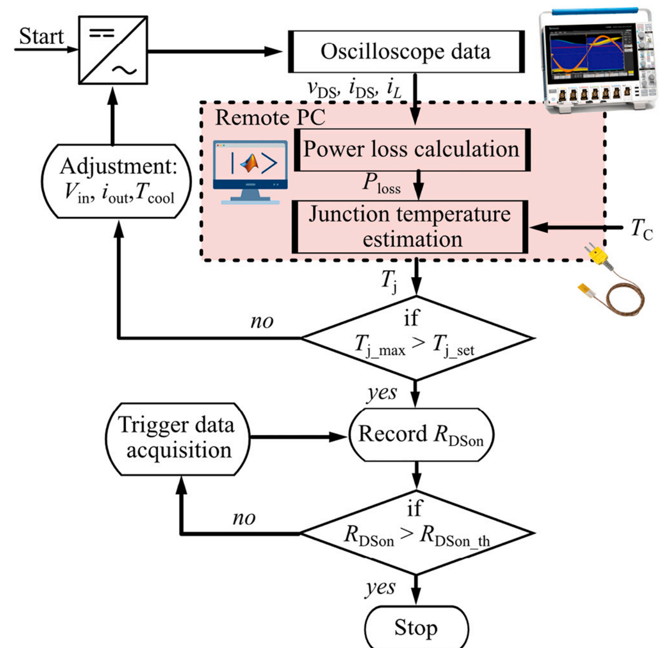


Fig. 5. Flowchart for device temperature estimation and processing.

R_{DS_ON} data, recorded at regular intervals, tracks the progression of device degradation. The IAT test is concluded once the change in R_{DS_ON} reaches its predefined threshold.

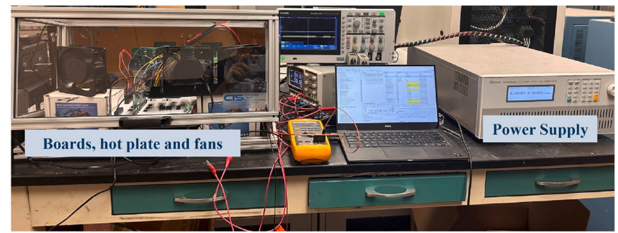
4. Experimental results

This section details the experimental setups and results for the PCT and IAT. Measurements for each AT are captured using Tektronix TBS2000B (for PCT) and MSO46 (for IAT) oscilloscopes. The power supply and Digital Signal Processor (DSP) controller are KEPCO KLN 1500-30E and Texas Instruments TMS320F28379D, respectively. Device case temperatures are recorded with Fluke 87-V multimeters. The ATs were intermittently shut down, and the DUTs were extracted from the converters. As illustrated in Fig. 6, in a separate set of experiments, the variation in electrical parameters is measured offline using Keithley instruments (models 8010, 2636B, 2651A, and 2657A). Subsequently, the DUTs are assessed to examine the impact of degradation on their electrical performance. The extracted electrical parameters in this article are R_{DS_ON}, output characteristics, transfer characteristics, and breakdown voltage. The comparative analysis of all samples revealed consistent variations in the aging parameters. This article focuses on showcasing a selection of representative experimental results.

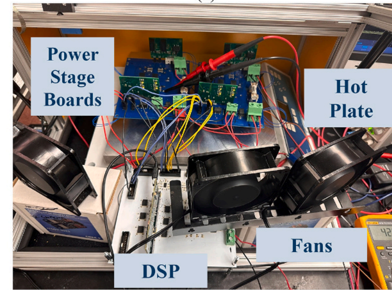
4.1. PCT experimental setup and results

As mentioned, the PCT test bench is a full bridge topology that allows four samples of each AT test condition to be run simultaneously. Fig. 7 illustrates the experimental PCT setup. As DUTs, at least a total of four SiC MOSFETs are used for each PCT. In the PCT, the selected DUTs have ratings of 1200 V/10 A. As a result, a summary of the operation and testing parameters of the four PCTs is provided in Table 1. The experimental waveform for one of the PCTs is depicted in Fig. 8 to illustrate the operation of the converter. As indicated in Fig. 1, devices S_1 and S_4 are conducting in the same direction, whereas S_2 and S_3 are operating in the opposite direction. Additionally, there is a delay between each conduction to prevent any short-circuit occurrences.

Fig. 6. Keithley instruments to characterize DUTs.



(a)



(b)

Fig. 7. (a) The PCT experimental hardware and (b) a zoomed-in view of the enclosure.

Table 1
Summary of the PCT parameters for SiC MOSFET.

PCT #	I (A)	t_{on}/t_{off} (s)	ΔT_j (°C)	T_{j-min} (°C)	$N_{f,pct}$
1	10	0.5/10	125	42	2850
2	9	1.75/10	76	48	7963
3	8	2.2/10	71	62	15,019
4	8	2.2/10	58	55	34,210

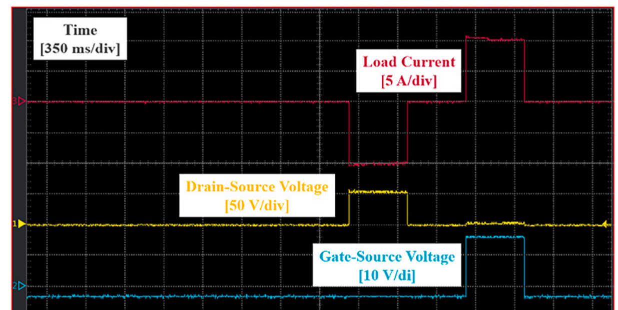
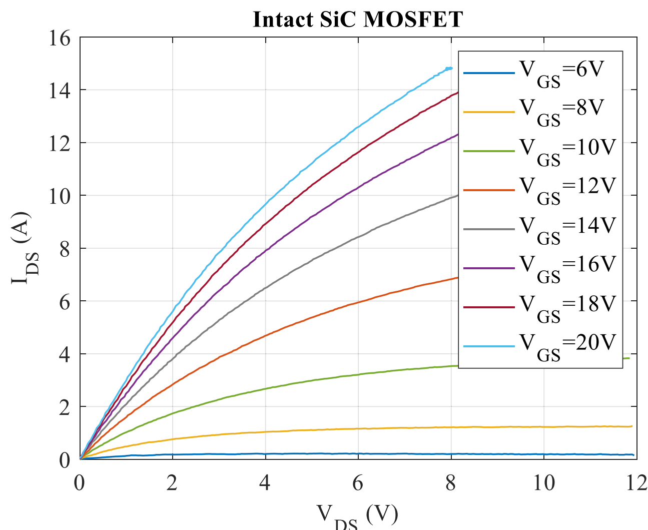
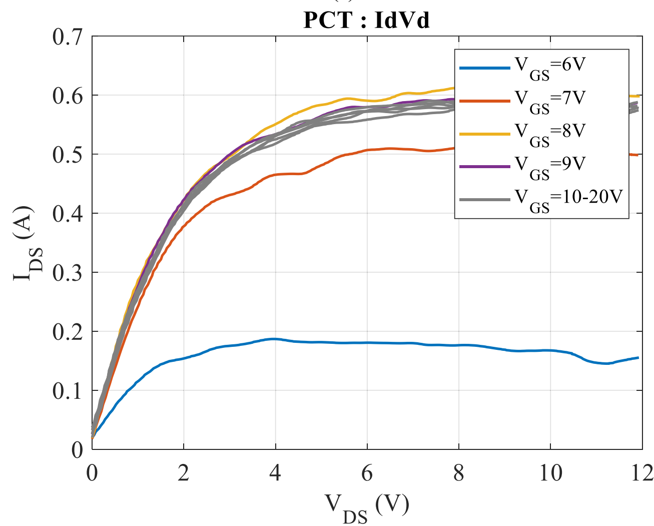


Fig. 8. PCT experimental hardware waveforms of load current, drain-source, and gate-source voltages.

In all experiments, after each test, the tested devices were characterized to assess their performance accurately. Since almost similar results were observed from all samples, the data from all tests were collected, plotted, and averaged to minimize variations and provide a clearer representation of both the output and transfer characteristics. According to the results from the Keithley instruments, the output characteristics of the DUTs for the pre-PCT and post-PCTs are depicted in Fig. 9 (a) and (b). It is evident from Fig. 9 (b) that after PCT, the DUTs are no longer influenced by a gate-source voltage higher than 8 V, as the drain current saturates prematurely. Additionally, despite the increase in V_{DS} beyond 4 V, the drain current I_{DS} does not increase further after PCT. However, in Fig. 9 (b), the post-PCT SiC MOSFET still exhibits a slight increase in drain current of up to 4 % compared to the pre-test SiC MOSFET. Moreover, the transfer characteristic of post-PCT SiC MOSFET



(a)



(b)

Fig. 9. Output characteristics of the SiC MOSFET (a) pre-test (b) post-PCT with varying V_{GS}.

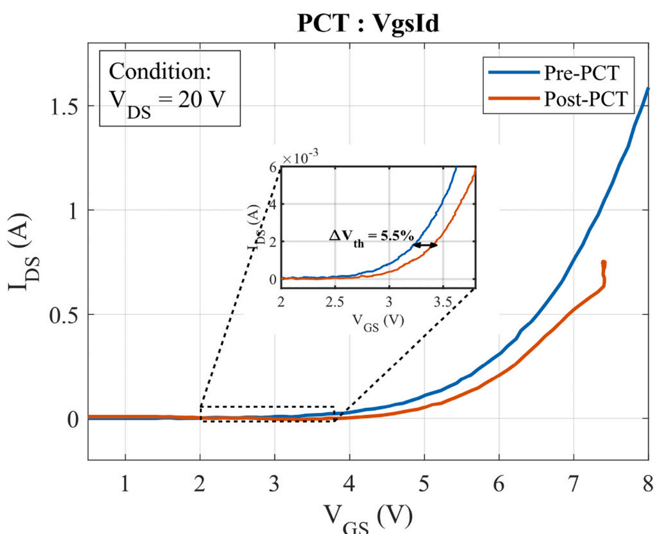


Fig. 10. The transfer characteristics of the pre-PCT and post-PCT SiC MOSFET.

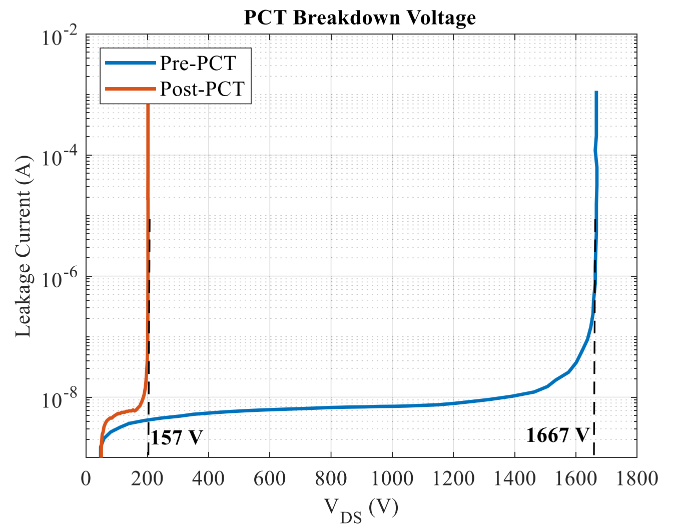


Fig. 11. The breakdown voltage of the pre-PCT and post-PCT SiC MOSFET.

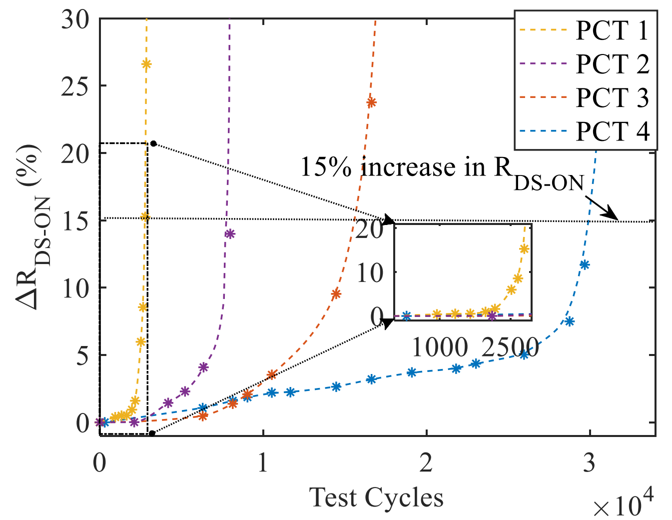


Fig. 12. PCT test results showing SiC MOSFET R_{DS_ON} for test cases in Table 1.

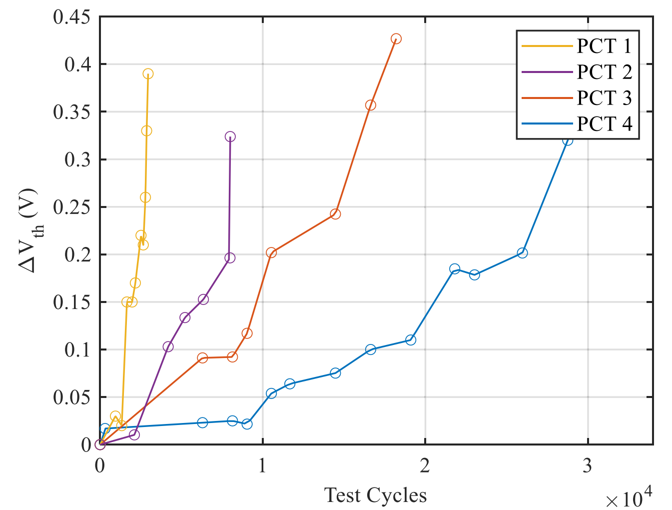


Fig. 13. The threshold voltage shifts of SiC MOSFETs during PCT.

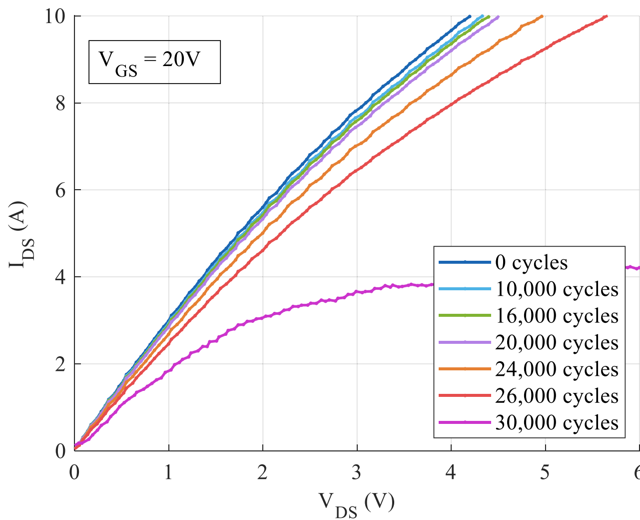


Fig. 14. The output characteristic of the SiC MOSFET during PCT.

is recorded. As shown in Fig. 10, the threshold voltage is shifted by 5.5 %. However, beyond a gate-source voltage of 7.5 V, the drain current of the SiC MOSFET no longer increases, indicating that the device has reached saturation. This behavior is consistent with the results in Fig. 9 (b), where the drain current saturates at approximately 0.6 A after PCT.

In Fig. 11, the breakdown voltages of pre-PCT and post-PCT are displayed. It is evident that the drain-source junction of the SiC MOSFET has been compromised, causing the SiC MOSFET to be unable to withstand voltages exceeding 156.9 V, which is 9.4 % of the nominal value.

In accordance with Table 1, the change characteristic of R_{DS_ON} is displayed in Fig. 12. As mentioned previously, the failure criterion is defined as a 15 % increase in the value of R_{DS_ON}.

On another note, the change in threshold voltage V_{th} for all PCTs is illustrated in Fig. 13, providing insight into the shifts in device behavior during testing. Furthermore, and as an example, Fig. 14 illustrates the output characteristic for PCT 4 at a gate-source voltage V_{GS} of 20 V, highlighting the degradation in device performance caused by extended cycling.

4.2. IAT experimental setup and results

In contrast to PCT, the experimental setup for IAT is more intricate. As mentioned before, the input filter for IAT consists of DC Link capacitors, while the output filter consists of an LC filter. The setup details are outlined in Table 2. The topology employed is an H-ANPC inverter. It is crucial to design the H-ANPC inverter for the IAT with adequate

Table 2
Summary of the IAT test parameter specifications.

Parameter	Value
Bus Voltage	800 V
DC-Link Capacitor	1190 μF
Si IGBT (IKW03N120H)	1200 V/10 A
SiC MOSFET (C2M0280120D)	1200 V/10 A
Snubber Capacitor	560 *p*F
Subber Resistor	50 Ω
Inductor Filer	1.76 *m*H
Capacitor Filter	7.8 μF
Fundamental Frequency	10 Hz
Switching Frequency	42 *k*Hz

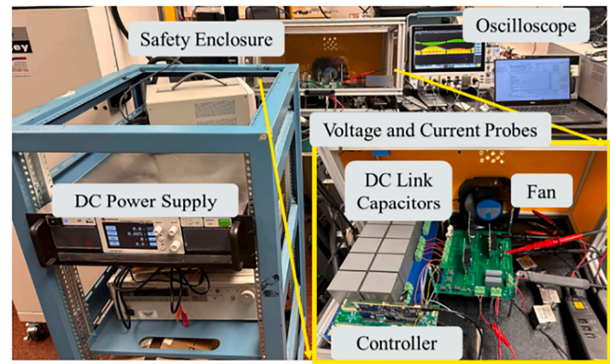


Fig. 15. IAT experimental hardware setup.

Table 3
Summary of the IAT parameters for SiC MOSFET.

IAT #	T_{j-min}(°C)	ΔT_j (°C)	I_{max}(A)	$N_f \times 10^3$
1	43.5	84.5	10	8.8409
2	47	82	9.6	20.6968
3	43	80	9.4	28.4991
4	43	77	9.4	34.9463
5	51	61	9.3	71.8389
6	78	46	8.3	189.866

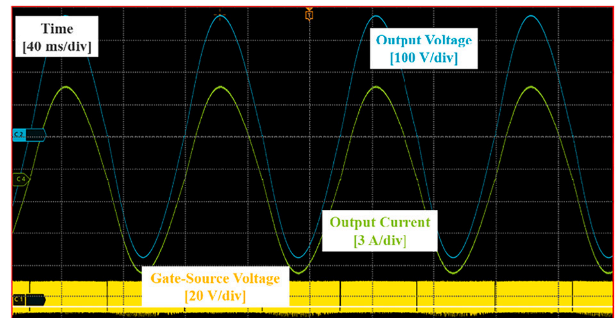


Fig. 16. IAT experimental hardware waveforms of output current and voltage, gate-source voltage.

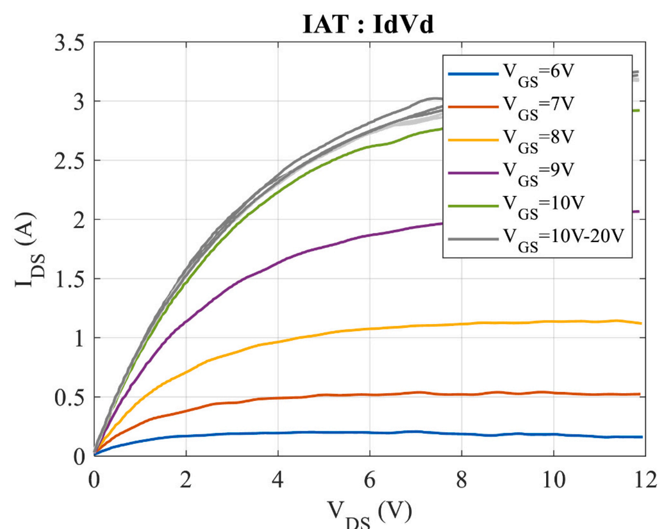


Fig. 17. Output characteristics of the post-IAT SiC MOSFET with varying V_{GS}.

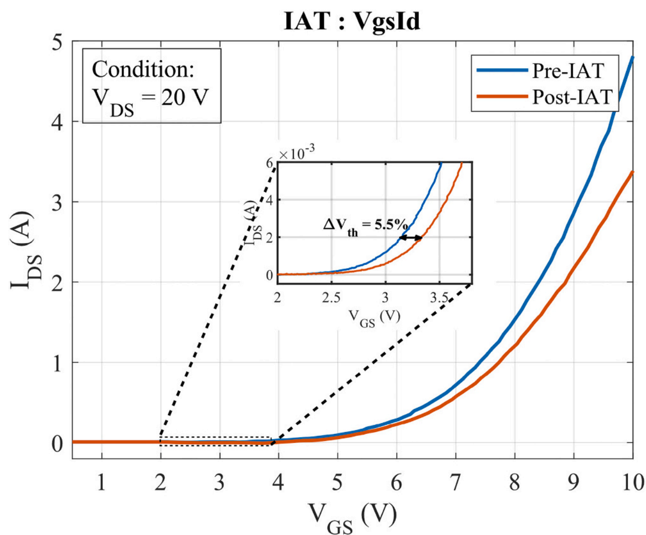


Fig. 18. The transfer characteristics of the pre-IAT and post-IAT SiC MOSFET.

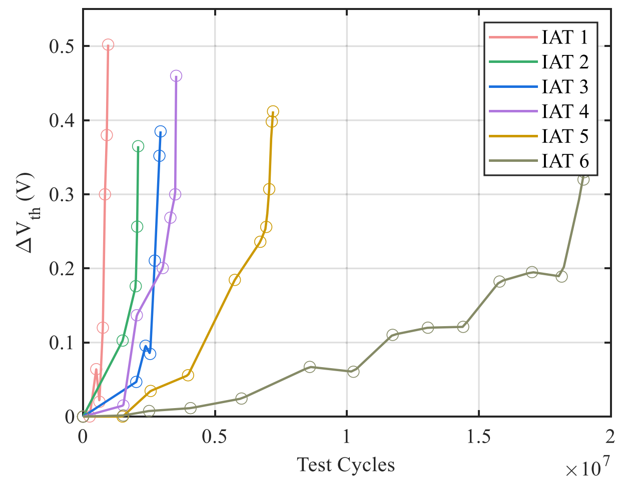


Fig. 21. The threshold voltage shifts of SiC MOSFETs during IAT.

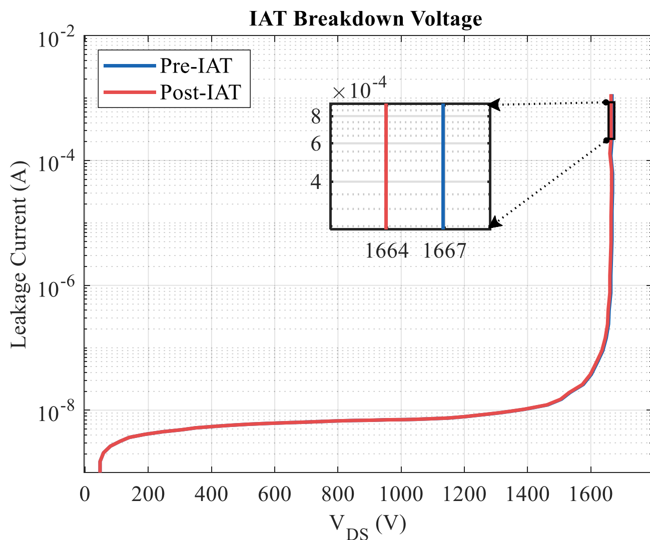


Fig. 19. The breakdown voltage of the pre-IAT and post-IAT SiC MOSFET.

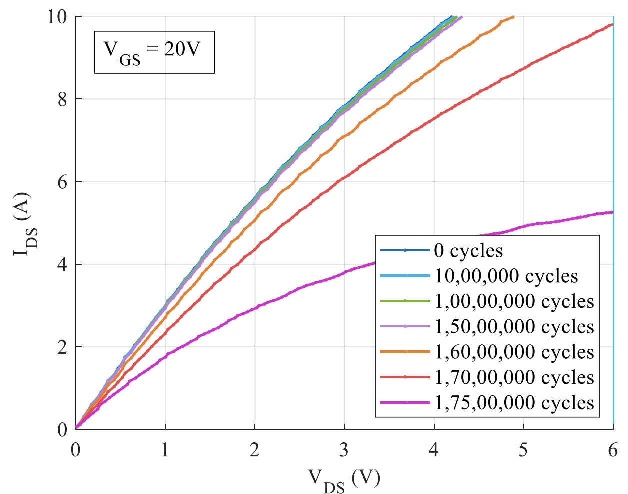


Fig. 22. The output characteristic of the SiC MOSFET during IAT.

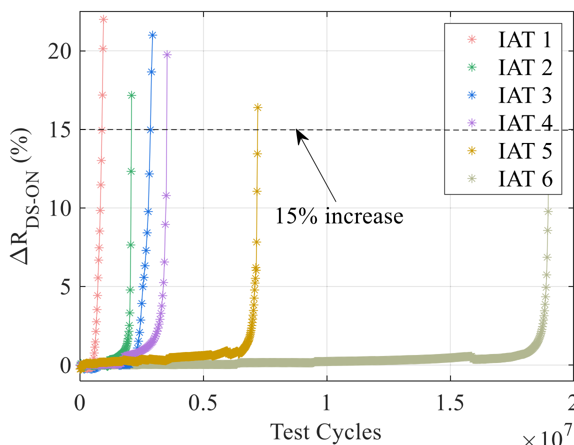


Fig. 20. IAT test results show SiC MOSFET R_{DS_ON} for test cases in Table 3 (Note: Test Cycles represent the number of 10 Hz cycles).

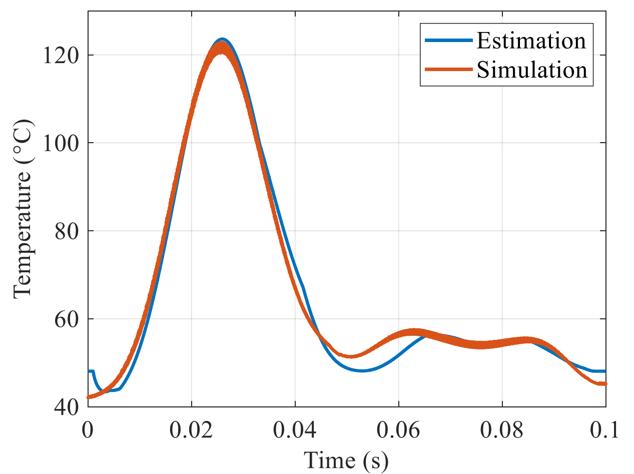


Fig. 23. SiC MOSFET junction temperature plot for SiC MOSFET operates within the H-ANPC inverter at $I_{max} = 10\,A$ and $T_{j-min} = 40^{\circ}C$.

protection to safeguard other components in the event of device failure. Additionally, precise inverter design is essential to mitigate issues such as EMI noise. In each IAT test condition, the two SiC MOSFETs are monitored, and their data is recorded. Some test conditions are repeated to gather multiple samples. The experimental setup for IAT is depicted in Fig. 15, and detailed test conditions are provided in Table 3. Furthermore, the line frequency is set at 10 Hz to increase device stress. Fig. 16 demonstrates the output voltage and current of the H-ANPC inverter as one of the IAT conditions. The output and transfer characteristics of DUTs according to the IAT results are illustrated in Figs. 15 and 16. The output characteristics in post-IAT become consistent across different gate-source voltages higher than 10 V, as shown in Fig. 17. Regarding the drain current, it increases more significantly than post-PCT, yet it still falls short compared to the pre-test SiC MOSFET (up to 20 %), shown in Fig. 9(a). Fig. 18 illustrates the variation in transfer characteristics over stress time. Throughout the aging process, the threshold voltage of post-IAT SiC MOSFET increases by 5.5 %.

The breakdown voltage of pre-IAT and post-IAT are shown in Fig. 19. The drain-source junction of the SiC MOSFET remains functional and can effectively block voltage similar to the pre-IAT SiC MOSFET. The failure criterion is the same as PCT (a 15 % increase in the value of R_{DS_ON}). Hence, R_{DS_ON} is plotted based on Table 3 and displayed in Fig. 20 to determine the N_f and lifetime of the SiC MOSFET. To better comprehend the device degradation, the changes in threshold voltage V_{th} observed during all IATs are shown in Fig. 21. In addition, Fig. 22 presents the output characteristic for IAT 6 at a V_{GS} of 20 V, providing a representative example illustrating the behavior of the device following test cycles.

4.3. Junction temperature of DUTs verification

The lifetime estimation model for SiC MOSFETs subjected to the PCT and IAT depends critically on the accurate estimation of the junction temperature. To validate the precision of this estimation, a detailed electrothermal model of the test circuit is simulated on SaberRD. The device junction temperature from the simulation is compared with the real-time estimation technique obtained following the procedure in Section 3. Fig. 23 shows the time domain comparison of the estimated and simulated junction temperature of the SiC MOSFET for a maximum current of 10 A in the more complicated IAT setup. Additionally, the parametric plot in Fig. 24 compares the estimated and simulated swings in the junction temperature of the SiC MOSFET operating across various device currents and a fixed case temperature. A maximum mismatch of 1.5 % validates the accuracy of the real-time junction temperature estimation technique. This confirms the accuracy of the junction temperature estimate used in the lifetime model.

5. Lifetime of SiC MOSFET and discussion

5.1. Lifetime assessment

The PCT results obtained from Table 1 (detailed in [24]) and IAT captured in Table 3 are used to build an empirical lifetime model, specifically Bayerer's model [25,26]. This lifetime model captures the cycle-to-failure of semiconductor devices as a function of their electrothermal stress. The lifetime model describes the relationship between the number of thermal cycles and device failure of the SiC MOSFETs under varying thermal and electrical stresses observed during the PCT and IAT and is given by:

$$N_f = K \bullet \Delta T_j^{\beta_1} \bullet e^{\left(\frac{\beta_2}{T_{j-min}+273}\right)} \bullet t_{on}^{\beta_3} \bullet I^{\beta_4} \quad (5)$$

where N_f is the number of cycles to failure, t_{on} is the duration of the device on time during each cycle, ΔT_j is the junction temperatures swing, T_{j-min} is the minimum temperature of the devices and I is the current per bond wire. The model parameters K and $\beta_1 - \beta_4$ are determined by least squares curve fitting of the test data. These parameters are presented in Table 4 and compared to those from previous PCTs conducted on the same part number of SiC MOSFETs.

Following the determination of model parameters, a mission profile-based device lifetime prediction is conducted. This involves simulating the annual operational profile of the inverter and evaluating the temperature stress of the SiC MOSFETs and damage accumulation using the newly calibrated model. Mission profiles representing the typical inverter operating power for PV inverters in Arizona (260 sunny, 100 cloudy days) and Seattle (130 sunny, 230 cloudy days) are used in this paper. The operation of the H-ANPC inverter following the mission profiles is translated into the junction temperature and current stress of the SiC MOSFETs using a precise electrothermal model for the H-ANPC inverter simulated on SaberRD. This simulation identifies periods of cyclic thermal stress throughout the year, which are used to calculate the cumulative damage for the SiC MOSFETs. Additionally, a Monte Carlo analysis is applied to estimate the failure probability distribution of the SiC MOSFETs. This statistical method accounts for variations in model parameters and operational conditions, providing a probabilistic view of device reliability. The authors describe the details of the lifetime assessment process in [24]. Fig. 25 (a) and (b) present a comparison of the unreliability functions of the SiC MOSFET in the H-ANPC inverter based on lifetime models derived from IAT data and PCT data for Seattle-like and Arizona-like mission profiles, respectively. The plots indicate the B_{10} lifetime of the SiC MOSFETs, showing the probability of failure for 10 % of the SiC MOSFETs in the H-ANPC inverter. The results indicate that the SiC MOSFET lifetime estimation from the IAT-derived model projects a 32 % lower lifetime compared to the PCT-based model. This discrepancy suggests that the IAT-based model, which more realistically replicates actual inverter operations, indicates a higher failure probability for the SiC MOSFET in the H-ANPC inverter than the PCT model. Consequently, the traditional PCT model may overestimate the reliability of the SiC MOSFET, highlighting the importance of using realistic testing methods like the IAT for more realistic lifetime predictions.

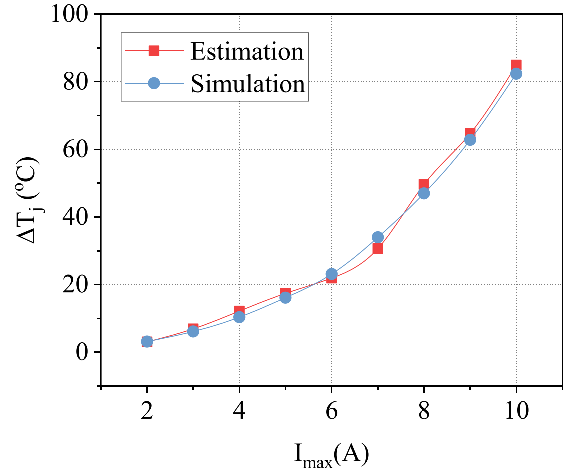


Fig. 24. Simulation and estimation of ΔT_j of SiC MOSFET across the operating current of the SiC MOSFET within the H-ANPC inverter.

Table 4
Lifetime model parameters for SiC MOSFET Tested.

	K (x 10^5)	β_1	β_2 (x 10^3)	β_3	β_4
PCT	3.5365	− 3.7534	6.0619	− 0.7506	− 0.1970
IAT	40.0101	− 3.6654	5.2356	− 0.4282	− 0.0115

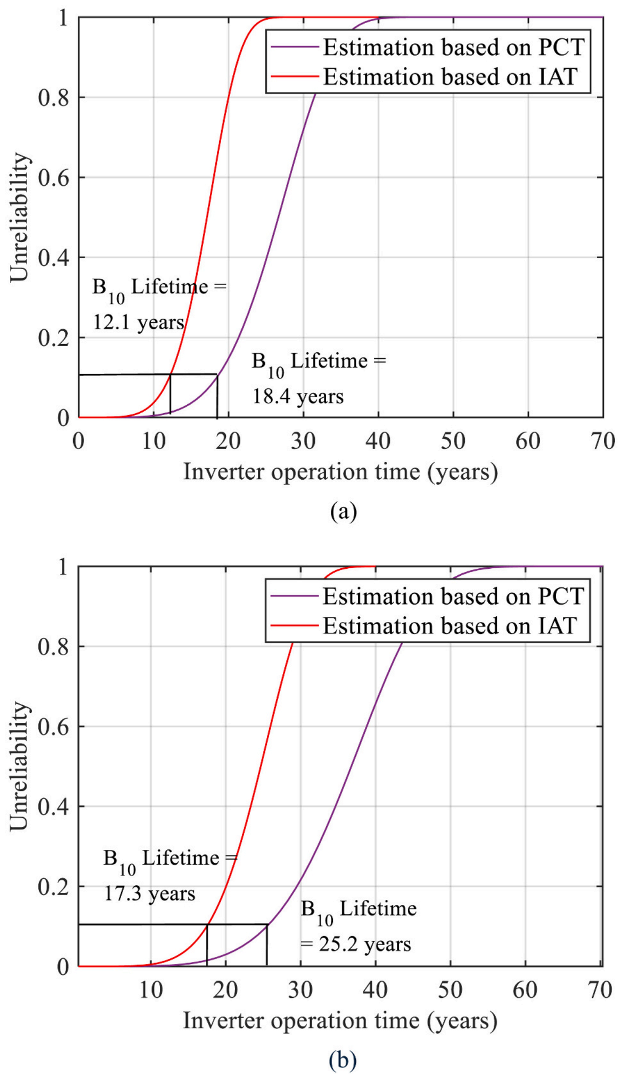


Fig. 25. The unreliability function for SiC MOSFET in the H-ANPC inverter is based on the PCT and IAT lifetime model, operating in (a) Seattle and (b) Arizona.

5.2. Comparison discussion

The PCT setup, characterized by a full-bridge topology and simultaneous testing of multiple samples, shows less complexity compared to the more intricate IAT setup with an H-ANPC inverter. Both tests adhere to a failure criterion defined by a 15 % increase in R_{DS_ON}. Based on these results, it is evident that the SiC MOSFETs subjected to PCT experience more significant degradation compared to those subjected to IAT. The PCT results reveal that the I_{DS} saturates prematurely, limiting the post-PCT output characteristics to only a modest 4 % increase in drain current compared to pre-test conditions. This saturation is also reflected in the transfer characteristics, which show a 5.5 % shift in threshold voltage, with no further increase in current beyond a V_{GS} of 7.5 V, indicating the device has reached the I_{DS} saturation. In contrast, the IAT results demonstrate consistency in output characteristics across V_{GS} higher than 10 V, with a more significant I_{DS}, although still up to 20 % compared to pre-test conditions. Similarly, for the transfer characteristics, the PCT results show a complete termination of response at 7.5 V and a 5.5 % shift in threshold voltage, signaling the I_{DS} saturation condition. The IAT, however, demonstrates a continuous response to gate-source voltage and a similar shift in threshold voltage up to 7.5 V compared to PCT. In the same way, the breakdown voltage of the SiC MOSFETs was measured after both post-PCT and post-IAT. The results indicate that the post-PCT SiC MOSFET exhibits significant damage to its drain-source junction, withstanding only 9.4 % of the pre-PCT SiC MOSFET breakdown voltage value. In contrast, the drain-source junction of the post-IAT SiC MOSFET remains largely intact and performs similarly to the pre-test MOSFET. It is important to mention here that the results highlight distinct degradation behavior due to the different testing conditions.

Additionally, the $R_{DS\text{-}ON}$ is increased by 15 % for both PCT and IAT experiments. To address the root cause of the increase in $R_{DS\text{-}ON}$, it is important to understand the components of $R_{DS\text{-}ON}$, which are as follows

$$R_{DS-ON} = R_{CH} + R_{JFET} + R_{epi} \tag{6}$$

while R_{CH} is channel resistance, R_{JFET} is Junction Field Effect Transistor (JFET) resistance, R_{epi} is epitaxial layer resistance of the drift region. As indicated in [27], the $R_{DS\text{-}ON}$ of a SiC MOSFET is particularly sensitive to changes in the threshold voltage (V_{th}), which primarily correlates with R_{CH}. The channel resistance is given by the following equation,

$$R_{CH} = \frac{L}{W\mu_n q n_{inv}} \approx \frac{L}{W\mu_n C_{ox}\left(V_{G,use} - V_{th}\right)} \tag{7}$$

where W is channel width, L is Channel length, μ_n is free electron mobility, q is elementary charge, n_{inv} is inversion charge density at the interface, $V_{g,\ use}$ is Gate drive voltage, V_{th} is the threshold voltage of the device, C_{ox} is gate oxide capacitance. Based on (6), (7), Fig. 13, and Fig. 21, the change in R_{CH} is approximately 3.45 %. As mentioned, the $R_{DS\text{-}ON}$ is increased by 15 % after PCT and IAT tests. Therefore, the primary contributor to the degradation of $R_{DS\text{-}ON}$ is package degradation rather than changes in R_{CH}.

The other important difference between PCT and IAT is the lifetime prediction based on the PCT and IAT model derived in Section 5. The results show that the IAT-based model, which closely replicates actual H-ANPC inverter operations, predicts a 32 % shorter lifetime for the SiC MOSFETs compared to the PCT-based model. This suggests that the PCT method tends to overestimate the lifetime, highlighting a potential overestimation of reliability when using traditional PCT methods. Therefore, according to the differences between PCT and IAT, the article underscores the importance of using realistic testing methods like IAT for more accurate lifetime predictions of SiC MOSFETs in inverters.

6. Conclusion

The importance of realistic testing protocols for assessing the long-term reliability of SiC MOSFETs in power electronics applications under real-world operating conditions is emphasized in this article. As discussed in Section 5, a detailed comparison between the IAT and the standard PCT revealed significant differences in degradation behavior and lifetime predictions. The IAT, which replicates the operational conditions of the H-ANPC inverter closely, projected a 32 % shorter lifetime for SiC MOSFETs compared to the PCT. This suggests that the PCT method tends to overestimate reliability, potentially leading to unrealistic expectations of device performance over time. Conversely, the PCT was found to cause significantly more degradation to the SiC MOSFETs than the IAT. Additionally, the observed increase in $R_{DS\text{-}ON}$ is primarily linked to package degradation rather than a shift in the threshold voltage. Future studies will aim to investigate further and pinpoint the exact mechanisms underlying this package-related degradation. These findings underscore the importance of evaluating devices within their specific operational conditions and temperature profiles, particularly in converter-specific accelerated testing scenarios, as demonstrated with the H-ANPC inverter in this article.

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Data availability

The data that has been used is confidential.

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