Reactive-Power Compensation in a Single-Stage Differential-Mode Solid-State Transformer

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***Abstract*—Isolated single-stage solid-state transformer (SST), which employs zero-voltage switching (ZVS) for high-efficiency operation, generally has limited capability for supporting reactive load. In this article, a novel technique is proposed for a single-stage differential-mode SST (DM-SST), which supports reactive-power compensation in such non-unity-power-factor loads. A pulsewidth modulation active-clamp (PAC) Ćuk converter is used for the DM-SST modules to employ the technique. The PAC-Ćuk converter utilizes clamp circuits across the two main switches, each consisting of an auxiliary capacitor and a switch operating complementarily to the main switch. Addition of the clamp circuits provide ZVS operation on all the switches. In this article, the duty cycles of the switches are varied using a feedforward control to also support the reactive power. Furthermore, the output power relation of the DM-SST for the extended range of control parameters, duty cycles of the main switches, and the phase-shift ratio between the main switches is studied. A design guideline of the DM-SST supporting the reactive load is also presented using the extended output power relation. A 1-kVA hardware prototype of the DM-SST is built using the underscored design guideline to validate the analysis and the operation of the DM-SST.**

***Index Terms*—Reactive load, reactive-power compensation, solid-state transformer (SST), zero-voltage switching (ZVS).**

NOMENCLATURE

LFT	Low-frequency transformer.
PAC-Ćuk	PWM active-clamp Ćuk.
$C_{T1},\ C_{T2}$	Input- and output-side blocking auxiliary capacitors.
$C_{A1},\ C_{A2}$	Input- and output-side blocking capacitors.
n	Transformer turn ratio.
C_r	Equivalent blocking capacitor referred to input side $C_r = C_{A1}\ \|\|n^2 C_{A2}$.
L_r	Inductor in series with C_{A1}.
T_1	High-frequency transformer.
HFL	High-frequency link formed by $C_{A1}, L_r, C_{B1},$ and T_1.
$L_{\text{in}},\ L_o$	Input and output inductors.
$S_1 - S_4$	Switches of the PAC-Ćuk converter module.
T_s	Switching period of the DM-SST.
f_s	Switching frequency of the DM-SST.
Z_r	Characteristic impedance of high-frequency link formed by L_r and C_b, $Z_r = \sqrt{L_r/C_b}$.
ω_r	Angular frequency of high-frequency link formed by L_r and C_b, $\omega_r = 1/\sqrt{L_r C_b}$.
Δ_ϕ	Phase-shift ratio defined as the ratio of delay between the turn-OFF of S_1 and turn-ON of S_3 normalized by the switching period T_s.
d_1, d_2	Duty cycles of main switches S_1 and S_3, respectively.
$V_{\text{in}},\ V_o$	RMS input and output voltages of the ac/ac converter.
$v_{\text{in}},\ v_o$	Instantaneous input and output voltages of the DM-SST.
i_{in}, i'_o	Instantaneous input current and output current.
p_T	Power transfer through the HFL over T_s.
v_1, v'_2	Instantaneous node voltage across the switches S_1 and S_3.
$\langle v_2 \rangle$	Average of v'_2 referred to the primary side of transformer over T_s.
$\langle i_2 \rangle$	Equivalent current through the HFL over T_s seen at the output side given by $p_T/\langle v_2 \rangle$.
ϕ_{in}	Lagging angle formed between the fundamental component of i_{in} and v_{in}.
ϕ_o	Lagging angle formed between the fundamental component of i'_o and v_o.
ω_L	Angular line frequency of the grid voltage.
g^*	Ideal solution function on HFL for ac/ac conversion given by i_2/v_{in}.
$g(d_1, d_2, \Delta_\phi)$	Solution function on HFL for the DM-SST. Also represented by g in the article.
T_Δ	Time for which $g = g^*$ in a half-line cycle.

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I. INTRODUCTION

SOLID-STATE transformers (SSTs) are an emerging technology to replace the bulky and monolithic conventional LFTs. In contrast to LFTs, the SSTs have the potential to offer fast autovoltage regulation and reactive-power compensation internally. As the efficiency and reliability of an LFT are high [1], single-stage isolated ac/ac converters are leading contenders for the SST technology. A single-stage isolated SST can potentially

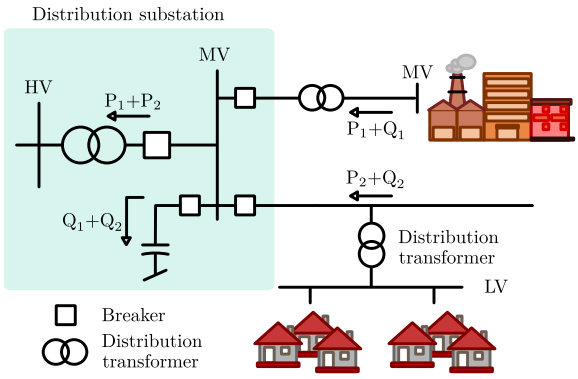

Fig. 1. Example of a simplified one-line diagram of a distribution system.

yield higher efficiency owing to lower component count and reduced energy processing in the ac/ac conversion compared with multistage solution [2], [3]. To further increase the SST efficiency, an ac/ac converter with the capability of performing zero voltage switching (ZVS) turn-ON on all switches over a wide operating range of the load is preferred to mitigate the switching losses. The ac/ac topological solutions involving dual-active bridge (DAB) converter [4], [5], [6], *LLC* converter [7], [8], [9], and matrix-type converter [10], [11] have been explored for SST applications and demonstrated to achieve high efficiency by mitigating the switching losses. However, the works on the single-stage ac/ac converters, presented in these articles, primarily demonstrated the SST operations with active-power loads.

As reactive power is prevalent in distribution systems (e.g., motor-based appliances [12], [13] and voltage control [14], [15], [16]), an SST application often necessitates reactive-power-handling capability [17]. The reactive compensating sources (e.g., shunt capacitors and static-VAR compensators [12]) are generally placed in distribution substations, which can be far from the load, as shown in Fig. 1, resulting in losses and voltage fluctuations. An SST with added capability of reactive-power compensation can mitigate these adverse effects, improving the grid performance and its utility [17]. In addition, the increased penetration of distributed energy resources is resulting in reduced instantaneous energy reserves, which causes voltage fluctuation and instability. Methods, such as Volt–Var optimization, are being deployed to provide local inertial using the reactive sourcing capability of photovoltaic (PV) inverters [18], [19]. In the modern power system, an SST can be used to interface PV inverter to the grid, hence, should have reactive-power-handling capability.

An integrated DAB-based ac/ac converter for SST solution is presented in [20] and [21]. Unlike a conventional three-stage solution involving separate ac–dc, dc–dc, and ac–ac conversion stages, the authors in [20] and [21] integrate the conversion stages to reduce the number of active switches from 16 to 12. In [21], the presence of dc links at the primary and secondary sides of the SST transformer enables seamless operation with reactive-power load since the dc link at the output side absorbs the reactive power. As noted in Table I, the solution offers wide ZVS operation of the switches over entire grid cycle. However, the three-stage solution also requires three controllers to ensure the stable operation of the converter, making the control design complex. Besides the need for a large number of active switches and bulky capacitors for the dc links, the multiple power-conversion stages of the SST lead to relatively low efficiency of 93.5%.

In [22], an integrated three-stage ac/ac symmetric half-bridge converter (SHBC) is presented where a DAB converter is combined with two interphase transformers. The solution offers a dense solution due to interleaving technique. Two dc-link capacitors are also present in this topology allowing input and output port decoupling. SHBC requires eight switches with partial ZVS turn-ON. The converter can handle wide reactive load and offer reactive compensation capability. The three-stage solution offers peak efficiency of 91.7%.

The authors in [28] and [29] showcase the simulation results of single-stage SSTs based on DAB feeding reactive loads. In both the articles, the phase shift between the two active bridges is used to control the power flow through the high-frequency link (HFL) formed by the series inductor and the transformer and saturates for reactive-load operation for low instantaneous input voltage due to imaginary solutions of the phase shift. The imaginary solution occurs for the single-stage converter due to the impedance of HFL, which limits the power transfer. In [28], the SST is shown to operate at 60% rated power with a lagging power factor of 0.95 ($\phi_o = 18°$); however, distortion at the output voltage is visible in the result. Detailed analysis on the effect of reactive power on the ac/ac operation is provided in [29]. The reactive-power operation for the DAB necessitates either changing the leakage inductance or the switching frequency to reduce the duration of the imaginary solution of phase shift, which causes output voltage distortion, over a line cycle for the ac/ac operation.

Single-stage hard-switching ac/ac solutions does not have limitation with reactive loads as they generally have high instantaneous power transfer capability. Eshkevari et al. [23] proposed a buck–boost ac (BB-AC) converter, which offers continuous input and continuous output current. The peak efficiency obtained for BB-AC is 93.5% and output voltage total harmonic distortion (THD) of 2.3% for *RL* load. Ahmed et al. [25] also proposed a continuous input and output current-based symmetric-bipolar-type buck-boost ac (SBT-BBAC) converter. Both the topology offers good reactive-load performance. Fathi et al. [24] presents a four-switch-based quasi-Z-source converter. Even though the converter requires low active switch count, high number of diodes and passive components are needed. The converter is experimentally tested with power factor (PF) = 0.8. As shown in Table I, the efficiency performance of these single-stage hard-switching converters is in the range of 91%–94% due to high switching losses. However, these converters have satisfactory performance with reactive load.

Zheng et al. [26] proposed a soft-switching single-stage current-source converter named S4T. Due to the current source nature of the converter, modular scaling of S4T (series input and series output) is easy to implement and has been demonstrated. The converter offers an estimated peak efficiency of 97% for ac/ac conversion. S4T is also reported to handle reactive load. However, the converter requires a high count of active switches

TABLE I
COMPARISON WITH OTHER ISOLATED AC–AC CONVERTERS

Topology	DM-SST	Three-stage DAB [21]	SHBC [22]	Hybrid DAB [5]	LLC [7]	Matrix-type DAB [10]	BB-AC [23]	Quasi-Z-source [24]	SBT-BBAC [25]	S4T [26]
Switches/diodes	8/0	12/0	8/0	12/0	12/0	14/0	5/4	4/10	8/0	10/10
Capacitors	12	3	5	4	3	3	3	7	4	4
Magnetic cores	6 (2*)	4	6	4	3	5	3	5	3	5
ZVS range	Wide	Wide	Partial	Wide	Wide	Wide	No	No	No	Wide
DC-link capacitor	No	Yes	Yes	No	No	No	No	No	No	No
Reactive-load capability	Yes	Yes	Yes	N/R	N/R	N/R	Yes	Yes	Yes	Yes
Reactive compensation	Yes	Yes	Yes	No	No	No	No	No	No	No
Peak efficiency	97.3%	93.5%	91.7%	92.1%	96.32%	93.3%	93.5%	91%	92.1%	97%
Output power	1 kVA	1 kW	500 W	2 kW	1.5 kW	2 kW	250 VA	2 kVA	400 W	22 kVA
Switching frequency	40 kHz	100 kHz	30 kHz	100 kHz	40 kHz	100 kHz	40 kHz	100 kHz	25 kHz	16 kHz
Output voltage	220 V	100 V	110 V	220 V	220 V	220 V	100 V	100 V	110 V	480 V
Switch voltage rating	1.2 kV	1.2 kV	650 V	600 V	600 V	N/R	650 V	N/R	600 V	1.2 kV

N/R=Not reported, and * integrated magnetic solution [27]. Note: Wide ZVS range is used to indicate the capability of ZVS switching on the switches over entire-line cycle, and partial ZVS is used to indicate the capability of ZVS switching over limited region of linecycle.

and diodes due to the need of reverse current blocking. A very low leakage transformer is also required for better performance of the converter.

A single-stage isolated differential-mode solid-state transformer (DM-SST) based on PAC-Ćuk converter module is proposed in [30] and is shown in Fig. 2(a) and (b). As the converter is based on Ćuk converter, DM-SST offers continuous input and output current. The current-source nature of the input and output port allows easy modular scaling of the DM-SST to distribute the voltage equally between the modules, making it suitable for high-voltage applications [31]. However, the DM-SST discussed in [30] also suffers with output voltage distortion for reactive load.

In this article, a new control strategy is provided for the DM-SST, which overcomes the limitation using two aggregated strategies. First, the reactive power through the HFL is reduced by using the auxiliary capacitor to source the load reactive power. Second, by extending the maximum power transfer capability through the HFL using the duty cycles. The proposed solution expands reactive-power-handling and absorption capability of the DM-SST, however, with higher voltage stress on the switches and auxiliary capacitors. The following are the key contributions of this article.

1) Unlike the work presented in [30] where only phase-shift ratio is used to control the ac/ac operation, in this article, a novel operational mechanism that controls the voltage across the auxiliary capacitors through the duty cycle of the switches is proposed to facilitate and extend the reactive-power-handling capability of the DM-SST without needing any additional components. The proposed mechanism utilizes the auxiliary capacitors to support reactive-power compensation over a wide range while preserving the high-efficiency operation, a typical feature of multistage ac/ac converters.
2) A detailed analysis on the effect of the extended range of duty cycles and polarity of phase-shift ratio on the operation of the DM-SST is also performed. It is noted that, while in [32] and [33], duty-cycle dependencies on the operation of the PAC-Ćuk are presented, only positive phase-shift ratio is considered, which limits the validity of the model.
3) A feedforward-linearization control is also devised for ac/ac operation, which greatly simplifies the closed-loop controller of the DM-SST. The linearization significantly improves the tracking performance of the DM-SST for reactive loads.

Overall, in this article, the analysis of the effect of duty cycles on the operation of the DM-SST is provided in Section II. The analysis is separated by the time scale of line and switching cycles for simplification. Section III discusses the operation of the DM-SST; furthermore, a feedforward-linearization function is also devised to enable the closed-loop voltage control. In Section IV, a design guideline for the DM-SST is provided for reactive-power operation. Section V presents the simulation and experimental results regarding validation. Finally, Section VI concludes this article.

II. OPERATION OF DM-SST WITH VARIABLE DUTY CYCLE

The single-stage DM-SST consists of two identical isolated dc/dc modules (Modules 1 and 2) connected differentially at the input and output port, as shown in Fig. 2(a), to perform the ac/ac conversion. The modules are operated under discontinuous modulation scheme (DMS) [30] where only one module is switched at a time at high frequency depending on the polarity of the input voltage v_{in} as given in the following equation:

$$v_{\text{in},1} = \begin{cases} v_{\text{in}} & \text{for } v_{\text{in}} > 0 \\ 0 & \text{for } v_{\text{in}} < 0 \end{cases}, \quad v_{o,1} = \begin{cases} v_o & \text{for } v_{\text{in}} > 0 \\ 0 & \text{for } v_{\text{in}} < 0 \end{cases}$$

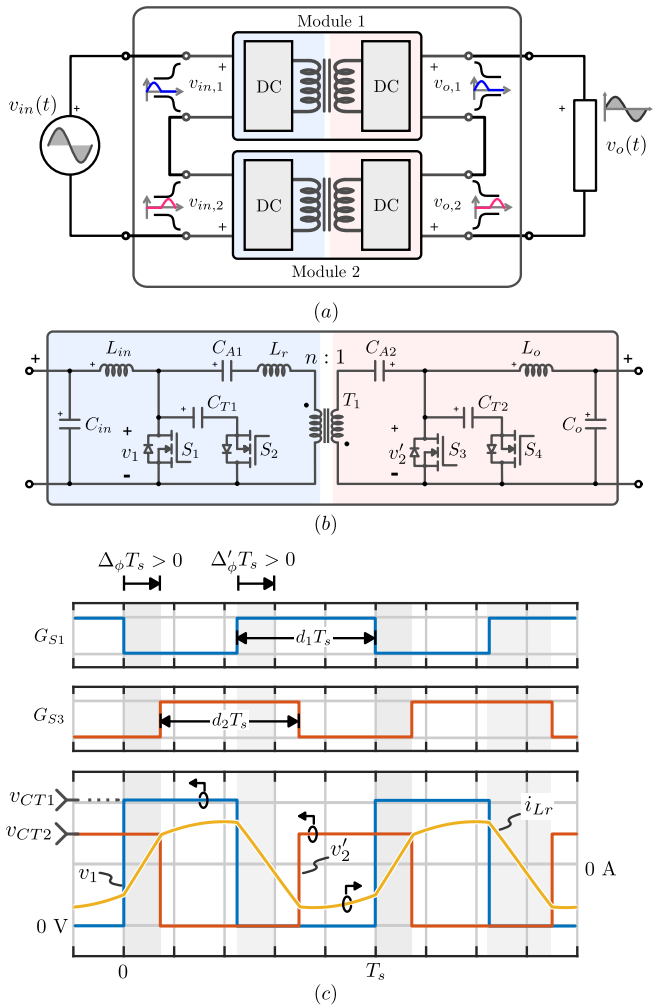

Fig. 2. (a) Architecture of the DM-SST. (b) Isolated PAC-Ćuk converter used for a DM-SST module. (c) Waveforms of the PAC-Ćuk module.

$$v_{\text{in},2} = \begin{cases} 0 & \text{for } v_{\text{in}} > 0 \\ -v_{\text{in}} & \text{for } v_{\text{in}} < 0 \end{cases}, \quad v_{o,2} = \begin{cases} 0 & \text{for } v_{\text{in}} > 0 \\ -v_o & \text{for } v_{\text{in}} < 0 \end{cases} \tag{1}$$

where $v_{\text{in},1}$ and $v_{o,1}$ are the input and output voltages of Module 1, respectively, while $v_{\text{in},2}$ and $v_{o,2}$ are the input and output voltages of Module 2, respectively. DM-SST under DMS is operated such that the output voltage (v_o) and the input voltage (v_{in}) are in phase.

The PAC-Ćuk dc/dc converter (Module 1), as shown in Fig. 2(b), comprises auxiliary capacitors C_{T1} and C_{T2}, blocking capacitors C_{A1} and C_{A2}, series inductor L_r, isolation transformer T_1, and switches $S_1 - S_4$. Module 2, which has a topology identical to that of Module 2, comprises the same set of components. Parameters for these components used for Modules 1 and 2 in the DM-SST are so chosen that high efficiency is achieved while yielding reactive-power compensation for a non-unity-power-factor load. The PAC-Ćuk module has two half bridges formed by $S_1 - S_2$ and $S_3 - S_4$, where the switches of the half-bridge pair are operated complementarily with small deadband to avoid shoot-through condition. The PAC-Ćuk module has three control parameters: the duty cycle d_1 of S_1, the duty cycle d_2 of S_3, and phase-shift ratio Δ_ϕ defined as the ratio of delay between the turn-OFF of S_1 and turn-ON of S_3 to the switching period T_s. Fig. 2(c) shows the waveform associated with the operation of a PAC-Ćuk module. When G_{S1} is active, the nodal voltage v_1 is 0 V, while when G_{S1} is inactive, v_1 matches the voltage (v_{CT1}) across C_{T1}. Similarly, when G_{S3} is active, the nodal voltage v_2' is 0 V, while when G_{S3} is inactive, v_2' matches the voltage (v_{CT2}) across C_{T2}. By performing volt-second-balance analysis [34] on the input inductor (L_{in}), output inductor (L_o), and series inductor (L_r) over a switching period yields the following average-voltage relations [33], [35]:

$$\langle v_{CT1} \rangle = \frac{\langle v_1 \rangle}{d_1'} = \frac{v_{\text{in}}}{d_1'} \tag{2a}$$

$$\langle v_{CT2} \rangle = \frac{\langle v_2' \rangle}{d_2'} = \frac{v_o}{d_2'} \tag{2b}$$

$$\langle v_{CA1} \rangle = \langle v_1 \rangle = v_{\text{in}} \tag{2c}$$

$$\langle v_{CA2} \rangle = \langle v_2' \rangle = v_o. \tag{2d}$$

In (2a)–(2d), $\langle \blacksquare \rangle$ is the operator used to denote average value over a switching period $d_1' = (1 - d_1)$ and $d_2' = (1 - d_2)$. By assuming a quasi-static equilibrium [34], the simplified analysis of DM-SST operation can be separated into two time scales: the grid line cycle (T_L) and the switching cycle (T_s), with ($T_s \ll T_L$).

A. Grid Line-Cycle Analysis of the DM-SST Module

As the two PAC-Ćuk modules are identical and operated exclusively as captured in (1), the analysis of only Module 1 is considered in this section. Using (2), PAC-Ćuk dc/dc module, as shown in Fig. 2(b), can be simplified to Fig. 3(a). The power transfer between the input and the output ports via the HFL is defined to be p_T and is dependent on converter design parameters [32], [33] L_r and $C_r = (C_{A1} || C_{A2}/n^2)$ and the control parameters d_1, d_2, and Δ_ϕ. By performing circuit simplification [34], the equivalent capacitances for C_{T1} and C_{T2} reflected across the nodes with voltages $\langle v_1 \rangle$ and $\langle v_2' \rangle$ are found to be $C_{T1}/d_1'^2$ and $C_{T2}/d_2'^2$, respectively.

In Fig. 3(a), the impedance offered by the input and the output inductors at the line frequency is negligible compared with the impedance of the capacitors. Hence, the voltage drop across the inductors can be ignored resulting in an approximate equivalent model, as given by Fig. 3(b). The input- and output-side equivalent lumped capacitors $C_{\text{eq},1}$ and $C_{\text{eq},2}$ are obtained by combining the capacitors on the node with voltages $\langle v_1 \rangle$ and $\langle v_2 \rangle$ and are given by

$$C_{\text{eq},1} = C_{\text{in}} + C_{A1} + \frac{C_{T1}}{(1 - d_1)^2}$$

$$C_{\text{eq},2} = \frac{C_o}{n^2} + \frac{C_{A2}}{n^2} + \frac{C_{T2}}{n^2(1 - d_2)^2}. \tag{3}$$

As shown by (3), the equivalent internal capacitance of the DM-SST has dependency on the control parameters d_1 and d_2 indicating that the duty cycles can be used to control the current

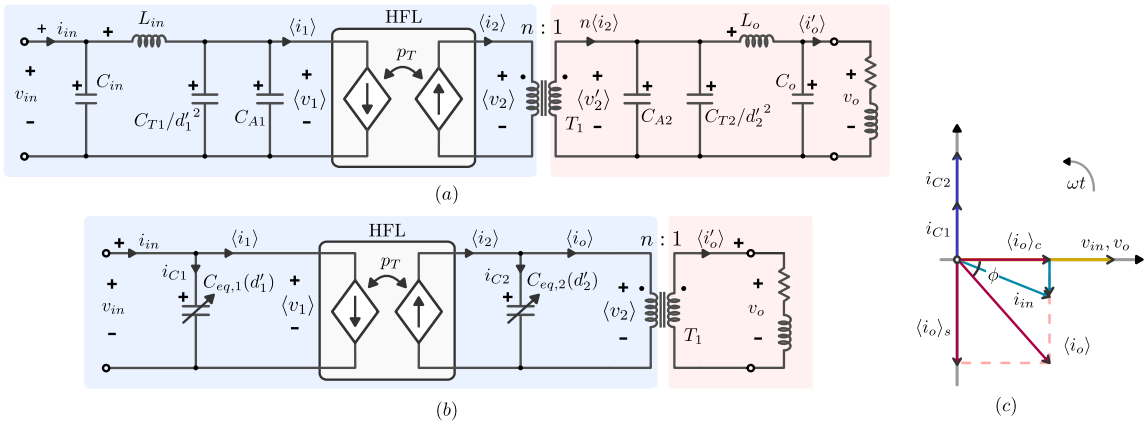

Fig. 3. (a) Detailed model, (b) approximated equivalent model, and (c) phasor diagram referred to input port of the PAC-Ćuk module.

drawn by the capacitors and absorb the inductive current of the load.

The resistive–inductive load current referred to input side $\langle i_o \rangle = n\langle i_o' \rangle$ can be written in phasor form as follows:

$$\langle i_o \rangle = |I_o| \angle (-\phi_o) = \langle i_o \rangle_c + j\langle i_o \rangle_s \tag{4}$$

where $|I_o|$ is the magnitude of the load current, ϕ_o is the lagging phase angle between v_{in} and $\langle i_o \rangle$, $\langle i_o \rangle_c$ is the real component, and $\langle i_o \rangle_s$ is the orthogonal component of the load current. The current through the capacitors $C_{\text{eq},1}$ and $C_{\text{eq},2}$ is denoted by $\langle i_{C1} \rangle$ and $\langle i_{C2} \rangle$, respectively, and is given as follows:

$$\begin{aligned} \langle i_{C1} \rangle &= \frac{v_{\text{in}}}{\omega_L C_{\text{eq},1}} \\ \langle i_{C2} \rangle &= \frac{n v_o}{\omega_L C_{\text{eq},2}}. \end{aligned} \tag{5}$$

Assuming lossless power transfer through the HFL, the current into the HFL $\langle i_1 \rangle$ is given by

$$\langle i_1 \rangle = \frac{\langle v_2 \rangle}{\langle v_1 \rangle} \langle i_2 \rangle \approx \frac{n v_o}{v_{\text{in}}} \langle i_2 \rangle = m \langle i_2 \rangle \tag{6}$$

where m is the converter gain, and $\langle i_2 \rangle = \langle i_o \rangle + \langle i_{C2} \rangle$.

In Fig. 3(c), phasor diagram of the converter is shown to illustrate the compensation capability on the orthogonal component of the load current. Using the phasor diagram, the input current i_{in} at the input port is given by

$$i_{\text{in}} = m\langle i_o \rangle_c + j\left(m\langle i_o \rangle_s - (\langle i_{C1} \rangle + m\langle i_{C2} \rangle)\right). \tag{7}$$

The capacitor currents $\langle i_{C1} \rangle$ and $\langle i_{C2} \rangle$ have dependency on d_1 and d_2 through $C_{\text{eq},1}$ and $C_{\text{eq},2}$, as given by (7), and can be used to reduce the orthogonal component of the input current resulting in improvement in power factor at the input port.

B. Switching Frequency Operation of the DM-SST Module

The power transfer p_T through the HFL formed by L_r, C_{A1}, and C_{A2} is dependent on the controller parameters d_1, d_2, and Δ_ϕ. The blocking capacitors C_{A1} and C_{A2} can be lumped into $C_r = C_{A1} \,||\, C_{A2}/n^2$ for simplification, as shown in Fig. 4(a). In [30], constant symmetric duty cycles of 0.5 are

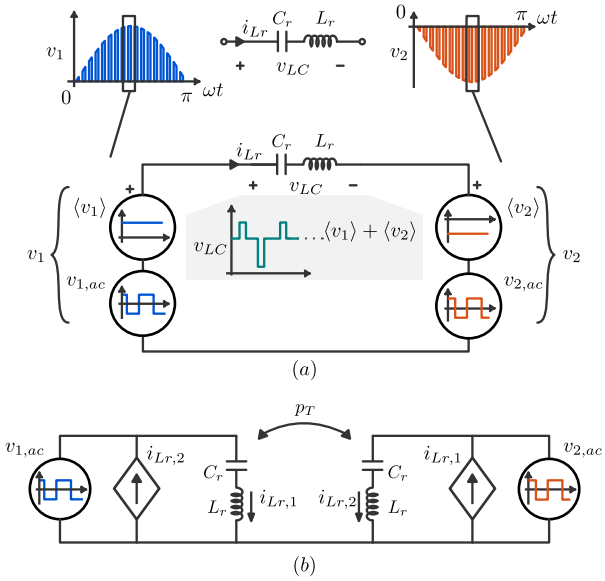

Fig. 4. Equivalent HFL circuit formed using Thévenin's theorem. (a) Simplified HFL circuit and (b) equivalent HFL circuit formed using Thevenin's theorem.

used, which simplifies the modeling of the DM-SST due to the symmetricity of the operation. However, as the duty cycles varies for reactive-power operation, a detailed model accounting for wide variation of the control parameters d_1, d_2, and Δ_ϕ is needed.

A closed-form solution for a circuit consisting of dual two-level voltage sources connected in series across the *LC* resonant tank is complex and generally realized using the first-harmonic approximation (FHA) [36], [37] for simplification. However, FHA introduces significant errors for duty cycles not equal to 0.5 and f_s not near the resonant-tank frequency $2\pi f_o$. In contrast, the circuit analysis of a two-level voltage source across an *LC* tank constitutes a second-order system with only two modes. At quasi-static state, the average current through the *LC* resonant tank is 0 A and the state variables of the *LC* resonant-tank system are readily solvable. Hence, Thévenin's theorem and principle of superimposition can be applied to decompose the circuit to the one, as shown in Fig. 4(b) [33].

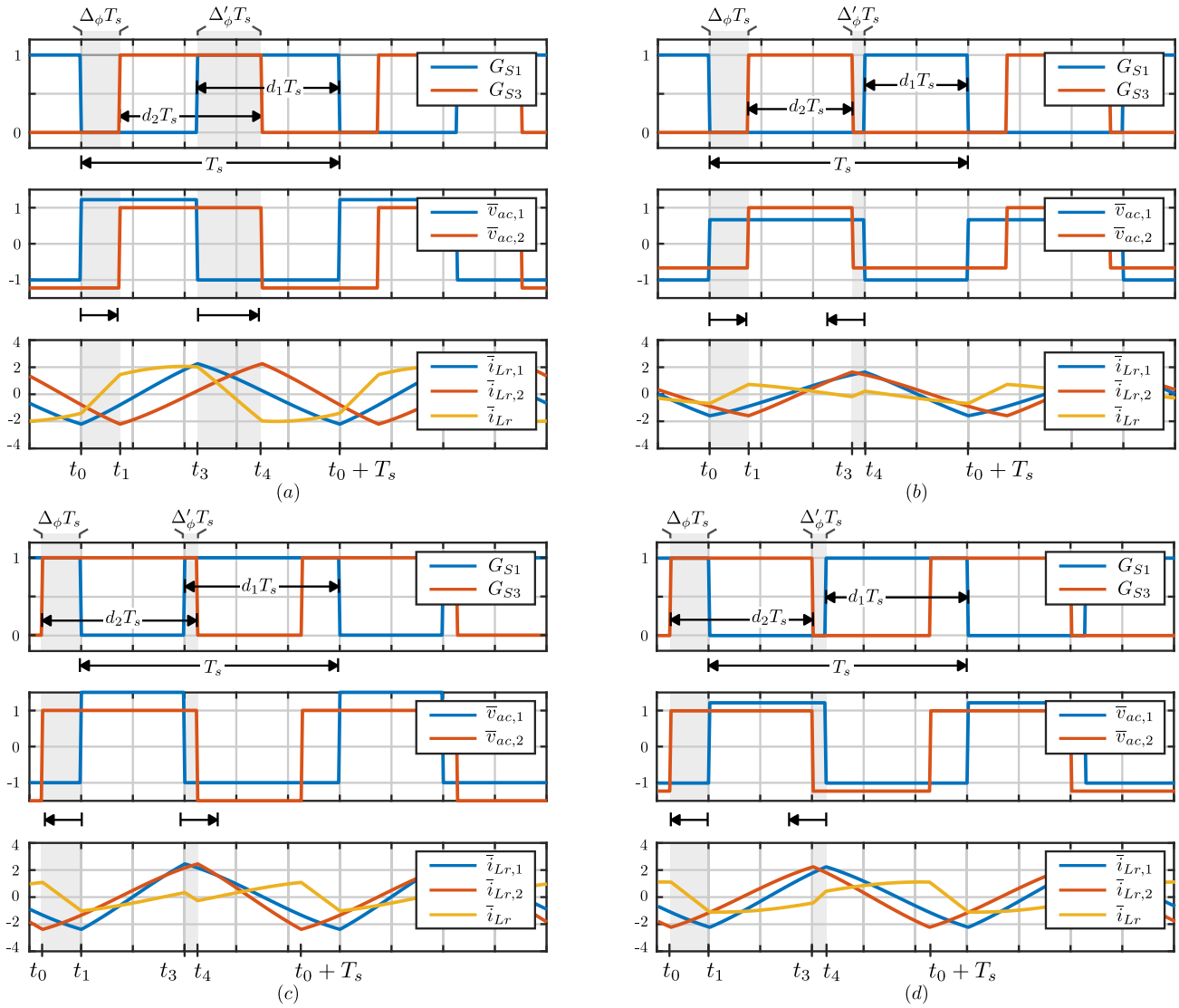

Fig. 5. Waveforms of PAC-Cuk module operating with (a) case I: $d_1 = d_2 = 0.55$, $\Delta_\phi = 0.15$, and $\Delta'_\phi = 0.25$. (b) Case II: $d_1 = d_2 = 0.40$, $\Delta_\phi = 0.15$, and $\Delta'_\phi = -0.05$. (c) Case III: $d_1 = d_2 = 0.60$, $\Delta_\phi = -0.15$, and $\Delta'_\phi = 0.05$. (d) Case IV: $d_1 = d_2 = 0.55$, $\Delta_\phi = -0.15$, and $\Delta'_\phi = -0.05$.

Fig. 4(a) shows an equivalent circuit obtained with focus on only the HFL. The nodal voltages v_1 and v_2 are decomposed in ac and dc components, as given by the following equation:

$$\begin{aligned} v_1 &= \langle v_1 \rangle + v_{1,\text{ac}} \\ v_2 &= \langle v_2 \rangle + v_{2,\text{ac}} \end{aligned} \tag{8}$$

where $v_{1,\text{ac}}$ and $v_{2,\text{ac}}$ are the normalized ac voltage sources and are defined as follows:

$$v_{1,\text{ac}} = \begin{cases} v_{\text{in}} d_1 / d'_1 & \text{for } 0 < t < d'_1 T_s \\ -v_{\text{in}} & \text{for } d'_1 T_s < t < T_s \end{cases}$$

$$v_{2,\text{ac}} = \begin{cases} n v_o & \text{for } 0 < t' < d_2 T_s \\ -n v_o d_2 / d'_2 & \text{for } d_2 T_s < t' < T_s \end{cases} \tag{9}$$

where $t' = t - \Delta_\phi T_s$.

The average dc components of v_1 and v_2 are blocked by C_r due to the high impedance of the capacitors at low frequency, as given by (2). Hence, these components does not participate in the power transfer [33] and are ignored in the analysis.

In Fig. 4(b), only the decomposed ac sources are applied on the *LC*, while the average component of the nodal voltages is ignored as net power transfer through the average component is zero over a switching period. The separation of the ac sources is performed by applying superposition theorem and Thévenin's theorem. The decomposed circuit can now be analyzed by focusing on solving the two-level circuit independently.

The current generated by $v_{1,\text{ac}}$ in the *LC* tank is denoted by $i_{Lr,1}$ and current generated by $v_{2,\text{ac}}$ in the *LC* tank is denoted by $i_{Lr,2}$. The solution for $i_{Lr,1}$ and $i_{Lr,2}$ is given as follows:

Details on solving the resonant-link current are detailed in [32] and are not repeated here. The resultant i_{Lr} can be obtained

TABLE II
EXPRESSION OF OUTPUT POWER FOR DIFFERENT CASES

Control parameter condition	Output power relation p_T
$\Delta_\phi > 0, \Delta'_\phi > 0$	$p_T = kf_1(d_1, d_2, \Delta_\phi)$
$\Delta_\phi > 0, \Delta'_\phi < 0$	$p_T = kf_2(d_1, d_2, \Delta_\phi)$
$\Delta_\phi < 0, \Delta'_\phi > 0$	$p_T = kf_3(d_1, d_2, \Delta_\phi)$
$\Delta_\phi < 0, \Delta'_\phi < 0$	$p_T = kf_4(d_1, d_2, \Delta_\phi)$

by the relation given as follows:

$$i_{Lr} = i_{Lr,1} - i_{Lr,2}. \tag{11}$$

As noted by (10) shown at the bottom of this page, the $i_{Lr,1}$ has dependency only on the input-side control parameter d_1, while $i_{Lr,2}$ has dependency on the output-side control parameter d_2 and Δ_ϕ. The net power transfer p_T from the input port to the output port is found by computing the power delivered to $v_{2,\text{ac}}$ by $i_{Lr,1}$ in T_s and is mathematically expressed as follows:

$$p_T = \frac{1}{T_s}\int_0^{T_s} v_{2,\text{ac}} i_{Lr,1} dt. \tag{12}$$

A closed-form expression for p_T can be found by separating the integration into the four modes of operation as both $v_{2,\text{ac}}$ and i_{Lr} are piecewise functions defined by (9) and (10). As with other dual two-level HFL-based topologies [38], [39], [40], [41], the modes and their sequence for the PAC-Ćuk module differ with the control parameters, as shown in Fig. 5. In the figure, $\bar{v}_{1,\text{ac}}$ and $\bar{v}_{2,\text{ac}}$ are the normalized voltages with v_{in} as the base voltage, whereas $\bar{i}_{Lr,1}$, $\bar{i}_{Lr,2}$, and $\bar{i}_{Lr}$ are the normalized currents $v_{\text{in}}/(\omega_L L_r)$ as the base current. There could be four possible cases depending on the polarity of Δ_ϕ and Δ'_ϕ, where $\Delta'_\phi = d_1 + d_2 + \Delta_\phi - 1$; hence, the closed-form solution of p_T is a piecewise function for the four cases.

For example, in Fig. 5(a) and (b), in the mode between the time periods $t_1 - t_0$, both the G_{S1} and G_{S3} are inactive as $\Delta_\phi > 0$. While for the mode between the time periods $t_4 - t_3$, both the G_{S1} and G_{S3} are active for the case, as shown in Fig. 5(a), as $\Delta'_\phi > 0$, while for the case of Fig. 5(b), both the G_{S1} and G_{S3} are inactive as $\Delta'_\phi < 0$. These discrepancies result in different solutions of (11) as $v_{2,\text{ac}}$ and $i_{Lr,1}$ are the piecewise solutions, which have different overlap regions for the two cases.

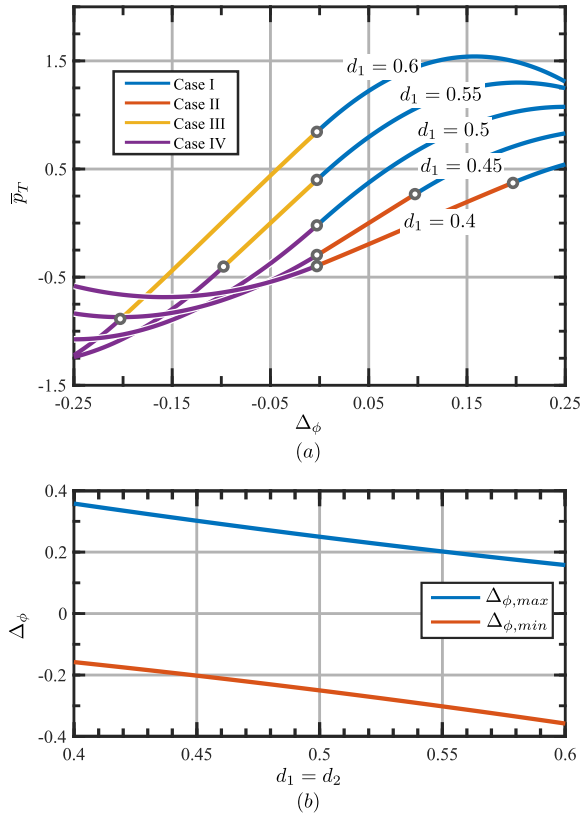

Fig. 6. (a) Output power dependency of PAC-Ćuk on the control parameters against Δ_ϕ and $d_1 = d_2$. (b) $\Delta_{\phi,\max}$ and $\Delta_{\phi,\min}$ as a function of $d_1 = d_2$.

Table II provides the output power relation p_T for the complete range of the control parameters by accounting for the four cases and solving (12). In Table II, $k = nv_{\text{in}}v_o/(d'_1 d'_2 Z_r \omega_r T_s \sin(\frac{\omega_r}{2}))$, while f_1, f_2, f_3, and f_4 are given by (12). The output power transfer through the HFL is directly proportional to input and output voltages. Fig. 6(a) showcases the normalized output power $\bar{p}_T$ ($\bar{p}_T = p_T/(nv_{\text{in}}v_o/(\omega_L L_r))$) dependency on the control parameters by utilizing the power relation obtained from (13) shown at the bottom of the next page.

As shown in Fig. 6(a), higher $d_1 = d_2$ results in higher maxima of $\bar{p}_T$ for constant Δ_ϕ. Also, the peak of the output power occurs at different ranges of Δ_ϕ for various $d_1 = d_2$. The $\bar{p}_T$ trend reverses after the peak of $\bar{p}_T$ with increasing Δ_ϕ. Hence,

$$i_{Lr,1}(t) = \begin{cases} \frac{v_{\text{in}}}{d'_1 Z_0}\frac{\sin\left(\frac{\omega_r T_s d_1}{2}\right)}{\sin\left(\frac{\omega_r T_s}{2}\right)} \sin\left(\omega_r T_s\left(\frac{t}{T_s} - \frac{d'_1}{2}\right)\right), & 0 < t < d'_1 T_s \\ \frac{v_{\text{in}}}{d'_1 Z_0}\frac{\sin\left(\frac{\omega_r T_s d'_1}{2}\right)}{\sin\left(\frac{\omega_r T_s}{2}\right)} \sin\left(\omega_0 T_s\left(-\frac{t}{T_s} + 1 - \frac{d_1}{2}\right)\right), & d'_1 T_s < t < T_s \end{cases} \tag{10a}$$

$$i_{Lr,2}(t) = \begin{cases} \frac{v_o}{d'_2 Z_0}\frac{\sin\left(\frac{\omega_r T_s d'_2}{2}\right)}{\sin\left(\frac{\omega_r T_s}{2}\right)} \sin\left(\omega_r T_s\left(\frac{t'}{T_s} - \frac{d_2}{2}\right)\right), & 0 < t' < d_2 T_s \\ \frac{v_o}{d'_2 Z_0}\frac{\sin\left(\frac{\omega_r T_s d_2}{2}\right)}{\sin\left(\frac{\omega_r T_s}{2}\right)} \sin\left(\omega_r T_s\left(-\frac{t'}{T_s} + \frac{1+d_2}{2}\right)\right), & d_2 T_s < t' < T_s \end{cases} \tag{10b}$$

where $t' = t - \Delta_\phi T_s$, $Z_r = \sqrt{L_r/C_r}$, and $\omega_r = \sqrt{1/L_r C_r}$.

the range of Δ_ϕ needs to be obtained by solving the maxima and minima of p_T for a given $d_1 = d_2$.

Fig. 6(b) provides the range of Δ_ϕ for $d_1 = d_2$ by finding the maxima and minima of f_1 and f_4, respectively. It is observed that the difference between the maximum phase-shift ratio $\Delta_{\phi,\max}$ and the minimum phase-shift ratio $\Delta_{\phi,\min}$ is near 0.25. In addition, the relation between $\Delta_{\phi,\max}$ can be approximated by a linear function of d_1 for practical application.

III. Operation of the DM-SST for Reactive Load

Single-stage ac/ac converter based on HFL with L or LC faces challenges with reactive load due to limited power transfer capability [28], [29]. This limitation arises as the power transfer relation is directly proportional to the input and the output voltages. While the maximum power transfer capability of the converter depends on the design parameters L_r, C_r, and T_s under reactive-load conditions, the instantaneous power required to be transferred through the HFL is higher than what the converter can support, resulting in significant output voltage distortion, especially near the zero crossing of the input voltage. However, due to the presence of $C_{\text{eq},2}$ in the DM-SST, the reactive-power component of the load can be absorbed by the capacitor resulting in a wide range of reactive-load-handling capacity.

A. Analysis of the Limitation for Reactive-Power Load

Equation (14) captures the required instantaneous power p'_T through the HFL for the ac/ac operation using Fig. 3(b)

$$p'_T = n v_{\text{in}} v_o \, g^* = n \langle i_2 \rangle v_o \tag{14}$$

where g^* is an ideal solution function that ensures ac/ac operation. Using (14) and Fig. 3(b), the relation of g^* for the DM-SST is given as follows:

$$g^* = \frac{\langle i_2 \rangle}{v_{\text{in}}} = \frac{|I_2|}{V_{\text{in},m}} \frac{\sin(\omega_L t - \theta)}{\sin(\omega_L t)} \tag{15}$$

where $|I_2| = \sqrt{(I_{C2} - I_o \sin(\phi_o))^2 + (I_o \cos(\phi_o))^2}$ and $\theta = \angle \tan^{-1}(\frac{I_{C2} - I_o \sin(\phi_o)}{I_o \cos(\phi_o)})$, ω_L is the angular line frequency, and $V_{\text{in},m}$ is the amplitude of the input voltage.

Fig. 7 illustrates the required g^* for various load conditions for an ac/ac converter. For $\theta = 0, g^*$ is reduced to a constant, as shown in Fig. 7(a). A constant g^* indicates only real power flow through the HFL. With increase in θ (higher reactive-power flow), the required g^* also increases in proximity of zero crossing of input voltage.

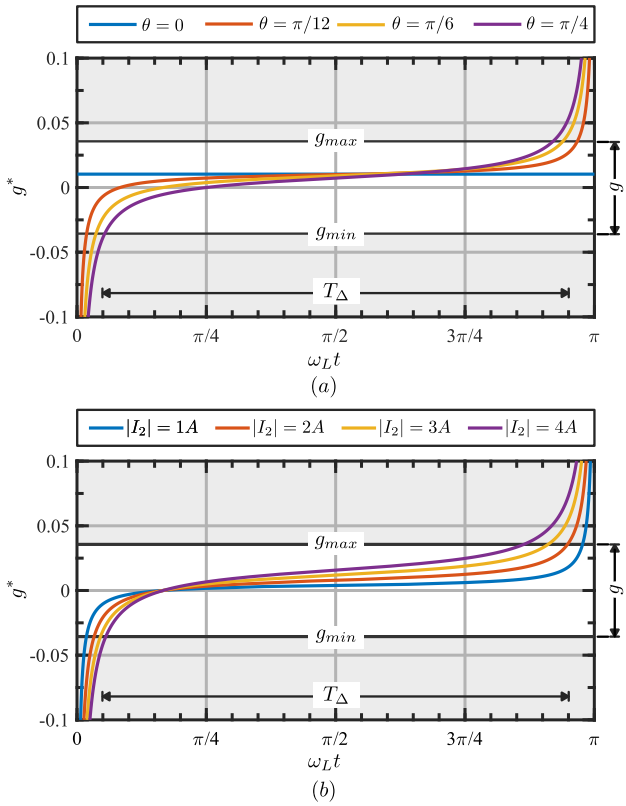

Fig. 7. (a) Solution of g^* for reactive load with constant $|I_2| = 2.3$ A and various phase condition θ through the HFL. (b) Solution of g^* for reactive load with various $|I_2|$ and constant phase $\theta = \pi/6$ through the HFL.

The solution function g, which the DM-SST can support, is given by (16) using the power transfer relation, as stated in Table II and substituting into (14)

$$g(d_1, d_2, \Delta_\phi) = \frac{f(d_1, d_2, \Delta_\phi)}{d'_1 d'_2 Z_r \omega_r T_s \sin\left(\frac{\omega_r}{2}\right)} \tag{16}$$

where $f \in \{f_1, f_2, f_3, f_4\}$ and g is dependent on the control parameters and converter design parameters. As g is bounded, $g(d_1, d_2, \Delta_\phi) = g^* \ \forall \ g_{\max} < g^* < g_{\min}$, where $g_{\max}$ and $g_{\min}$

$$f_1(d_1, d_2, \Delta_\phi) = \frac{\sin(\omega_r(\Delta_\phi + d_1 - 0.5)) + \sin(\omega_r(\Delta_\phi + d_2 - 0.5)) - \sin(\omega_r(\Delta_\phi - 0.5)) - \sin\left(\omega_r\left(\Delta'_\phi - 0.5\right)\right)}{2} - \sin\left(\frac{\omega_r}{2}\right)$$

$$f_2(d_1, d_2, \Delta_\phi) = \sin\left(\frac{\omega_r d_1}{2}\right)\left(\cos\left(\frac{\omega_r(2\Delta_\phi + d_1 - 1)}{2}\right) - \cos\left(\frac{\omega_r(2\Delta_\phi + d_1 + 2d_2 - 1)}{2}\right)\right)$$

$$f_3(d_1, d_2, \Delta_\phi) = \sin\left(\frac{\omega_r(1 - d_1)}{2}\right)\left(\cos\left(\frac{\omega_r(2\Delta_\phi + d_1 + 2d_2 - 2)}{2}\right) - \cos\left(\frac{\omega_r(2\Delta_\phi + d_1)}{2}\right)\right)$$

$$f_4(d_1, d_2, \Delta_\phi) = f_1\left(d_1, d_2, \Delta'_\phi\right) \tag{13}$$

are the maxima and minima of $g(d_1, d_2, \Delta_\phi)$. T_Δ is the duration for which $g = g^*$. Note: $g(d_1, d_2, \Delta_\phi)$ is represented by g, henceforth.

In Fig. 7, $g_{\max}$ and $g_{\min}$ bounds are obtained for $d_1 = d_2 = 0.5$. A higher θ will result in the saturation of g for a longer duration resulting in distortion in the output voltage due to the inability of the HFL to support the ac/ac operation. Fig. 7(b) illustrates the effect of the magnitude of current through the HLF on g^*. For the same θ, the trajectory of g^* is confined to the bound more for lower current and higher T_Δ. Hence, the HFL would result in lower distortion of output voltage for lower load conditions.

The DM-SST can also support higher reactive power (and higher θ) with minimal output voltage distortion by decreasing the design parameters (Z_r, ω_r, and T_s) [29] [increasing the maximum power-handling capability, as shown in Fig. 7(b)] resulting in a higher bound of g as given by the denominator of (16). However, such a modification will result in poor performance of the converter for active-power operation.

On the other hand, the DM-SST offers an extension of g through the modification of duty cycles d_1 and d_2. In addition, $\langle i_2 \rangle$ is the sum of $\langle i_o \rangle$ and $\langle i_{CT2} \rangle$, where $\langle i_{CT2} \rangle$ can be controlled using d_2 to decrease the effective reactive component of the current through the HFL. The current through the HFL is not directly related to the load current in the DM-SST but has intermediary current absorption feature controlled by the duty cycle, which provides wider operational capability for reactive loads.

B. Feedforward-Linearization Function for the Controller

The DM-SST can operate in closed loop using a simple output voltage controller with $< 2\%$ THD, which requires only input and output voltage sensors for resistive loads [30]. However, for reactive loads, the output of the controller is required to follow the solution function g^*, which is highly nonlinear, especially in proximity of zero crossing and for high reactive power. The controller needs to have higher bandwidth to be able to track such high nonlinearity, which is a limitation of voltage controllers [34]. An inner current loop-based controller can provide high bandwidth but will necessitate an additional current sensing and a complex dual-loop control structure [42], [43].

From (15), it can be noted that the nonlinearity is largely due to the presence of $\sin(\omega_L t)$ in the denominator, which is due to the sinusoidal input voltage. Hence, in this article, a linearization function is introduced so that the controller needs to address only the numerator component, which has a line frequency component as well as other nonlinearities of the converter. A proportional resonant controller (PRC) with the resonant frequency set at ω_L is used, as shown in Fig. 8. A phase-locked loop is used to obtain the phase angle of the input voltage.

IV. Design Guidelines of the DM-SST With Focus on Reactive-Power Operation

The DM-SST has the capability of extending the solution function g for ac/ac operation without changing the design parameter of the HFL. Hence, the design guidelines of the passive components of the DM-SST provided in [30] are largely valid. In this section, the dependency of region of operation of the DM-SST on the converter design and control parameters is discussed in the context of reactive load. As discussed in Section III, auxiliary capacitors C_{T1} and C_{T2} and the duty cycles d_1 and d_2 play a major role in handling the reactive loads and absorption of the reactive power. A 1-kVA DM-SST is designed in this section as per the electrical specification, as provided in Table III. The transformer turn ratio $n = 1$ is chosen to facilitate hardware implementation. At nominal operation, the converter gain $m = 1$ as $V_{\text{in}} = V_o = 220\,\text{V}_{\text{rms}}$.

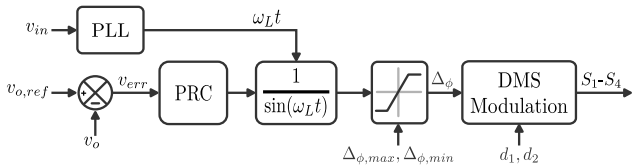

Fig. 8. Closed-loop control scheme for output voltage regulation.

TABLE III
Required Specification of the DM-SST

Parameter	Value
V_{in}	220 V_{rms}
V_o	220 V_{rms}
$S_{o,max}$	1 kVA
$Q_{o,max}$	400 VAR
f_s	40 kHz

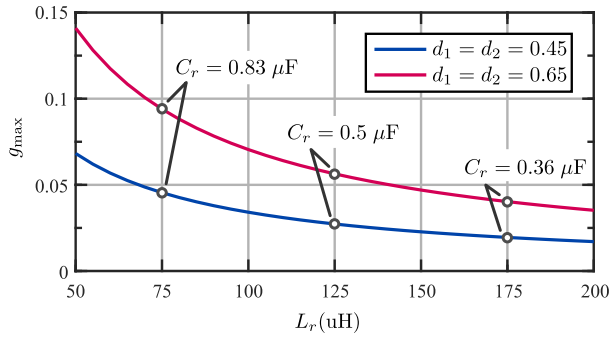

Fig. 9. Dependency of $g_{\max}$ on the HFL parameter for fixed ω_o.

A. HFL Parameters C_r and L_r

The resonance link formed by $C_r (= C_{A1} || \frac{C_{A2}}{n^2})$ and L_r plays a vital role in dictating the power flow through the link, as given by (12). The maximum and minimum values of g are governed by L_r and C_r for the given control parameters (d_1, d_2, and Δ_ϕ), as also shown by (15) and Fig. 9. A higher operational range of g enables reactive-power operation with lower distortion (higher T_Δ), as discussed in Section III and shown in Fig. 7. However, increasing the operational region of g by lowering L_r results in a higher C_r to maintain the same resonance frequency ω_r.

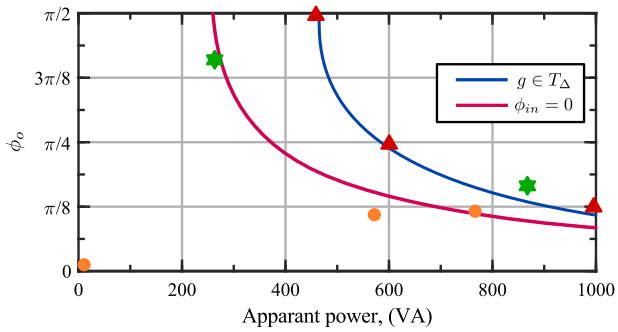

Fig. 10. Region of operation of the DM-SST for reactive loads.

A larger C_r affects the performance of the DM-SST because it results in increased capacitive current at the input port and higher phase-shift sensitivity for low-load conditions. Fig. 9 plots the dependency of $g_{\max}$ on L_r while maintaining the HFL resonance at $\omega_r = 126.5\,\text{rad/ms}$ ($f_r \cong 20\,\text{kHz}$).

The parameters of HFL for the DM-SST are optimized for active load of 1 kW, as outlined in [30], and other parameters and features of the DM-SST are used to handle reactive power without compromising the performance for pure resistive load. If the application requires wider reactive-load-handling capability, lower L_r can be used to increase the limit of $g_{\max}$.

B. Auxiliary Capacitors C_{T1} and C_{T2}

The voltage across the auxiliary capacitors in the DM-SST can be actively controlled to provide reactive-power absorption, as discussed in Section II. The minimum size constraint on C_{T1} and C_{T2} arises from the voltage ripple condition [30], whereas the maximum size constraint arises from the required reactive-power absorption by these capacitors.

The maximum reactive-power absorption $Q_{C2,\max}$ by the lumped capacitor $C_{\text{eq},2}$ present at the output side of the isolation transformer is given by (17) obtained using (3). Hence, $Q_{C2,\max}$ is the maximum reactive load for which the power flow through the HFL can be purely active power ($\theta = 0°$) and the DM-SST can support the required g^* for the entire-line cycle. Similarly, maximum reactive-power absorption $Q_{C1,\max}$ by the lumped capacitor $C_{\text{eq},1}$ is given by (18). The limit on the maximum reactive load for which the DM-SST can provide unity-power factor is obtained by adding (17) and (18), $(Q_{C1,\max} + Q_{C2,\max})$. Fig. 10 showcases the output load region for which the unity-power factor ($\phi_{\text{in}} = 0°$) can be obtained with $d_{2,\max} = d_{1,\max} = 0.65$, where $d_{2,\max}$ and $d_{1,\max}$ are the maximum allowable duty cycles d_2 and d_1, respectively. $d_{2,\max}$ and $d_{1,\max}$ are obtained as per the maximum allowable voltage of 890 V across the switches and auxiliary capacitors as given by (2) for $V_{\text{in}} = V_o = 220\,\text{V}_{\text{rms}}$. In this article, $C_{T1} = C_{T2} = 0.68\,\mu\text{F}$ is chosen to allow 200 VAR absorption through the DM-SST

$$Q_{C2,\max} = V_o^2\,\omega_L \left(C_o + C_{A2} + \frac{C_{T2}}{(1 - d_{2,\max})^2} \right) \tag{17}$$

$$Q_{C1,\max} = V_{\text{in}}^2\,\omega_L \left(C_{\text{in}} + C_{A1} + \frac{C_{T1}}{(1 - d_{1,\max})^2} \right). \tag{18}$$

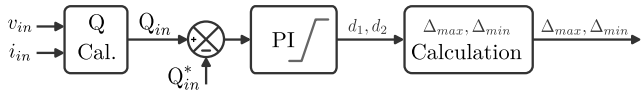

Fig. 11. Control scheme for operation of the DM-SST with reactive-load and reactive-power absorption.

C. Control Parameters d_1, d_2, and Δ_ϕ

The duty cycles d_1 and d_2 can extend the range of g, as given by (12) and (16), and hence, improve ac/ac operation for reactive-load condition. In addition, d_1 and d_2 also have control over reactive-power absorption. The maximum values of d_1 and d_2 are obtained by considering the rating of the switches and auxiliary capacitors.

In Fig. 10, the operable range of the load for the designed DM-SST is determined such that the DM-SST is following the required g^* function for the line cycle except for the 10% in proximity of the zero crossing $T_\Delta = 10\%$ of π/ω_L. The region of operation can be found by solving (19) for $\theta_{\max}$ and (20) for $\phi_{\max}$ with $\omega_L\, t_{L,m} = 0.95\pi$ (for the 10% threshold). The presence of *LC* filter formed by L_o and C_o at the output port filters the distortion, resulting in the output voltage with acceptable distortion measured using THD

$$\frac{g_{\max}(V_{o,m})^2 \sin(\omega_L t_{L,m})}{\sqrt{S^2 - Q_{C2,\max}}} = \sin(\omega_L t_{L,m} - \theta_{\max}) \tag{19}$$

where S is the apparent power, $V_{o,m}$ is the amplitude of output voltage, and $\omega_L t_{L,m}$ is the maximum radian angle for which $g = g^*$

$$\phi_{\max} = \cos^{-1}\left(\cos(\theta_{\max}) \sqrt{1 - \left(\frac{Q_{C2,\max}}{S} \right)^2} \right). \tag{20}$$

With $d_{1,\max}$ and $d_{2,\max} = 0.65$, $g_{\max} = 0.059$ is obtained. This allows DM-SST to operate with $\phi_o = 19°$ ($\text{PF}_o \approx 0.94$) at full load of 1 kVA, while 470 VA for pure reactive load. In comparison, operating the DM-SST with $d_1 = d_2 = 0.5$ results in $g_{\max} = 0.035$, which would allow the converter to operate with $\phi_o = 8°$ ($\text{PF}_o \approx 0.99$) at full load of 1 kVA, while 250 VA for pure reactive load while ensuring acceptable THD performance. Hence, higher duty cycle extends reactive-power-handling capability of the DM-SST.

Control scheme for reactive-power operation of the DM-SST is shown in Fig. 11. The input voltage and input current are used to compute the reactive power at the input port Q_{in} [44], [45]. A reactive-power reference Q^*_{in} is used to create error and fed to a proportional integer (PI) controller with saturation at $d_{\max} = 0.65$ and $d_{\min} = 0.4$. The duty cycles are used to calculate the range of $\Delta_{\phi,\min}$ and $\Delta_{\phi,\max}$ using linear approximation of plot, as shown in Fig. 6(b). For the power reference, if a unity displacement power factor ($\phi_{\text{in}} = 0°$) between the line frequency i_{in} and v_{in} is desired, $Q^*_{\text{in}} = 0$ should be used. However, the DM-SST can only compensate for maximum reactive load of $Q_{C1,\max} + Q_{C2,\max}$; beyond this limit, the controller will saturate to the maximum duty cycle.

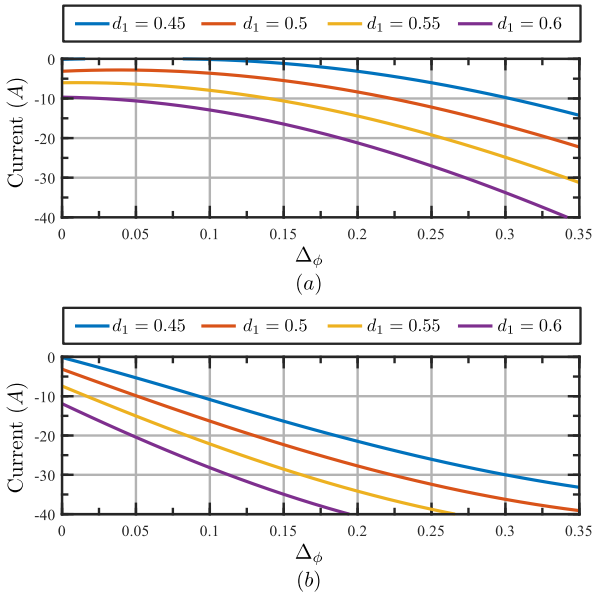

Fig. 12. Dependency of $i_{ds,ON}$ through switches (a) $\boldsymbol{S}_1$ and S_4, and (b) S_2 and S_3 for the designed DM-SST at $v_{in} = v_o = 300$ V with $d_1 = d_2$ and Δ_ϕ.

D. ZVS Region

The DM-SST offers an extensive ZVS turn-ON region for a wide load range resulting in reduced switching losses. The ZVS turn-ON of a switch requires a negative drain-to-source current $i_{\text{ds,ON}}$ through the switch before the gate transitions from OFF to ON. Hence, the extended model, as detailed in Section II, can be used to determine the polarity of $i_{\text{ds,ON}}$ to determine the ZVS turn-ON range for the DM-SST [30], [33]. Fig. 12(a) presents the $i_{\text{ds,ON}}$ for S_1 and S_4 for various duty cycles of the designed DM-SST, while Fig. 12(b) presents the $i_{\text{ds,ON}}$ for S_2 and S_3. The curves for the two switches are the same due to symmetricity in operation of the DM-SST. For S_2 and S_3, $i_{\text{ds,ON}}$ is negative and decreases monotonously with Δ_ϕ and duty cycles, hence, satisfies the ZVS turn-ON condition easily, as also noted in [33]. While for S_1 and S_4, $i_{\text{ds,ON}}$ remains flat for low Δ_ϕ and decreases with increase in duty cycles. In Fig. 12(a), ZVS condition is not satisfied for $\Delta_\phi < 0.8$ and $d_1 = d_2 = 0.45$ for which p_T is near zero or negative. In general, it can be concluded that the increase in duty cycles enhances the ZVS region of the DM-SST while improving the reactive-power-handling capability.

V. Simulation and Experimental Results

A 1-kVA DM-SST system is simulated using MATLAB-SIMULINK software and an experimental hardware is built as per the specification provided in Table IV to validate the operation and design methodology outlined in this article. The simulation results are primarily used to validate the DM-SST operation at the borderline load rating conditions marked by red triangle in Fig. 10 where various high inductive loads are required. As procuring power inductors in the order of 100 s of mH are difficult, simulation results are shown. The experimental validation of the DM-SST at the rated voltage is shown by the orange dots. The green star in Fig. 10 is the equivalent operating load condition performed at derated voltage due to rating limitation of the loads.

TABLE IV
Designed Parameters of the Prototype Converter

Parameter	Value
L_r	125 μH
L_{in}, L_o	600 μH
L_m	2 mH
C_{t1}, C_{t2}	0.68 μF
C_{b1}, C_{b1}	1 μF
C_{in}, C_o	0.68 μF

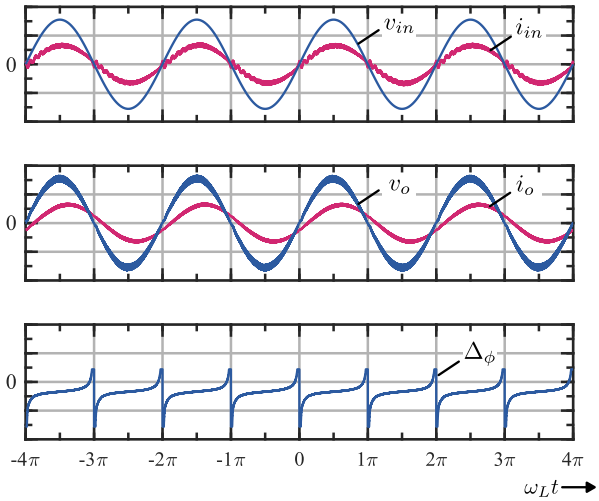

Fig. 13. Simulation results of the DM-SST with $S = 1$ kVA and $\phi_o = 22.6°$. Input voltage v_{in}:[200 V/div], output voltage v_o:[200 V/div], input current i_{in}:[10 A/div], output current i_o:[10 A/div], and Δ_ϕ:[0.25 Unit/div].

A. Simulation Results

Fig. 13 demonstrates 1 kVA and 220 V_{rms} operation of the DM-SST with $\phi_o = 22.6°$ at which duty cycles are operating at $d_{\max} = 0.65$ to maximize the possible solution function g. The DM-SST is operated in closed-loop control using the output voltage signal with linearization function as per Fig. 8. The control parameter Δ_ϕ is used to regulate the output voltage and takes the shape of solution function g for reactive power, as discussed in Section III. As duty cycles are at the maximum value, which results in maximum reactive-power absorption by the DM-SST, the fundamental component of the input current is lagging by $\phi_{\text{in}} = 6°$ with respect to the v_{in} even though i_o is lagging with $\phi_o = 22.6°$ demonstrating the reactive compensation features of the DM-SST.

Fig. 14(a) demonstrates 600 VA load operation of the DM-SST with the output current lagging the output voltage by $\phi_o = 45°$. The fundamental component of the input current is lagging by $\phi_{\text{in}} = 18°$ with respect to the v_{in}, which is higher than the previous result, as shown in Fig. 13, as the reactive

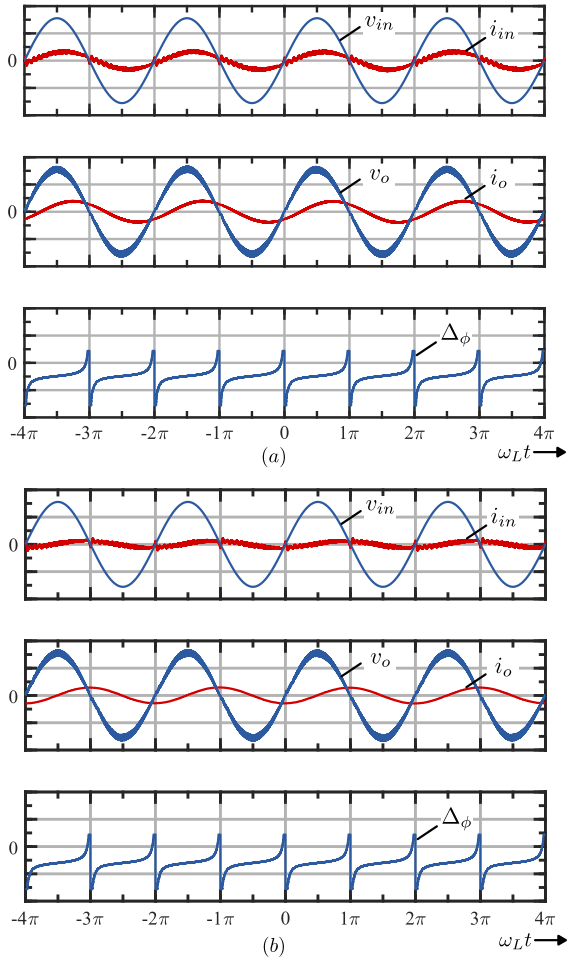

Fig. 14. Simulation results of the DM-SST with (a) $S = 600$ VA and $\phi_o = 45°$, and (b) $S = 450$ VA and $\phi_o = 90°$. Input voltage v_{in}:[200 V/div], output voltage v_o:[200 V/div], input current i_{in}:[10 A/div], output current i_o:[10 A/div], and Δ_ϕ:[0.25 Unit/div].

component of the load is also higher. The THD of the output voltage $V_{o,\text{THD}}$ is measured to be 1.09%. A simulation with the same load condition, fixed duty cycles of 0.5, and the feedforward method was conducted, which resulted in $V_{o,\text{THD}} = 7.5\%$ demonstrating the impact of duty-cycle control. Fig. 14(b) showcases the operation of the DM-SST with maximum pure reactive load ($S_o = 450$ VA, $\phi_o \approx 90°$) as per the converter design for below 5% out of bound operation. The majority of the reactive power required by the load is supplied by the DM-SST resulting in apparent power at the input port $S_{\text{in}} = 179$ VA for $d_1 = d_2 = 0.65$. Hence, the duty cycles of the DM-SST not only extend the converter capability to handle reactive load but also absorbs the reactive power. The measured $V_{o,\text{THD}}$ in the simulation is 1.17%.

B. Experimental Results

A hardware prototype, as shown in Fig. 15, is designed and built based on Tables III and IV for validation of the work outlined in this article. For the voltage source, NR Research's 9410-36 grid simulator is used, whereas Yokogawa's WT1806E is used to obtain the experimental data on THD, efficiency,

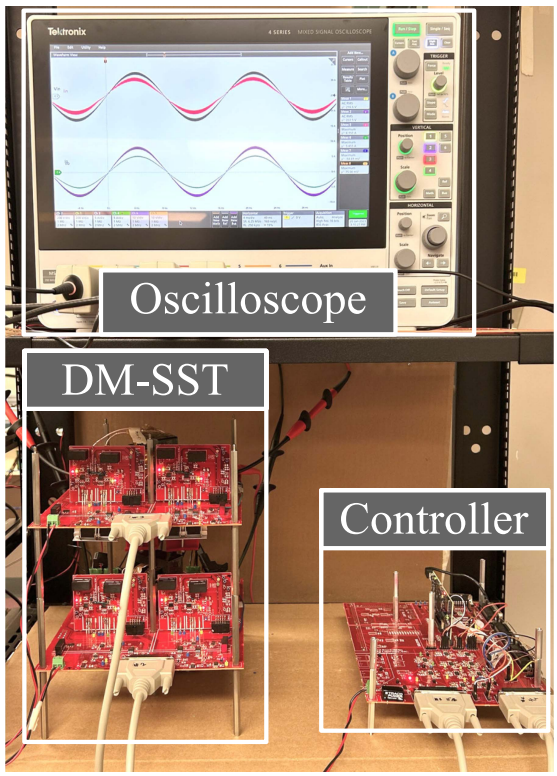

Fig. 15. Experimental prototype of the DM-SST.

power factors, and active- and reactive-power measurements. The output voltage controller with the proposed feedforward function (see Fig. 8), reactive-power absorption controller (see Fig. 11), and the DMS modulator is implemented using Texas instrument's TMS320F28379D. The control loop frequency is maintained at 40 kHz ($= f_s$).

Fig. 16(a) and (b) provides the data of the design DM-SST operated at rated input and output voltages of 220 V_{rms} for an *RL* load of $(79 + j28)\Omega$ using a 65 mH inductor. For this test, the DM-SST is operated with various duty cycles to measure the effect on input current phase angle ϕ_{in}, converter efficiency, and measured output voltage THD $V_{o,\text{THD}}$ for the given load condition. The output voltage controller is active in this test, whereas the duty cycles are manually adjusted to gather the data. The load results in the output current of $2.6\ A\angle -19.8°$.

Fig. 16(a) showcases the dependency of $d_1 = d_2$ on the ϕ_{in}. As expected from the analysis, as developed in Section II-A, increase in duty cycles results in increase in absorption of reactive power by the DM-SST causing ϕ_{in} to decrease with duty cycles. At duty cycles of 0.52, unity-power factor is achieved on the input port. With output reactive power, $Q_o = 193$ VAR, the DM-SST absorbed all the reactive powers at duty cycles of 0.52, which resulted in $S_{\text{in}} = 555$ VA, while $S_o = 572$ VA. Further increase in the duty cycles causes capacitive loading (leading input current) at the input port. Fig. 16(b) shows the efficiency and $V_{o,\text{THD}}$ plot against the duty cycles. For low value of duty cycles, the g_{max} and g_{min} are very small resulting in high distortion of the output voltage. With higher duty cycles, the $V_{o,\text{THD}}$ is near 2%. The peak measured efficiency is 97.36% at duty cycles

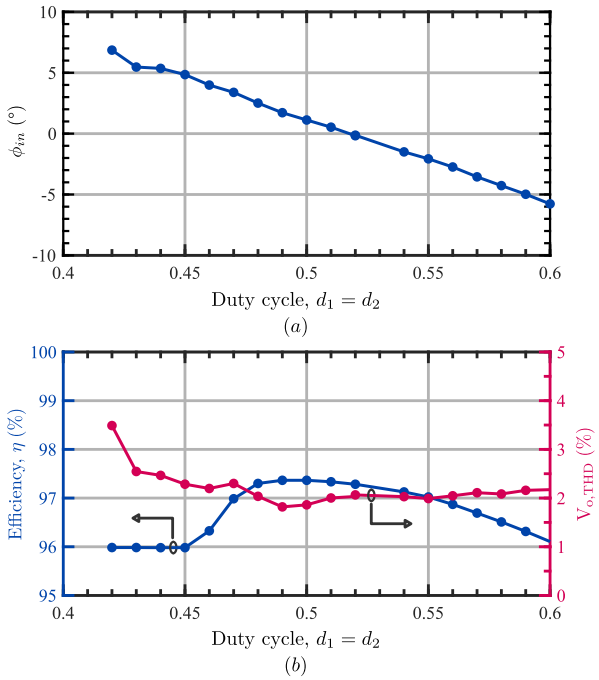

Fig. 16. Experimental data of dependency of the DM-SST operated at rated input and output voltage with $S = 572\angle 19.8^\circ$ for various duty cycles against (a) input current phase angle ϕ_{in} and (b) efficiency and measure output voltage THD $V_{o,THD}$.

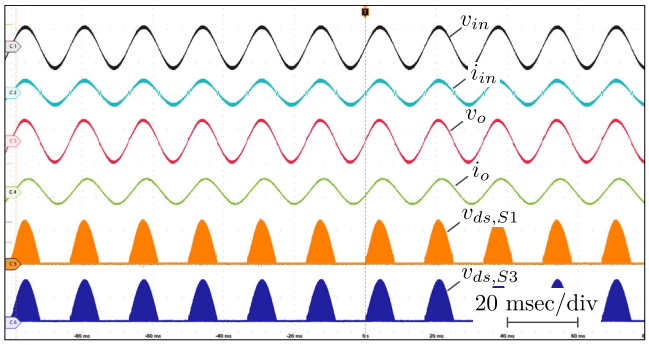

Fig. 17. Experimental waveform of the DM-SST with $d_1 = d_2 = 0.5$ with $S = 572$ VA$\angle 19.8^\circ$. Input voltage v_{in}:[500 V/div], output voltage v_o:[500 V/div], input current i_{in}:[10 A/div], output current i_o:[10 A/div], drain-to-source voltage of *S*1 $v_{ds,S1}$:[500 V/div], and drain-to-source voltage of *S*3 $v_{ds,S1}$:[500 V/div].

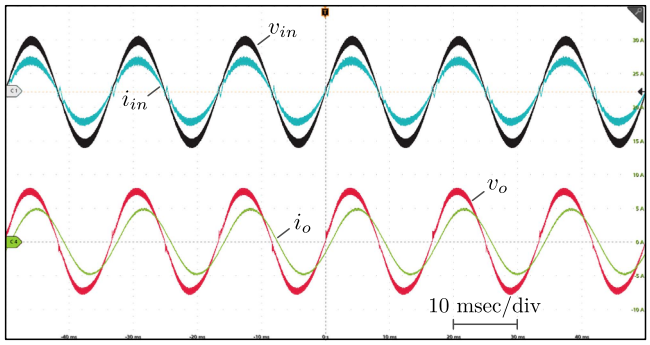

Fig. 18. Experimental result of the reactive-power compensation by DM-SST for output load of $Z_o = 62.5\ \Omega\angle 21^\circ$ at input voltage $= 220\ V_{rms}$ and output voltage $= 220\ V_{rms}$. Input voltage v_{in}:[200 V/div], output voltage v_o:[200 V/div], input current i_{in}:[5 A/div], and output current i_o:[5 A/div].

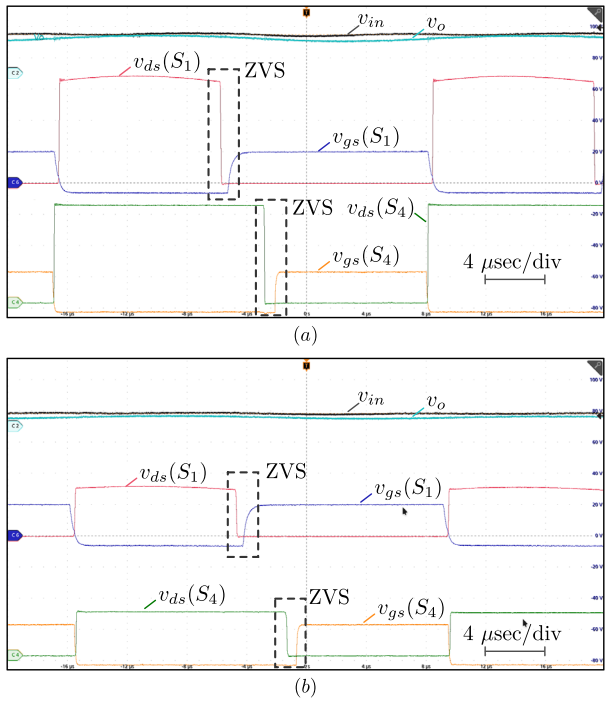

Fig. 19. Switch waveform of S_1 and S_4 showcasing ZVS turn-ON (a) near the peak and (b) zero crossing of the input voltage. Input voltage v_{in}: [200 V/div], output voltage v_o: [200 V/div], drain-to-source voltage of S_1 $v_{ds}(S_1)$: [200 V/div] and S_4 $v_{ds}(S_4)$: [200 V/div], and gate-to-source voltage of S_1 $v_{gs}(S_1)$: [20 V/div] and S_4 $v_{gs}(S_4)$: [20 V/div].

of 0.5 for the given reactive load, while the efficiency is still maintained above 96% through the sweep of the duty cycles.

Fig. 17 showcases the DM-SST waveforms for the *RL* load used in Fig. 16. The output current is lagging the output voltage by 19.8°, while the input current is lagging the input voltage by 1.7°. The $v_{\rm ds}$ of the primary-side main switch S_1 and $v_{\rm ds}$ of the secondary-side main switch S_3 are also shown operating in the DMS modulation. The envelop of the $v_{\rm ds}$ for both the switches follows the input and output voltages.

In Fig. 18, the experimental waveform of the DM-SST operating with $V_{\rm in} = V_o = 220\,{\rm V_{rms}}$ for an *RL* load of $S_o = 767\,{\rm VA}\angle 21^\circ$ is shown. In this test, the reactive-power compensator is enabled with $Q^*_{\rm in} = 0$ reference to obtain zero phase angle of input current. As $Q_{C1,\max} + Q_{C2,\max} > Q_o = 274\,{\rm VAR}$, the controller can obtain zero phase angle $I_{\rm in} = 3.4\,{\rm A}\angle -0.46^\circ$, as also shown in the figure, hence confirming and validating the reactive-power compensator capability of the designed DM-SST. The $V_{o,\rm THD} = 2.68\%$ is measured at the output port with efficiency $\eta = 96.3\%$.

Fig. 19 presents the switching waveform of S_1 and S_4 while the DM-SST is operating with the *RL* load of $S_o = 767$ VA$\angle 21^\circ$ to validate ZVS turn-ON of all the switches. Fig. 19(a) is captured near the peak of the input voltage, while Fig. 19(b) is captured near the zero crossing of the input voltage. As ZVS turn-ON of the switch is achieved if the $v_{\rm ds}$ of the switch is 0 V when gate-to-source voltage is applied, both S_1 and S_4 are undergoing

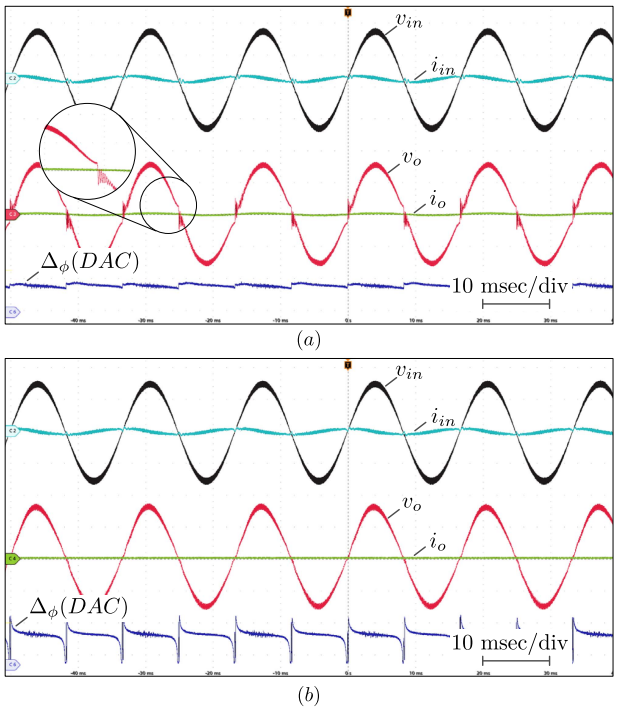

Fig. 20. Experimental waveform of the DM-SST at $V_{in} = V_o = 220\ \mathrm{V}_{rms}$ and $d_1 = 0.45$. (a) Without feedforward R =1 kΩ. (b) With feedforward no load. Input voltage v_{in}:[200 V/div], output voltage v_o:[200 V/div], input current i_{in}:[10 A/div], and output current i_o:[10 A/div].

ZVS turn-ON for both the input voltage cases. The turn-OFF of S_1 and S_4 occurs at the instance when gate-to-source voltage of the switches is removed, which indirectly indicates diode conduction of S_2 and S_3 before the removal of the gate signals. Hence, S_2 and S_3 are also undergoing ZVS turn-ON in both cases.

The feedforward-linearization function, as discussed in Section III-B, helps greatly in the application of linear controller for output voltage control, especially for low resistive load and reactive-load condition due to the requirement of highly nonlinear Δ_ϕ for ac/ac operation. Fig. 20(a) showcases the DM-SST operation for a very high resistive load (4.5% of the rated power) using a lead-lag compensator as also used in [30]. The Δ_ϕ is scaled and passed through the microcontroller (MCUs) internal digital-to-analog to capture the real-time value of the Δ_ϕ. In Fig. 20(a), the output voltage controllers have limited bandwidth due to which the output of the controller Δ_ϕ cannot rise or fall sharply as required for the DM-SST due to which significant distortion on output voltage $(V_{o,\mathrm{THD}} = 4.46\%)$ is observed near the zero crossings. At low-load condition, the capacitors along with high-load resistance on the output side of the HFL serve as an *RC* load with *R* sufficiently high to not discharge the capacitor C_{eq2} completely by the end of the half-line cycle for DMS modulation. The remnant charge on C_{eq2}, which needs to be transferred to the input port, results in deviation of the output voltage, as shown in the figure.

To demonstrate the effectiveness of the proposed feedforward controller, the waveforms for the DM-SST operated with no-load condition are shown in Fig. 20(b). No voltage jumps are observed near the zero crossing when the feedforward-linearization function is used along with PRC for the output voltage control. Δ_ϕ is at the maxima ($\Delta_{\phi,\max}$) at the start of the half-line cycle to charge the C_{eq2}, whereas Δ_ϕ reaches minima ($\Delta_{\phi,\max}$) near the end of the half-line cycle to discharge the capacitor. For the no-load operation, $V_{o,\mathrm{THD}}$ is measured at 3.38%, with $Q_{\mathrm{in}} = -138$ VAR. The proposed feedforward function also enables the operation of the DM-SST for reactive load, which is not possible with lead-lag controller alone.

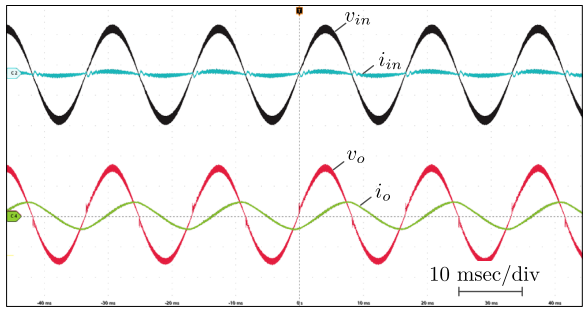

Fig. 21. Derated test of the DM-SST for high inductor load using autotransformer connected to an inductor at $V_{in} = V_o = 110\ V_{rms}$. Input voltage v_{in}:[100 V/div], output voltage v_o:[100 V/div], input current i_{in}:[5 A/div], and output current i_o:[2 A/div].

A pure reactive test at the rated input and output voltage of 220 $\mathrm{V_{rms}}$ requires a very large inductor. To facilitate the validation of the DM-SST for highly reactive load in experiment, a derated operation is performed at $V_{\mathrm{in}} = V_o = 110\ \mathrm{V_{rms}}$. An autotransformer rated for 110 $\mathrm{V_{rms}}$ is connected to the output terminal of the DM-SST whose secondary is connected with the 60 mH inductor to emulate high reactive-load condition. A 500 Ω resistor is also placed in parallel to the inductor, which allows reasonable linear operation of the setup for the reactive-load test. Fig. 21 presents the result of the DM-SST for this test. At the output port, $S_o = 66\ \mathrm{VA}\angle 74^\circ$ equivalent to $S_o^* = 264\ \mathrm{VA}\angle 74^\circ$ if the DM-SST would have operated at the rated voltages. The efficiency η of 77.8% and $V_{o,\mathrm{THD}} = 2.34\%$ is measured. The efficiency is low as most of the energy is being circulated through the DM-SST to support the reactive power while only 18 W of real power is delivered. The $V_{o,\mathrm{THD}}$ is maintained very low even though the load setup is exhibiting $I_{o,\mathrm{THD}}$ of 3.62%.

In addition, another derated *RL* load test was performed at $V_{\mathrm{in}} = V_o = 110\ \mathrm{V_{rms}}$ to operate the DM-SST out of the designed bound T_Δ, as shown in Fig. 10. The tested load is $S_o = 217\ \mathrm{VA}\angle 30^\circ$ equivalent to $S_o^* = 868\ \mathrm{VA}\angle 30^\circ$ if the DM-SST is operated at the rated voltages. As the load is out of bound, the DM-SST is operated at maximum duty cycle of 0.65 resulting in measured $V_{o,\mathrm{THD}} = 3.65\%$ and efficiency $\eta = 95.6\%$. The power measurement at the input port is $S_{\mathrm{in}} = 201\ \mathrm{VA}\angle 9^\circ$, which shows some reactive-power absorption but not sufficient to result in $\phi_{\mathrm{in}} = 0^\circ$.

VI. Conclusion

This article presents a single-stage DM-SST, which allows wide range reactive-load operation of the ac/ac converter by using PAC-Ćuk dc/dc modules. The PAC-Ćuk modules are used to take advantage of the auxiliary capacitors, which are normally

used for ZVS operation of the switches. By utilizing the duty cycles of the switches in the DM-SST, the voltage across the auxiliary capacitors is controlled that enhances the reactive-power-handling capability. The absorption capability at the output side reduces the reactive-power transfer burden on the HFL, increasing the reactive-power-handling capacity of DM-SST.

A closed-form piecewise solution of the power transfer relation for the PAC-Ćuk converter defined for full range of control parameters ($d_1, d_2,$ and Δ_ϕ) has been developed to analyze the impact of duty cycle on power transfer capability over a switching period. Notably, increasing the duty cycles not only boosts reactive-power absorption but also facilitates higher power transfer through the HFL. In addition, a feedforward-linearization function has been devised to allow output voltage control for *RL* loads. A 1-kVA hardware prototype of the DM-SST is also designed based on the design guidelines presented in this article. Simulation and experimental results for various loads are also provided to validate the proposed work. The designed DM-SST is shown to operate with output voltage THD below $<3\%$ for wide *RL* load range without compromising its performance for pure active load.

REFERENCES

[1] X. She, A. Q. Huang, and R. Burgos, "Review of solid-State transformer technologies and their application in power distribution systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 186–198, Sep. 2013, doi: 10.1109/JESTPE.2013.2277917.

[2] M. A. Hannan et al., "State of the art of solid-state transformers: Advanced topologies, implementation issues, recent progress and improvements," *IEEE Access*, vol. 8, pp. 19113–19132, 2020, doi: 10.1109/ACCESS.2020.2967345.

[3] A. Q. Huang, "Medium-voltage solid-state transformer: Technology for a smarter and resilient grid," *IEEE Ind. Electron. Mag.*, vol. 10, no. 3, pp. 29–42, Sep. 2016, doi: 10.1109/MIE.2016.2589061.

[4] H. Qin and J. W. Kimball, "Solid-state transformer architecture using AC-AC dual-active-bridge converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3720–3730, Sep. 2013, doi: 10.1109/TIE.2012.2204710.

[5] M. Su, J. Huang, H. Wang, L. Jiang, and X. Chen, "Direct AC-AC solid-state transformer based on hybrid DAB," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 2, pp. 1385–1394, Apr. 2024, doi: 10.1109/JESTPE.2023.3303455.

[6] S. Sen, L. Zhang, R. Xu, and A. Q. Huang, "Medium voltage single-stage single active bridge based solid state transformer," in *Proc. IEEE Electron. Power Grid*, 2018, pp. 1–6, doi: 10.1109/eGRID.2018.8598679.

[7] L. F. Pacheco, K. C. M. Nascimento, and I. Barbi, "Isolated AC/AC converter with LLC resonant converter high-frequency link and four-quadrant switches in the output stage," *IEEE Access*, vol. 8, pp. 213104–213114, 2020, doi: 10.1109/ACCESS.2020.3040617.

[8] W. Khan, J. A. Dar, K. S. Parihar, and M. K. Pathak, "Analysis of a new single-stage AC/AC converter for solid-state transformer," *IEEE Trans. Ind. Appl.*, vol. 60, no. 2, pp. 3359–3372, 2023, doi: 10.1109/TIA.2023.3343312.

[9] W. Xu, S. Rajendran, Z. Guo, A. Vctrivelan, and A. Q. Huang, "7.2kV/100kVA solid state transformer based on half bridge LLC resonant converter and 15kV SiC AC switch," in *Proc. Conf. IEEE Appl. Power Electron. Conf. Expo.*, 2023, pp. 1516–1522, doi: 10.1109/APEC43580.2023.10131549.

[10] H. Wang, S. Yuan, L. Jiang, T. Yu, and M. Su, "Single-stage matrix-type power electronic transformer with reduced switches," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 2, pp. 1427–1436, Apr. 2024, doi: 10.1109/JESTPE.2023.3292361.

[11] M. A. Tawfik, M. Ehab, A. Ahmed, and J.-H. Park, "Single-stage isolated AC/AC converter with phase-shifted controller," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 2, pp. 1815–1826, Apr. 2023, doi: 10.1109/JESTPE.2022.3219023.

[12] P. Waide and C. U. Brunner, "Energy-efficiency policy opportunities for electric motor-driven systems," Int. Energy Agency, Paris, France, Ch. 2, pp. 20–28, 2011.

[13] Eaton, "Power factor correction : A guide for the plant engineer," *Power Factor Correction Guid. Plant Engineer*, vol. 1, no. 1, pp. 2–15, 2020.

[14] J. Khodabakhsh and G. Moschopoulos, "Solid State transformers as enhanced smart inverters for power quality improvement in active distribution networks," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 1230–1235, doi: 10.1109/ECCE47101.2021.9595705.

[15] L. F. Costa, G. De Carne, G. Buticchi, and M. Liserre, "The smart transformer: A solid-state transformer tailored to provide ancillary services to the distribution grid," *IEEE Power Electron. Mag.*, vol. 4, no. 2, pp. 56–67, Jun. 2017, doi: 10.1109/MPEL.2017.2692381.

[16] X. Gao, F. Sossan, K. Christakou, M. Paolone, and M. Liserre, "Concurrent voltage control and dispatch of active distribution networks by means of smart transformer and storage," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6657–6666, Aug. 2018, doi: 10.1109/TIE.2017.2772181.

[17] J. Burkard and J. Biela, "Evaluation of topologies and optimal design of a hybrid distribution transformer," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, 2015, pp. 1–10, doi: 10.1109/EPE.2015.7309097.

[18] I. P. Filed, I. C. Commission, and D. No, "Report on impact of smart inverters with volt /var on ComEd's voltage optimization program table of contents page i," no. 18, 2019. [Online]. Available: https://icc.illinois.gov/downloads/public/edocket/506189.PDF

[19] A. Savasci, A. Inaolaji, and S. Paudyal, "Two-stage volt-VAr optimization of distribution grids with smart inverters and legacy devices," *IEEE Trans. Ind. Appl.*, vol. 58, no. 5, pp. 5711–5723, Sep./Oct. 2022, doi: 10.1109/TIA.2022.3183182.

[20] O. C. Da Silva Filho, F. L. Tofoli, L. H. S. C. Barreto, and D. De Souza Oliveira, "Single-phase isolated AC-AC symmetrical full-bridge converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 1, pp. 846–855, Feb. 2022, doi: 10.1109/JESTPE.2021.3107335.

[21] A. Chambayil and S. Chattopadhyay, "A single-stage single phase bidirectional AC-AC converter for solid state transformer application," in *Proc. 10th IEEE Int. Conf. Power Electron. Drives Energy Syst.*, 2022, pp. 1–6, doi: 10.1109/PEDES56012.2022.10080768.

[22] O. C. D. S. Silva, F. L. Tofoli, D. D. A. Honorio, L. H. S. C. Barreto, and D. D. S. Oliveira, "Single-phase isolated AC-AC converters based on the dual active bridge converter," *IEEE Trans. Ind. Electron.*, vol. 69, no. 6, pp. 5680–5689, Jun. 2022, doi: 10.1109/TIE.2021.3088363.

[23] A. L. Eshkevari, H. F. Ahmed, and I. Abdoli, "An isolated identical bipolar buck-boost AC-AC converter with step-changed frequency operation and reduced active and passive components," *IEEE Trans. Power Electron.*, vol. 39, no. 2, pp. 14827–14837, Nov. 2024, doi: 10.1109/TPEL.2024.3434564.

[24] S. Fathi, S. M. J. Mousavi, and E. Babaei, "A high-frequency isolated four-switch single-phase quasi-Z-source AC-AC converter with inherent commutation and step-changed frequency operation," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4937–4944, Apr. 2023, doi: 10.1109/TPEL.2022.3228939.

[25] H. F. Ahmed, M. S. E. Elmoursi, B. Zahawi, K. Al Hosani, and A. A. Khan, "Single-phase symmetric-bipolar-type high-frequency isolated buck-boost AC-AC converter with continuous input and output currents," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11579–11592, Oct. 2021, doi: 10.1109/TPEL.2021.3073236.

[26] L. Zheng, R. P. Kandula, and D. Divan, "Soft-switching solid-state transformer with reduced conduction loss," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5236–5249, May 2021, doi: 10.1109/TPEL.2020.3030795.

[27] A. Sepahvand, M. Doshi, V. Yousefzadeh, J. Patterson, K. K. Afridi, and D. Maksimovic, "Automotive LED driver based on high frequency zero voltage switching integrated magnetics Ćuk converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–8, doi: 10.1109/ECCE.2016.7854893.

[28] Q. Huang, S. Rajendran, S. Sen, Z. Guo, L. Zhang, and A. Q. Huang, "500kVA hybrid solid state transformer (HSST): Architecture, functionality and control," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 4864–4871, doi: 10.1109/ECCE44975.2020.9235435.

[29] K. J. Veeramraju, A. Sharma, and J. W. Kimball, "A comprehensive analysis on complex power flow mechanism in an AC-AC dual active bridge," in *Proc. IEEE Power Energy Conf. Illinois*, 2022, pp. 1–6, doi: 10.1109/PECI54197.2022.9744009.

[30] S. Gupta and S. K. Mazumder, "A differential-mode isolated AC/AC converter," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 12846–12858, Oct. 2023, doi: 10.1109/TPEL.2023.3292983.

[31] D. Sur, S. Gupta, M. D. R. Greidanus, and S. K. Mazumder, "Spectral-decomposition based mitigation of radiative side-channel noise intrusion in a cascaded SST," *IEEE Trans. Power Electron.*, vol. 40, no. 2, pp. 2674–2679, Feb. 2025, doi: 10.1109/TPEL.2024.3477274.

[32] S. Gupta and S. K. Mazumder, "Analysis of resonant PWM active-clamp Ćuk DC/DC converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2023, pp. 2170–2176, 2023, doi: 10.1109/APEC43580.2023.10131318.
[33] S. Gupta and S. K. Mazumder, "A novel modulation scheme for isolated PWM active-clamp Ćuk DC/DC converter," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14966–14980, Dec. 2022, doi: 10.1109/TPEL.2022.3189672.
[34] R. W. Erickson and D. Maksimović, "Fundamentals of power electronics," in *Fundamentals of Power Electronics*. Cham, Switzerland: Springer, 2020, doi: 10.1007/978-3-030-43881-4.
[35] S. Ćuk and R. D. Middlebrook, "Advances in switched-mode power conversion: Part I," *IEEE Trans. Ind. Electron.*, vol. IE-30, no. 1, pp. 10–19, Feb. 1983, doi: 10.1109/TIE.1983.356697.
[36] Z. Li, Y. Zhang, and M. Zhao, "Model and control for transient process of dual-bridge series resonant converter," *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 9202–9220, Aug. 2024, doi: 10.1109/TPEL.2024.3387939.
[37] S. Hu, X. Li, and A. K. S. Bhat, "Operation of a bidirectional series-resonant converter with minimized tank current and wide ZVS range," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 904–915, Jan. 2019, doi: 10.1109/TPEL.2018.2818145.
[38] A. Tong, L. Hang, G. Li, X. Jiang, and S. Gao, "Modeling and analysis of a dual-active-bridge-isolated bidirectional DC/DC converter to minimize RMS current with whole operating range," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5302–5316, Jun. 2018, doi: 10.1109/TPEL.2017.2692276.
[39] F. Krismer and J. W. Kolar, "Closed form solution for minimum conduction loss modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 174–188, Jan. 2012, doi: 10.1109/TPEL.2011.2157976.
[40] A. K. Jain and R. Ayyanar, "PWM control of dual active bridge: Comprehensive analysis and experimental verification," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1215–1227, Apr. 2011, doi: 10.1109/TPEL.2010.2070519.
[41] M. Mahdavifard and S. A. Khajehoddin, "Closed-form continuous asymmetrical hybrid modulation, ensuring wide ZVS range and seamless transients for DAB converters," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 5776–5792, May 2024, doi: 10.1109/TPEL.2024.3367279.
[42] C. Bao, S. Gupta, and S. K. Mazumder, "Modeling and analysis of peak-current-controlled differential mode Ćuk inverter," in *Proc. IEEE 12th Int. Symp. Power Electron. Distrib. Gener. Syst.*, 2021, pp. 1–7, doi: 10.1109/PEDG51384.2021.9494167.
[43] N. Kumar, M. Mohamadi, and S. K. Mazumder, "Passive damping optimization of the integrated-magnetics-based differential-mode ćuk rectifier," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10008–10012, Oct. 2020, doi: 10.1109/TPEL.2020.2981918.
[44] H. Akagi, Y. Kanazawa, and A. Nabae, "Instantaneous reactive power compensators comprising switching devices without energy storage components," *IEEE Trans. Ind. Appl.*, vol. IA-20, no. 3, pp. 625–630, May 1984, doi: 10.1109/TIA.1984.4504460.
[45] S. Xu, J. Wang, and J. Xu, "A current decoupling parallel control strategy of single-phase inverter with voltage and current dual closed-loop feedback," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1306–1313, Apr. 2013, doi: 10.1109/TIE.2011.2161660.

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